



**UNIVERSITY OF
BIRMINGHAM**

**DIRECT INTEGRATION OF PUSH-PULL AMPLIFIER
AND APERTURE COUPLED ANTENNA**

BY

FARID ZUBIR

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School of Electronic, Electrical & Systems Engineering

University of Birmingham

Edgbaston, B15 2TT

Birmingham

United Kingdom

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ABSTRACT

The work described in this thesis concerns the integration of push-pull class B amplifier and antenna modules. Push-pull class B is well-known with its fruitful advantages of using differential feeding technique, resulting in low distortion, reasonably high efficiency and high output power. Meanwhile, the antenna module in this work is adapted from the aperture-coupled antenna structure due to its degree of freedom to control the variables which provide the best possible topology that could be realised in system on chip or system in package. More generally, the variables allow good coverage of the Smith Chart so that a wide range of odd-mode matching requirements could be met, for different devices and bias condition of a given transistor. The approach also offers additional filtering up to 3rd harmonic in that it comprises identical harmonic traps on both sides of the aperture using resonant stubs to form bandstop filters, which reduce the ripples at the output waveforms, giving them a significant advantage of neat and tight integration of a push-pull transmitting amplifier.

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PUBLICATIONS

1. F. Zubir, P. Gardner, “A New Power Combiner Using Aperture Coupling Technique for Push-pull Class B Power Amplifier”, IET 4th Annual Passive RF and Microwave Components Seminar, 18th March 2013, Birmingham, United Kingdom.
2. F. Zubir, P. Gardner, “Multilayer Antennas with Harmonic Filtering for Differentially Fed Power Amplifier Integration”, ICEAA – IEEE APWC – EMS 2013, 9th – 13th September 2013, Torino, Italy.
3. F. Zubir, P. Gardner, “Differentially Fed Multilayer Antennas with Harmonic Filtering for Push-pull Class B Power Amplifier Integration”, The 43rd European Microwave Conference (EuMC), 8th – 10th October 2013, Nuremberg, Germany.
4. F. Zubir, P. Gardner, “Design of Optimum Matching Networks for Push-Pull Amplifier – Antenna Modules”, IET Colloquium on Antennas, Wireless and Electromagnetics, 27th May 2014, Ofcom, Riverside House, 2a Southwark Bridge Road, London.
5. F. Zubir, P. Gardner, M. K. A. Rahim, “New Technique to Comply with Impedance Requirement of Transistor for Push-Pull Amplifier”, Radio Frequency and Microwave Conference 2015, RFM 2015. IEEE International.

ABBREVIATIONS

RF	-	Radio Frequency
IC	-	Integrated Circuit
T/R SW	-	Transmit/Receive Switch
LNA	-	Low Noise Amplifier
PA	-	Power Amplifier
RX	-	Receiver
TX	-	Transmitter
GND	-	Ground
SRD	-	Short Range Device
InP	-	Indium Phosphide
SiGe	-	Silicon Germanium
GaN	-	Gallium Nitride
GaAs	-	Gallium Arsenide
MMIC	-	Monolithic Microwave Integrated Circuit
EM	-	Electromagnetic
SWR	-	Standing Wave Ratio
VCCS	-	Voltage Control Current Source
DC	-	Direct Current
AC	-	Alternative Current
PAE	-	Power Added Efficiency
IMD	-	Intermodulation Distortion
FET	-	Field-Effect Transistor

MESFET	-	Metal-Semiconductor Field-Effect Transistor
IF	-	Intermediate Frequency
FEM	-	Finite Element Method
FDTD	-	Finite Difference Time Domain
MoM	-	Method of Moment
PT	-	Total Power
AWRDE	-	Applied Wave Research Design Environment Microwave Office
MWO		
CST MWS	-	Computer Simulation Technology Microwave Studio
BSF	-	Bandstop Filter

TABLE OF CONTENT

ABSTRACT

ACKNOWLEDGEMENT

PUBLICATIONS

ABBREVIATIONS

CHAPTER 1: INTRODUCTION

1.1	Overview of Wireless Communications	1
1.2	Motivation and Objectives	3
1.3	Thesis Organisation	11

CHAPTER 2: BACKGROUND AND LITERATURE REVIEW

2.1	Overview	14
2.2	Microwave Theory	16
2.2.1	S-Parameters	17
2.2.2	Mismatch	18
2.2.3	Transmission Lines	20
2.2.3.1	Microstrip	20
2.2.4	Balun Theory	24
2.2.4.1	Ideal Balun	25
2.2.4.2	Balun Categories	28
2.3	Ideal Transistor Model	31

2.4	Conventional Power Amplifier Classes	32
2.4.1	Class A	34
2.4.2	Class B	36
2.4.3	Class AB	40
2.4.4	Class C	41
2.5	Integrated Circuit Antenna	42
2.5.1	Amplifying Antennas	44
2.5.2	Quasi-optical Power Combining and Self-oscillating Active Antennas	46
2.5.3	Frequency Tuneable and Converting Active Antennas	48
2.5.4	Active Transceiver Antennas	49
2.6	Microstrip Patch Antennas	50
2.6.1	Coaxial Probe	55
2.6.2	Microstrip Line	57
2.6.3	Aperture Coupled Microstrip Feed	58
2.7	Microstrip Slot Antennas	60
2.7.1	Coaxial Probe	62
2.7.2	Microstrip Line	63
2.8	Balanced Fed Antennas	64
2.9	Summary	70

CHAPTER 3: DESIGN OF PUSH-PULL CLASS B POWER AMPLIFIER

3.1	Introduction	72
3.2	History of Push-pull Output	73
3.3	Design Architecture of Push-pull Power Amplifier	74

3.4	Research Design Flow Charts	76
3.5	Design Procedure	79
3.5.1	Input Matching Setting	81
3.5.2	DC Analysis	83
3.5.3	Optimum Load Impedance	89
3.5.4	Integrated Biasing and Matching Networks	94
3.5.5	Power Splitter and Combiner	96
3.5.6	Optimisation with Lossy Components	99
3.6	Effect of Higher Order Harmonics Filtering	100
3.7	Summary	103

CHAPTER 4: DIFFERENTIALLY FED APERTURE COUPLED ANTENNA

4.1	Introduction	105
4.2	Differential Aperture Coupling Technique for Push-pull Transmitting Amplifier	106
4.2.1	Conceptual of Single Fed Aperture Coupled Antenna	109
4.2.2	50Ω Differential Input Version	111
4.2.3	Complex Arbitrary Input Impedance Version	119
4.3	Parametric Study on Design Slot A	129
4.3.1	Effect of Filter Width Variation	130
4.3.2	Effect of Slot Width Variation	132
4.3.3	Effect of Slot Length Variation	134
4.3.4	Effect of Moving Filter Point	136
4.4	Parametric Study on Design Slot B	138
4.5	Summary	141

CHAPTER 5: FULLY INTEGRATED AMPLIFIER–ANTENNA

SIMULATIONS AND MEASUREMENTS

5.1	Introduction	144
5.2	Push-pull Transmitting Amplifier	145
5.3	Wilkinson Power Splitter / Divider	148
5.4	Biasing Decoupling Circuit	150
5.5	Comparison of Push-pull Amplifier Topologies	153
5.6	Fully Integrated Push-pull Transmitting Amplifier	154
5.7	Measurement	156
5.8	Summary	160

CHAPTER 6: SUMMARY, CONCLUSION AND FUTURE WORK

6.1	Summary	162
6.2	Conclusion	164
6.3	Future Work	165

REFERENCES	167
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CHAPTER 1

INTRODUCTION

1.1 Overview of Wireless Communications

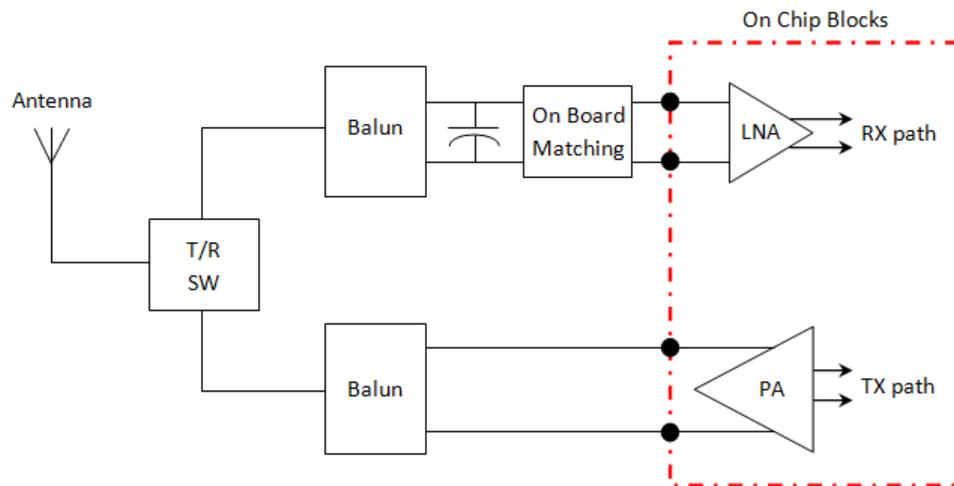
Wireless communications systems represent a branch of technology concerned with the communication engineering industry, which is taking place around the globe and is still developing rapidly. This explosive growth industry has created a mass market based on the media and consumers. For instance, the projected growth of the number of mobile phone users to billions worldwide indicates potential development in wireless communication technologies including mass-market consumer products. Billions of subscribers and a growing market for handheld devices over the years, demanding enhanced wireless communication services, lead operators to invest billions of dollars in spectrum for 3rd Generation (3G) systems, such as UMTS and most recently 4th Generation (4G) systems like LTE. The revolution of such systems is focussed towards larger capacity, better quality, more bandwidth, wider coverage, lower power consumption, high efficiency, mobility and more services. However, with an explosion of wireless mobile devices and services, there are still some challenges that cannot be accommodated by 4G, such as the spectrum crisis and high energy consumption. Wireless system designers have been facing the continuously increasing demand for high data rates and mobility required by new wireless applications and therefore have started research on fifth generation

(5G) that are expected to be deployed beyond 2020. There is an expectation that everyone will be permanently connected to the internet, no matter where they are. People are expecting that more information of a higher quality is delivered immediately and therefore newer services require higher data volumes and transfer rates. The aim is to connect the entire world and achieve seamless and ubiquitous communications between anybody (people to people), anything (people to machine, machine to machine), wherever they are (anywhere), whenever they need (anytime), by whatever electronic devices/services/networks they wish (anyhow). This means that 5G technologies should be able at least to support communications for some requirements which are not supported by 4G systems like relatively low power consumptions, higher efficiency, higher capacity, wider bandwidth and better coverage. This development remains a technical challenge with many issues still to be resolved in order to deliver the desired performance by taking into consideration the fact that is necessary to bear all or part of the weight of emerging applications. In this thesis, we propose a transmitter architecture based on a direct integration technique between power amplifier and antenna that can minimise the losses and thereby improve the whole system efficiency. This promising solution could be potentially adopted in 5G systems in order to deliver some of the aforementioned targeted requirements.

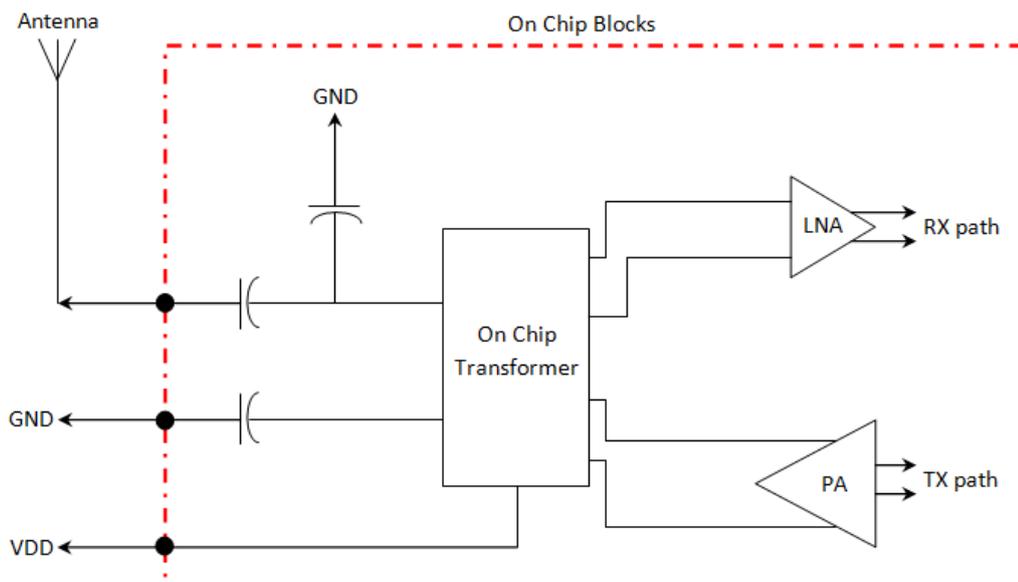
1.2 Motivation and Objectives

In recent years, intense development and fierce competition in the wireless communications industry has generated ambitious requirements for 4G LTE and most recently is 5G on radio frequency (RF) and microwave systems. The increasing demands are becoming more stringent and very difficult to achieve. Consumers demand for handy and compact devices drives the technology to integrate all necessary components and features neatly into a small space which is able to perform better in terms of energy efficient, coverage and wider bandwidth or at least has the same function as its larger version of circuit of discrete components. Furthermore, more people crave faster internet access and advanced multimedia capabilities on the move, trendier mobiles and in general, instant communication with others or access to information. In other words, the trends towards small, handy devices dictate a compact and low cost fully integrated RF and microwave front-end.

RF and microwave transceivers with the quality of being functional in the integrated circuit (IC) form have become more popular [1]. Nowadays, nearly all of the transceiver functionality could be realised in system on chip. Bhatti et al [2] has sufficient evidence through demonstration about the feasibility of establishing the integration of the balun into the combined radio transmitter and receiver. It is shown in Fig. 1.1.



(a) Conventional transceiver with some important sub-circuits are externally incorporated with the chip block.



(b) Transceiver with all discrete components lie within the chip block making it compact and handy.

Fig. 1.1: Transceiver front-end architectures.

As shown in Fig. 1.1(a), the conventional front-end transceiver architecture had some externally built discrete components like switch, baluns, antenna as well as

matching circuits which are incorporated with the on-chip blocks/modules which comprise the most power consuming active devices such as low noise amplifier (LNA) and power amplifier (PA). As can be seen in Fig. 1.1(b), other than the antenna, all discrete components within the transceiver front-end architecture could now be integrated as well as realised in system-on-chip blocks/modules. Simultaneously, this new architecture has impressively reduced the usage of discrete components, resulting in production of low cost RF and microwave front-end wireless devices. As reported by Bhatti et al in [2], there is still a need to accept responsibility for negative outcomes even though most of the discrete components have been made in system-on-chip blocks/modules. This is because on-chip transformer placement within the architecture still has an insertion loss of about 2.5 dB.

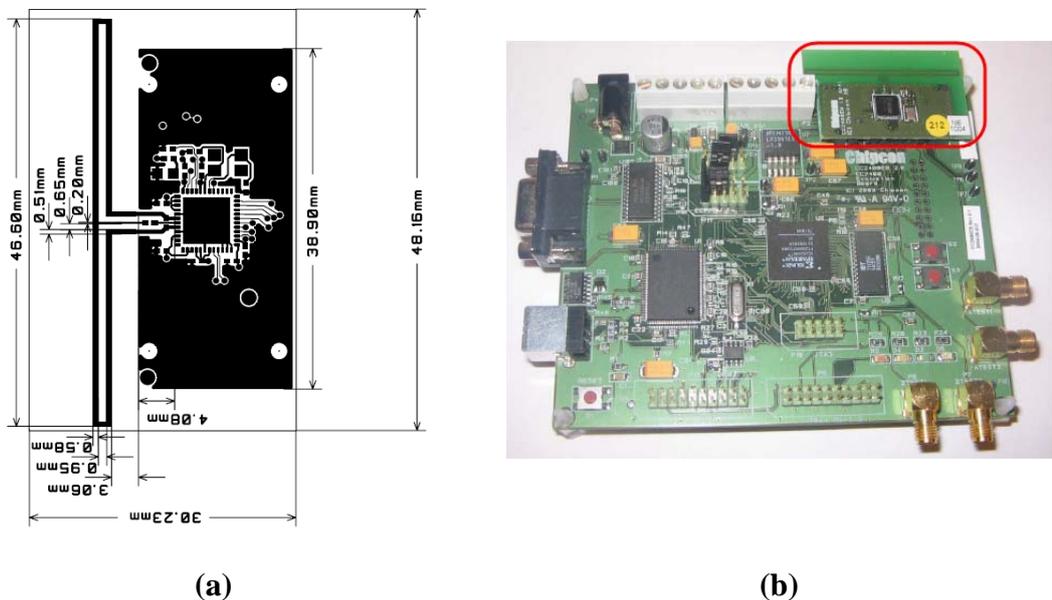


Fig. 1.2: (a) Layout of folded dipole on a single-chip transceiver. (b) Evaluation board with folded dipole on a single-chip transceiver. (reprinted from [2])

Fig. 1.2 shows a further example of reasonably small off-chip electrically short folded dipole antenna with the evaluation board. This folded dipole antenna has been specifically designed to be incorporated with a true single-chip general purpose transceiver at 2.4 GHz short range device (SRD) band for data rates up to 1 Mbps [3]. As this folded dipole behaves like a balanced antenna, it fits well with the differential interface that is shared by the PA and LNA during transmission and reception respectively.

The integration of an absolute transceiver front-end into a true single-chip solution requires a great amount of effort. The work to integrate a whole set of functions in the integrated package would be favourable and beneficial. The advantage of integrating the entire wireless communication system in one package has given encouragement and motivation for researchers around the world to study and investigate on several semiconductor dielectric substrate using fabrication technologies such as Indium Phosphide (InP), Silicon Germanium (SiGe), Gallium Nitride (GaN) and Gallium Arsenide (GaAs) [4 – 6]. Fig. 1.3 shows relative merits of the commercially available RF and microwave low noise transistor examples. This data has been taken from commercial datasheet for NEC 2SC5761 (SiGe BJT), Bipolarics B12V114 (Si BJT) and Avago VMMK-1225 (PHEMT). On the other hand, Fig. 1.4 shows another relative merits of power transistor technologies which have been derived by Aaron Oki et al [7]. The choice of devices and device technologies used in this work is taken from the range of power transistors that using GaN fabrication technology. The selection of device technologies is based on its potential of very high output power, and efficient operation almost up to 100 GHz.

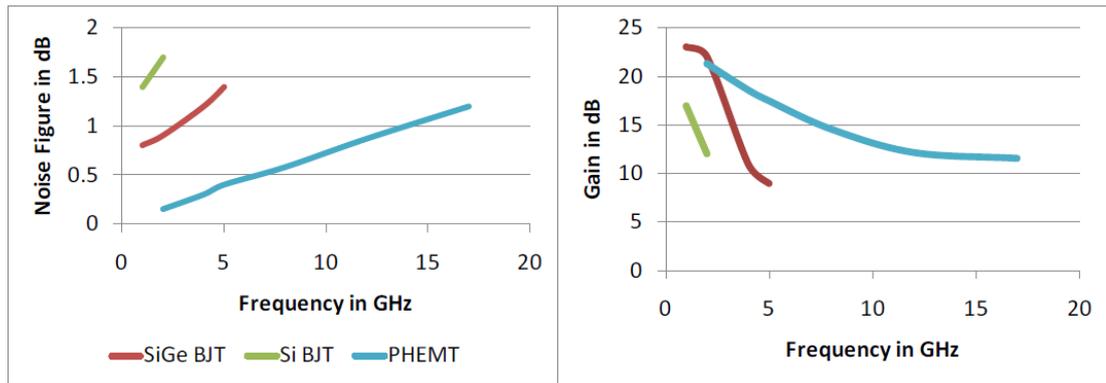


Fig. 1.3: Relative merits of the commercially available low noise transistors.

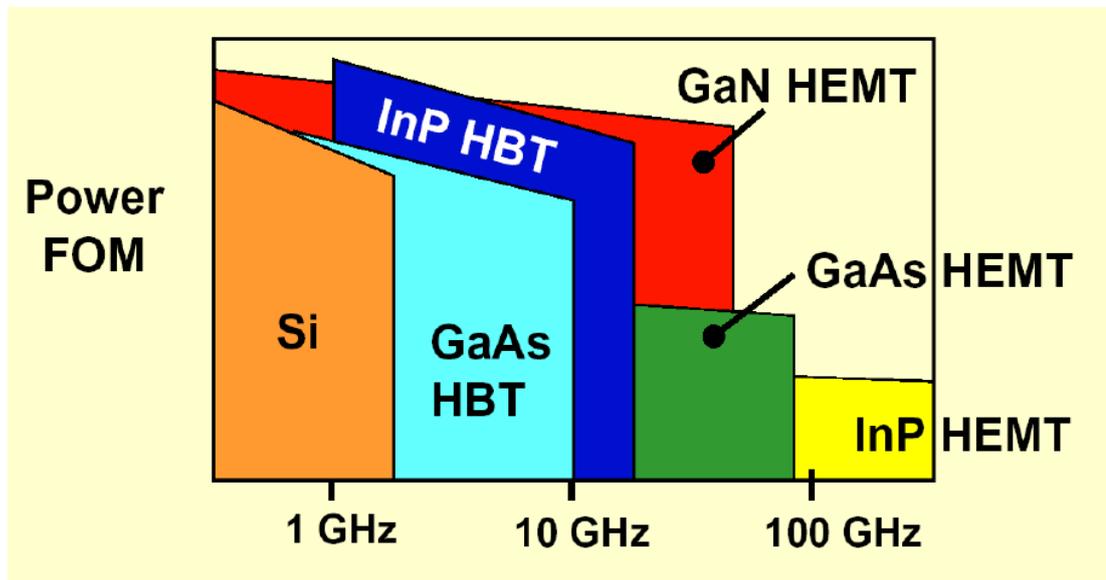


Fig. 1.4: Relative merits of power transistors technologies [7].

Due to this, antenna designers are determined to develop antennas that are physically compatible and fit within a given limited space where electrically small antennas are required to be a constituent part within handheld wireless devices. As a consequence to this, modern integrated circuit (IC) devices that are made from a single dielectric slab of semiconductor, called Monolithic Microwave Integrated Circuits (MMIC) have been developed [7]. The works on cascading of sub-circuits

within MMIC does not require an external matching networks and hence, making this technology easier to use. However, the ideas on compactness using MMIC technologies for such high level integration have been realised with much higher cost and there is always a trade-off for the overall system performance. This is a typical drawback when integrating an electrically small antenna into a system on-chip; it will suffer from poor gain, efficiency and bandwidth due to its relatively small radiation aperture size [8]. Therefore, a reasonably small off-chip or externally built antenna as proposed by Chan et al [9] is a viable option to be fed differentially and without having direct electrical connection using bond wires or vias through an MMIC.

Song et al [10] proposed to fix the antenna position on the chip carrier, and this has slightly improved the antenna performance. The overall systems performance was still inferior standard during low operating frequencies. The concept proposed by Song et al [10] was to electromagnetically couple the energy from the chip through the parasitic patch to the antenna. However, the chip carrier where the antenna was to be situated is usually designed based on the chip's size which is quite small. This has caused the overall systems to suffer from the poor performance especially at lower microwave frequency band. Neglecting the chip's size, a larger chip carrier space should be reserved for the antenna to reside in a particular state and this will increase the total cost to build one within a package. For this reason, a feasible technique that has a potential to overcome this limitation was proposed by Chan et al [9]. A greater advantage arises from the compatibility with a differential feeding technique to generate two signals to feed the two-port networks made up of exactly similar parts facing each other. In addition, this kind of feeding

technique is more desirable and suitable for IC realisation as seen in the Figs. 1.1 and 1.2, unlike most traditional antenna architectures which are generally one-port networks. This technique will create a null reaction to the crosstalk over common bias lines resulting from the two signals that flow in the opposite direction along the differential lines [11]. Simultaneously, it can enhance the circuit attributes in terms of immunity towards common mode interference.

Furthermore, differentially fed antenna designs will no longer require a balun such as hybrid coupler or impedance transformer within the front-end architecture as differential signals are preferable and can be directly fed into an IC [2]. In other words, this type of antenna not only radiates signal but it also behaves like a good matching circuit and a lossless coupler [3, 12]. However, there are always restrictions when employing new techniques into a system. For example, the physical geometry of a differentially fed antenna configuration should be in a symmetrical form. Besides, optimisations are still required within the circuit configurations such as additional open-circuit stubs etc.

In contrast, a traditional one-port antenna uses a balun as a platform for converting an unbalanced signal into an equivalent of balance signal before feeding into an IC [13-14]. The Balun is actually an electrical device that can cause a problem in the system performance. As shown in Fig. 2.4 (page 21), the balanced signals which are coming out from the balanced ports (Port 2 & 3) ideally are equal in their amplitudes and 180° out-of-phase. For a real balun, numerous reasons can cause a deviation from ideal conditions, and the balanced signals from a balun will

not be perfectly differential. This deviation is known as the balun's imbalance which is quantified as follows.

$$\textit{Amplitude Imbalance} = |S_{21}|(dB) - |S_{31}|(dB) \quad (1.1)$$

$$\textit{Phase Imbalance} = 180^\circ - |\angle(S_{21}) - \angle(S_{31})| \quad (1.2)$$

The balun's imbalance will increase the total system loss as this will cause even the symmetrical balanced ports become imbalanced which renders this device unusable within our push-pull PA configuration. Therefore, when it is still being used within the circuit configuration, it will result in poor efficiency. Moreover, the system using a balun within the configuration is not suitable for IC realisation and does not comply with the requirement of fully integrated solutions anyway.

Therefore, a novel technique for the direct integration of power amplifiers and antennas is to be investigated. Since the push-pull amplifier configuration uses the differential feeding technique, an EM structure like a typical two-port aperture coupled microstrip antenna is designed and it will be differentially fed at both ports so that it can be incorporated at the output stage within a push-pull amplifier architecture. Consequently, it can offer advantages of tight, neat and high level integration of a push-pull transmitting amplifier. Besides, an objective of this research is to minimise the losses by eliminating lossy devices like baluns or hybrid couplers within the existing configurations as can be seen in Fig. 1.1. Besides, incorporating an optimum matching network in the front-end circuit to ensure the maximum power transfer and minimise signal reflection from the load, is another goal of this research work. In the case of an amplifier that is part of a subsystem

circuit, the mode of operation is one of the important considerations in order to generate differential signals. Thus, the main objectives of this research work are the following:

- To investigate the feasibility of integrating the power transistor output matching network into the differential feed network of an aperture coupled antenna.
- To establish a novel technique for direct integration of push-pull power amplifiers and antennas by removing the lossy output balun within the configuration.
- To demonstrate the feasibility of this novel technique by applying it to fully integrated antenna–amplifier front-end solutions.

1.3 Thesis Organisation

A brief overview of wireless communications and an insight into the motivation behind this thesis has been presented in chapter 1. Chapter 2 presents the background and overview on microwave theory, conventional power amplifier classes and early innovations and developments that include the evolution of integrated circuit antennas, passive antennas and their feeding techniques. The most important part is about push-pull integrated antenna front-end in which differential feeding technique is employed on an unbalanced antenna so that the unbalanced antenna will behave like a balanced fed one.

Chapter 3 explains in brief, the history of push-pull amplifiers as well as their design architecture. Besides, two research design flow charts are included that will cover two different designs, which are: push-pull Class B power amplifier and EM structure; and aperture coupled patch antenna. An investigation into the effect of higher order harmonic filtering in a push-pull configuration is also presented in this chapter.

Chapter 4 presents in detail the differential aperture coupling technique for a push-pull transmitting amplifier. It starts with the concept of a single fed aperture coupled antenna to show how maximum current is effectively being created and electromagnetically coupled to a microstrip patch antenna through a slot/aperture. This is followed by descriptions of the two types of differentially fed aperture coupled passive antennas named Structure A and Structure B respectively. The chapter includes some simulated and measured results to support the proposed design theory. Furthermore, the parametric studies on the available design variables for two different slot/aperture designs are presented in this chapter as well.

Chapter 5 describes the direct integration of a push-pull amplifier and an aperture coupled antenna. It starts with the simulation of a push-pull transmitting amplifier, followed by its transformation into a fully integrated version using real lossy components such as optimised biasing and decoupling circuits and a Wilkinson power divider. Comparison of waveforms of the two versions has been achieved through simulation. The difference in the measured received power from both passive and active structures is also presented in this chapter.

Chapter 6 summarizes the work which has been carried out in this thesis. It concludes that the proposed technique is very useful for direct integration of amplifiers and antennas by effectively incorporating the output matching functions and power combiner of a push-pull amplifier into the two-port antenna structure.

CHAPTER 2

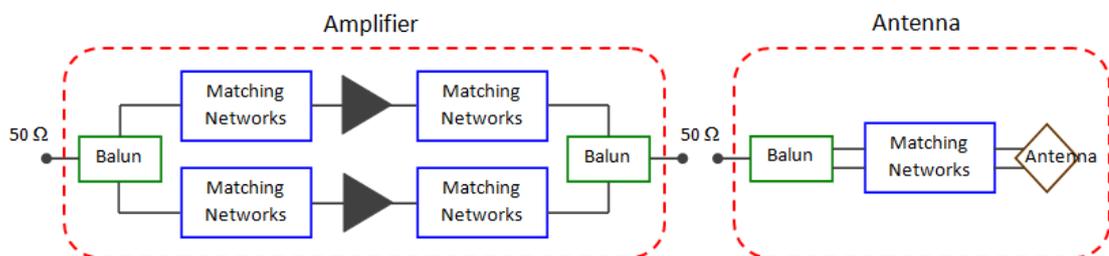
LITERATURE REVIEW

2.1 Overview

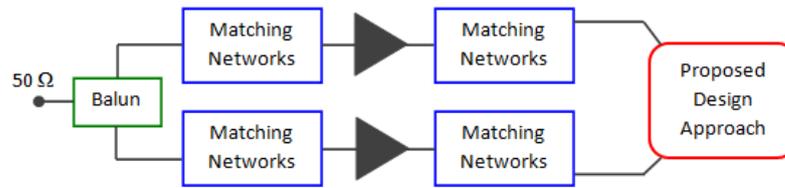
The 50Ω impedance interface is a very popular among RF and microwave engineers and researchers. Every constituent part within the front-end systems which include active devices as well as passive structures from the amplifiers, attenuators, antennas and so on to network analyser have all been designed and developed particularly to comply with the standard 50Ω environment without significant impedance mismatches. This unique advantage of universal connectability also has some drawbacks. For example in a Case A amplifier, where two devices are required to drive into an optimum impedance of real 20Ω . According to present conventional standards, that 20Ω impedance needs to be transformed into 50Ω environment. As a consequence, losses in the transforming circuit and limitations on the achievable bandwidth are unavoidable. However, Case B is where in general, the impedance has a complex value; this means that loads generally have a resistance component (symbol: R) which forms the real part of Z and a reactance (symbol: X) which forms the imaginary part of Z . In most cases, especially those involving power transmission at low frequency, the reactance may be negligible or zero. Therefore, impedance can be considered as a pure resistance, expressed as a real number. On the

other hand, this will become more significant in determining the overall system performance when it comes to impedance matching at higher frequency that involves a complex value of impedance requirement. All resistance and reactance components respectively are required to be taken into considerations when integrating an amplifier-antenna within the front-end systems. Another aspect of the 50Ω measurement interface is that there is only one signal connection and one ground connection. If a half wave dipole antenna, which has a balance feed is going to be connected to the standardised unbalanced interface, there is a need for a network in between to convert from signal-ground to signal-signal, a so called balun. Similarly with Push-pull topology, baluns are required at both input and output side respectively since it is using differential feeding technique.

The aim of this work is mainly to make a search and systematic inquiry into whether replacing the unbalanced 50Ω interface could be advantageous compared to that regularly used design procedure when designing an amplifier-antenna system. As represented in Fig. 2.1, it is obvious physically as well as electrically that the proposed design approach would produce a less complex front-end system than the conventional way.



(a) Conventional amplifier-antenna front-end system.



(b) The proposed design topology.

Fig. 2.1: The potential advantages of integrating an amplifier-antenna system.

This chapter will outline the theory behind conventional power amplifier design, illustrating the differences between different classes of operation. An ideal transistor model will be used to explain a simplified design methodology showing how the bias voltage and load termination affects the amplifier performance. Furthermore, the role of baluns in a Push-pull Amplifier and how their concept can be adapted by the proposed structure is briefly overviewed. The basics of microwave theory as well as a brief overview about active integrated circuit antennas is followed by a review of passive antenna concepts and their feeding methods, which are presented to assist in understanding the research work in this thesis.

2.2 Microwave Theory

In this section, the theory used to justify the different design goals and techniques is described. First of all, some general microwave theory will be dealt with, followed by the two sections concerning the theory of amplifiers and antennas that are of interest in the remainder of the thesis. Special importance is given to some basic concepts of microwave theory that are of significant interest to this thesis. The

concepts which will be mentioned in the following sub-section are inspired by the book of Pozar [15].

2.2.1 S-parameters

Scattering parameters are commonly known as S-parameters. These parameters are generally being used as a very useful tool within microwave theory especially for practical purposes. Basically, the S-parameters are represented as the elements in the matrix $N \times N$ form where N is the integer. The matrix describes the linear relationship between incident and reflected voltage wave on the N -port networks. This mutual relationship can be written as:

$$\begin{pmatrix} b_1 \\ \vdots \\ b_N \end{pmatrix} = \begin{pmatrix} S_{11} & \cdots & S_{1N} \\ \vdots & \ddots & \vdots \\ S_{N1} & \cdots & S_{NN} \end{pmatrix} \begin{pmatrix} a_1 \\ \vdots \\ a_N \end{pmatrix} \quad (2.1)$$

Where a_N and b_N are incident and reflected voltage waves at the N -th port respectively. The case when $N = 2$ refers to the very common 2-port networks and it can be seen in Figure 2.2. Incident waves are represented by a_1 and a_2 . In the same manner, the outgoing waves are represented by b_1 and b_2 .



Fig. 2.2: The common 2-port networks.

The expression in 2.1 is then reduced to:

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix} \quad (2.2)$$

Where S_{11} and S_{22} are the coefficients describing the reflection at the ports. S_{12} and S_{21} are the coefficients describing the gain between the ports in both directions.

2.2.2 Mismatch

High frequency signals reflect at the boundary between two impedances. In reality, this reflection is mostly undesirable since it will result in power loss when part of the signal is reflected to the source. The reflection between two impedances is expressed by the coefficient, Γ_L

$$\Gamma_L = \frac{V_-}{V_+} = \frac{Z_L - Z_o}{Z_L + Z_o} \quad (2.3)$$

Where V_+ and V_- are the phasor of the in- and outgoing wave respectively. The impedance Z_L is the load impedance and Z_o is the standard 50Ω impedance according to Figure 2.3. The arrow points towards the impedance that is considered as load.

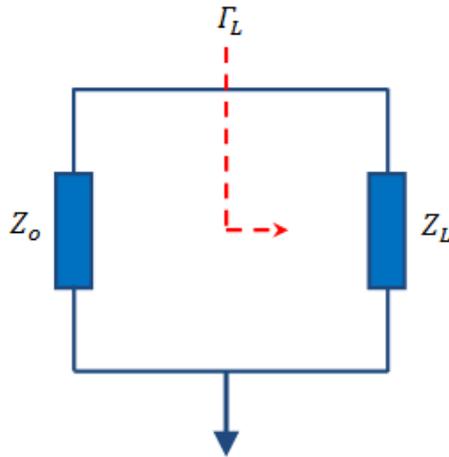


Fig. 2.3: Γ_L marked in the boundary between two impedances.

An alternative way which is frequently used to quantify mismatch is the *Standing Wave Ratio*, SWR. A standing wave occurs when the ingoing wave and the reflected wave are added before the mismatch and the ratio is taken from the highest and lowest amplitude of the total wave pattern.

The maximum amplitude of the standing wave will occur at the position where the waves are added constructively and the resulting amplitude is $V_{max} = |V_+| + |V_-|$. Meanwhile, the minimum of the standard wave will occur at the position where the two waves are added destructively which will correspond to an

amplitude of $V_{min} = |V_+| - |V_-|$ for a passive load. Then, the SWR is computed from the ratio of V_{max} to V_{min} .

$$SWR = \frac{|V_+| + |V_-|}{|V_+| - |V_-|} = \frac{|V_+|(1 + |\Gamma_L|)}{|V_+|(1 - |\Gamma_L|)} = \frac{1 + |\Gamma_L|}{1 - |\Gamma_L|} \quad (2.4)$$

2.2.3 Transmission Lines

The purpose of transmission lines is to transfer signals over a distance. Different types of transmission lines have been used and realised in different ways especially when it comes to high frequency applications. Theoretically, a transmission line is characterised by its characteristic impedance, Z_c which depends on the physical dimensions of the transmission line. In this subsection, a microstrip type of transmission line is reviewed. Microstrip is seen as the technically more flexible alternative since it can be realised in different shapes depending on the applications. Therefore it is used to transfer signals between devices.

2.2.3.1 Microstrip

Microstrip lines are widely used as transmission paths in all kinds of high frequency circuits. A microstrip consists of a conductor and a ground plane which are separated by a dielectric medium of a certain thickness (h). The wavelength of a wave travelling through the microstrip for a given frequency is dependent on the relative permittivity, ϵ_r of the substrate. High relative permittivity of a substrate will

give a short physical wavelength. The geometry of a microstrip transmission line width, w , is shown in Fig. 2.4.

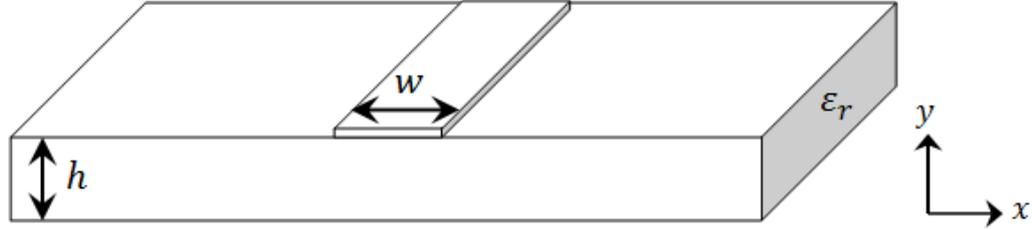


Fig. 2.4: Microstrip transmission line geometry.

The effective dielectric constant of a microstrip line is given approximately by

$$\epsilon_{eff} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} \left(\frac{1}{\sqrt{1 + 12h/w}} \right) \quad (2.4)$$

Given the dimension of microstrip transmission line, the characteristic impedance can be expressed as

$$Z_o = \begin{cases} \frac{60}{\sqrt{\epsilon_{eff}}} \ln \left(\frac{8h}{w} + \frac{w}{4h} \right) & \text{for } w/h \leq 1 \\ \frac{120\pi}{\sqrt{\epsilon_{eff}} [w/h + 1.393 + 0.667 \ln(w/h + 1.444)]} & \text{for } w/h \geq 1 \end{cases} \quad (2.5)$$

The following is the w/h ratio that can be estimated when characteristic impedance, Z_o , and dielectric constant, ϵ_r , are known.

$$\frac{w}{h} = \begin{cases} \frac{8e^A}{e^{2A} - 2} & , \frac{w}{h} < 2 \\ \frac{2}{\pi} \left[B - 1 - \ln(2B - 1) + \frac{\epsilon_r - 1}{2\epsilon_r} \left\{ \ln(B - 1) + 0.39 - \frac{0.61}{\epsilon_r} \right\} \right] & , \frac{w}{h} > 2 \end{cases} \quad (2.6)$$

Where

$$A = \frac{Z_o}{60} \sqrt{\frac{\epsilon_r + 1}{2}} + \frac{\epsilon_r - 1}{\epsilon_r + 1} \left(0.23 + \frac{0.11}{\epsilon_r} \right)$$

$$B = \frac{377\pi}{2Z_o\sqrt{\epsilon_r}}$$

On the other hand, microstrip structures can be used to replace lumped components like inductors and capacitors. The length of a transmission line is often specified by the electrical length, θ which is an angle corresponding to a phase at given angular frequency, ω :

$$\theta = \beta l = \frac{2\pi}{\lambda} l = \frac{\omega}{v_p} l \quad (2.7)$$

Where v_p is the velocity of propagation defined as $c/\sqrt{\epsilon_{eff}}$, λ is the corresponding wavelength, β is the propagation constant defined as $k_o\sqrt{\epsilon_{eff}}$ and k_o is a wavenumber defined as $2\pi/\lambda$. A general expression for the input impedance of a transmission line with the electrical length, θ , characteristic impedance, Z_o , and loaded with Z_L is

$$Z_{in} = Z_o \frac{Z_L + jZ_o \tan \theta}{Z_o + jZ_L \tan \theta} \quad (2.8)$$

As for a shorted piece of transmission line ($Z_L = 0$), the expression is

$$Z_{in} = jZ_o \tan \theta \quad (2.9)$$

which can be compared with the reactance of an inductor

$$Z_{ind} = j\omega L = jX_{ind} \quad (2.10)$$

Combining (2.9) and (2.10), the following expression for X_{ind} can be derived:

$$X_{ind} = Z_o \tan \theta \quad (2.11)$$

For small value of the electrical length, $\tan \theta \approx \theta$. Combining (2.11) and (2.7), the expression for the X_{ind} can be written as:

$$X_{ind} = Z_o \theta = Z_o \frac{\omega l}{v_p} \quad (2.12)$$

which shows that the reactance X_{ind} of a narrow transmission line is proportional to the frequency and length. Hence, the inductance is given by:

$$L = Z_o \frac{l}{v_p} \quad (2.13)$$

In the same way, the reactance X_{cap} of an open stub can be derived using (2.8) having $Z_L = \infty$, which leads to the expression

$$X_{cap} = -Z_o \cot \theta \quad (2.14)$$

And for small value of θ , the approximate value of the resulting capacitance is

$$C = \frac{l}{Z_o v_p} \quad (2.15)$$

Summing up, the inductor is realised by a narrow piece microstrip (high Z_o) and the inductance is proportional to the length. According to (2.15), a large capacitance is achieved by having a long piece of stub with a low characteristic impedance Z_o . Low characteristic impedance corresponds to a wide conductor. Note that approximation of having $\tan \theta \approx \theta$, should always be considered and is only valid for any small values of θ .

2.2.4 Balun Theory

“A balun is a network for the transformation from an unbalanced transmission line, system or device to a balanced line, system or device. Baluns are also used for impedance transformation. The term balun is derived from balanced to unbalanced” [16]. Baluns are used for antenna feeds, inputs to differential circuits,

anti-phase power combiners, transformers between transmission line types etc. The definition of a balun varies based on its use as it is more of a generic description that can take several forms in practice. For instance, an amplifier that takes a single ended input and outputs a differential signal can be referred to as an active balun. This and other known structures such as 180° hybrid and a voltage transformer can be employed as passive balun.

2.2.4.1 Ideal Balun

The ideal balun model is defined based on the application. As has been pointed out, a balun can take several forms. In this thesis, an ideal balun will be thought of as an ideal three ports transformer as shown in Figure 2.4.

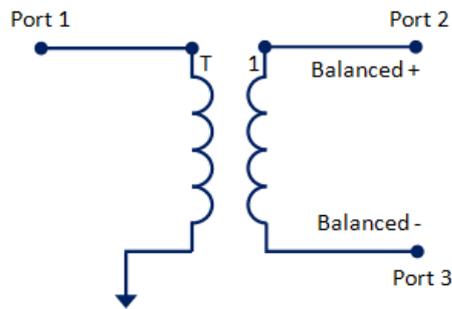


Fig. 2.4: The ideal transformer employed as an ideal balun.

The Scattering matrix parameters (S-parameters) for the ideal transformer balun are given by [17]

$$S = \begin{bmatrix} \frac{1 - 2T^2}{1 + 2T^2} & \frac{2T}{1 + 2T^2} & \frac{-2T}{1 + 2T^2} \\ \frac{2T}{1 + 2T^2} & \frac{1}{1 + 2T^2} & \frac{2T^2}{1 + 2T^2} \\ \frac{-2T}{1 + 2T^2} & \frac{2T^2}{1 + 2T^2} & \frac{1}{1 + 2T^2} \end{bmatrix} \quad (2.16)$$

For consistency during analysis, the transformation ratio T of the transformer for the ideal balun model adopted in this work is:

$$T = \frac{1}{\sqrt{2}} \quad (2.17)$$

As for this value of T , the balun will be matched at Port 1 and the balun will be acting as an anti-phase power splitter for 50Ω reference impedance at all ports.

$$S = \begin{bmatrix} 0 & \frac{1}{\sqrt{2}} & \frac{-1}{\sqrt{2}} \\ \frac{1}{\sqrt{2}} & \frac{1}{2} & \frac{1}{2} \\ \frac{-1}{\sqrt{2}} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \quad (2.18)$$

According to microwave theory, it is impossible to have a lossless, matched as well as reciprocal three-port device. Since the ideal balun is lossless and reciprocal then, it must be unmatched at all or some of the ports. It can be seen that Ports 2 and

3 respectively are unmatched and un-isolated. However, under certain conditions these ports can behave as matched ports. In order to understand how a balun operates, first it is important to look at two operating modes which are the odd and even mode of operation. Balun act as anti-phase power combiners, hence when operating in odd-mode, the balun combines the power coming from Port 2 and 3 and output them at Port 1 as shown in Figure 2.5. In this case, Ports 2 and 3 appear to be matched since no power is reflected back from these terminals. The impedance seen by terminal 2 and 3 in this mode is given by (2.19) and it is a function of the transformation ratio.

$$Z_{odd} = \frac{Z_o}{2T^2} = Z_o \quad (2.19)$$

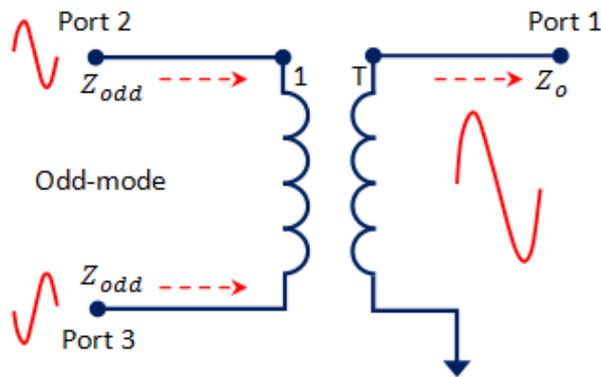


Fig. 2.5: Odd-mode behaviour of an ideal transformer-based balun.

When the balun is operating under even-mode conditions, the power is completely reflected from Port 2 and 3. As a result, the impedance seen at Ports 2 and 3 are open circuit and Port 1 produces no output.

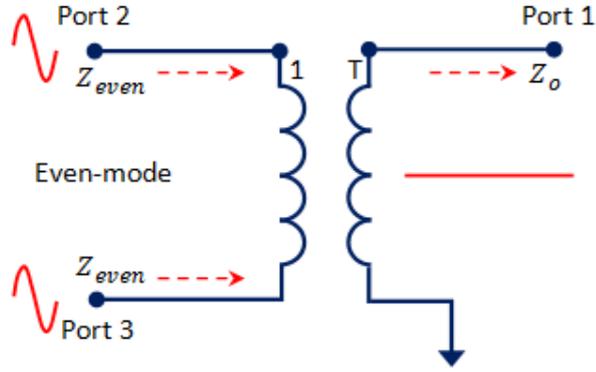


Fig. 2.6: Even-mode behaviour of an ideal transformer-based balun.

A more general formulation which describes the reflection coefficient at the balanced ports in each mode when the unbalanced port is terminated by the characteristic impedance Z_o is given by:

$$S_{Odd} = \frac{1}{2}[S_{22} - S_{23} - S_{32} + S_{33}] \quad (2.20)$$

$$S_{Even} = \frac{1}{2}[S_{22} + S_{23} + S_{32} + S_{33}] \quad (2.21)$$

2.2.4.2 Balun Categories

Baluns can be classified into three main categories. There are known as current balun, voltage Balun and the other one is a balun which does not fall into either mentioned categories [18].

A current balun is characterised by its feature regarded as always having a balanced current at the two output terminals regardless of the loads terminating ports

2 and 3. The ideal transformer that has been employed as an ideal balun as shown in Fig. 2.4, is the best way of illustrating this kind of balun. The low frequency Guanella and coaxial Marchand are another two examples that share the same attributes as Current balun.

Similarly, a voltage balun is characterised by its feature of maintaining balanced voltages at both terminals regardless of the loads connected to them. The ideal transformer with the secondary winding grounded in the centre is a good example to illustrate this type of balun. It is shown in Fig. 2.7.

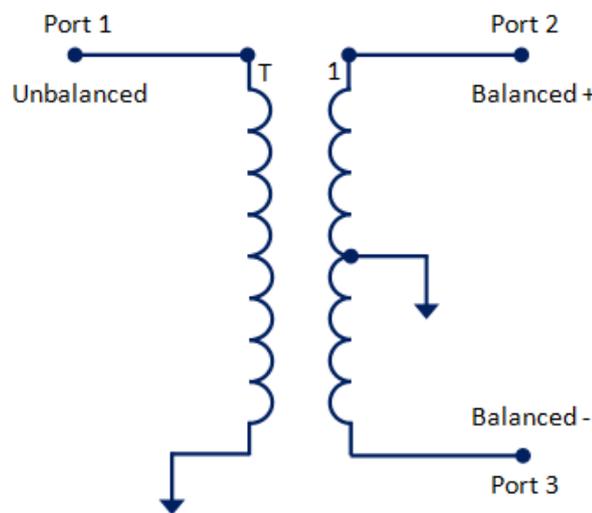


Fig. 2.7: The voltage balun based on ideal transformer with grounded center tap.

According to McLean in [18], a 180° Power Divider belongs to the third category of baluns. This type of balun is known to “fix a linear combination of voltage and current of the two output ports to be equal in magnitude and opposite in phase”. A 180° hybrid coupler with the isolated port which is connected to a matched

load is an appropriate example to demonstrate this third type of balun. Fig. 2.8 shows the illustration of 180° hybrid coupler being employed as a balun.

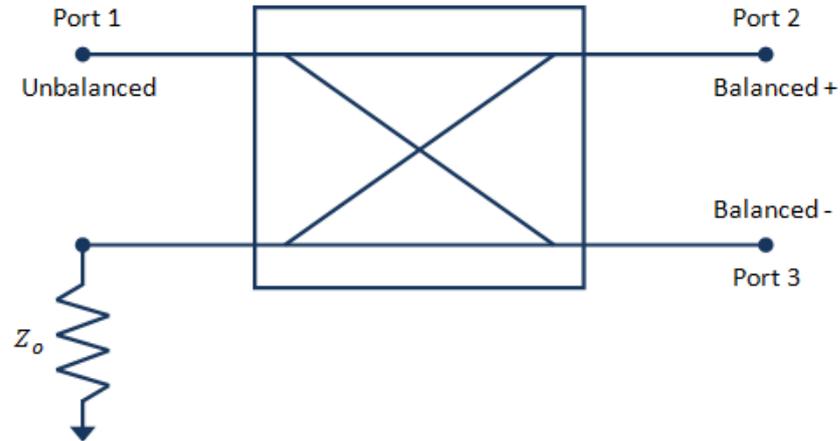


Fig. 2.8: 180° hybrid coupler employed as a balun.

In this thesis, most of the focus will be on this category of baluns as it was found that at RF frequencies, it could be a voltage Balun at one frequency and current Balun at another frequency while at most of the other frequencies its behaviour falls under the third category. In spite of the unique behaviour of the 180° hybrid coupler, physically it is simple and robust and practically it is easy to build as well as low profile. It is used in this work only at the input stage of Push-pull layout, because the purpose of the work is to investigate replacing the output balun with an integrated antenna structure.

2.3 Ideal Transistor Model

In this section, an ideal transistor model is used to illustrate the various power amplifier classes. Fig. 2.9 shows an ideal transistor model which comprises a voltage control current source (VCCS) with V_{gs} as the input voltage and I_{ds} as the output current. The current source operates linearly with input voltage levels above the pinch-off voltage V_p and below the saturation voltage V_{sat} as shown in Fig. 2.10(a). Besides, the Drain terminal requires a positive bias voltage which is at least slightly higher than transistor's knee voltage V_k and well below its breakdown voltage V_b respectively. The response of DC-IV characteristics are shown in Fig. 2.10(b).

The following analysis has been simplified and assumed as parasitic elements of the transistor are not included. This assumption is actually supporting the context of making clear the basic principle of various amplifier classes. As for remarks, the DC and RF or AC components of voltages and currents are recognised by different terms as well as signs. A capital letter subscript with an average bar over the term and a small letter subscript with no average bar will be a sign for DC and RF components respectively. Meanwhile, the term which use capital letter subscripts with no average bar will indicate the total signals.

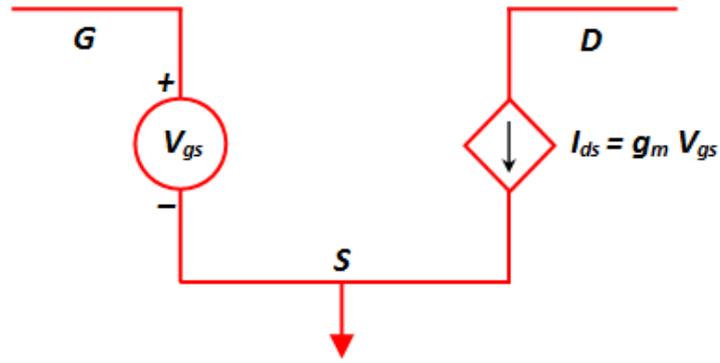


Fig. 2.9: Ideal field-effect transistor (FET) model.

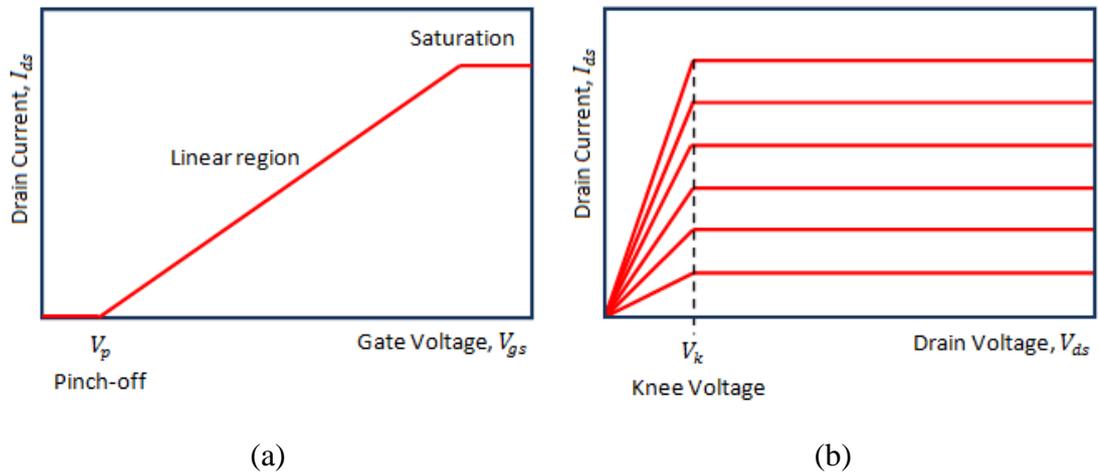


Fig. 2.10: The characteristics of ideal transistor model. (a) V_{gs} to I_{ds} transfer characteristic (b) I_{ds} vs V_{ds} for varying V_{gs}

2.4 Conventional Power Amplifier Classes

Power amplifiers can be classified into different categories. According to Cripps [19], RF power amplifiers are commonly being classified and described as Class A, AB, B or C in terms of the conduction angle as well as their trade-off

between linearity and maximum achievable efficiency. This section discusses four different classes of conventional radio frequency power amplifier operation which are predominantly used in most applications for wireless communication systems. Fig. 2.11 shows the typical classes based on the transistor transfer characteristics while Table 2.1 lists the maximum possible efficiencies respectively.

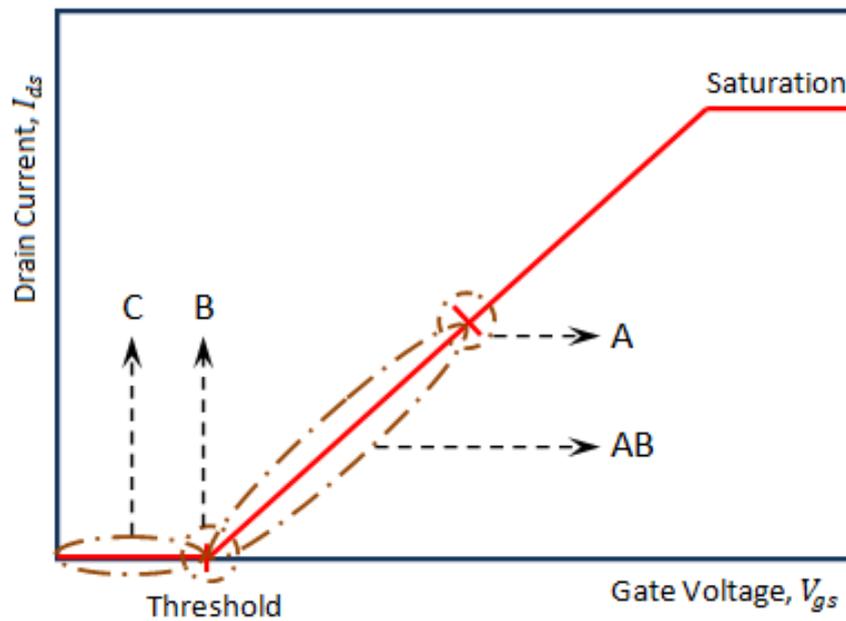


Fig. 2.11: Classes of operation of Power Amplifier based on transfer characteristic.

Table 2.1: Classification of different classes of operation for conventional RF Power Amplifier.

Classification	A	AB	B	C
Conduction Angle, θ (radian)	2π	$\pi < \theta < 2\pi$	π	$\theta < \pi$
Peak Achievable Efficiency (%)	50	50 – 78.5	78.5	≈ 100
Maximum Peak-to-Peak Output (V)	$\gg V_{cc}$	$\approx V_{cc}$	$< V_{cc}$	$\ll V_{cc}$
Distortion	Small	Small to moderate	moderate	Large
Linearity	Most linear	Slightly non-linear	Non-linear	Highly non-linear

2.4.1 Class A

Class A is the simplest class of operation of power amplifiers and it usually used as a benchmark for other classes. Class A is biased with a Gate voltage in the middle of the region between the pinch-off and saturation such that the DC component of I_{DS} denoted by $\overline{I_{DS}}$ is half of the maximum current provided by the transistor. On the other hand, the Drain DC voltage is set as the average of the knee voltage and breakdown voltage. In general, the input voltage is allowed to swing strictly between the pinch-off voltage and saturation voltage while the output voltage is allowed to swing between the knee voltage and breakdown voltage. The maximum power is achieved by aligning the maximum swing at the input and the maximum swing at the output using the proper output resistance denoted as R_{opt} [19]. Fig. 2.12 shows the relationship between input and output voltages.

The slope of the load-line is set by the load impedance and for maximum output power the value of the load impedance R_{opt} is given by:

$$R_{opt} = \frac{V_{max}}{I_{max}} = \frac{2\overline{V_{DS}}}{2\overline{I_{DS}}} = \frac{\overline{V_{DS}}}{\overline{I_{DS}}} \quad (2.22)$$

As for this case the output power will be,

$$P_{out_{max}} = \frac{1}{2}\overline{V_{DS}} \times \overline{I_{DS}} = \frac{1}{8} V_{max} \times I_{max} \quad (2.23)$$

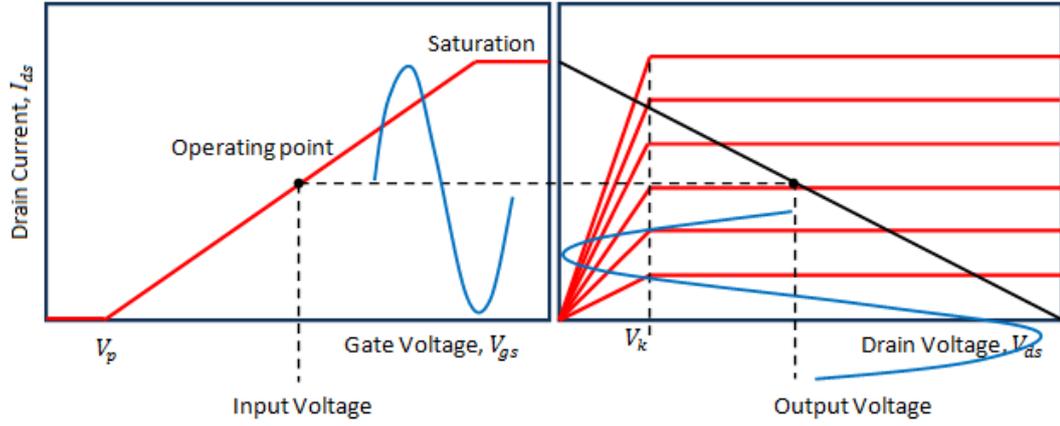


Fig. 2.12: The relationship between input and output waveforms of Class A power amplifiers.

Efficiency is one of the significant considerations that have usually been taken into account when designing power amplifiers. The quality of being efficient depends on the useful converted RF power from DC power performed by power amplifier. In other words, the power amplifier should be working productively with minimum wasted DC power into the form of heat. It is frequently being measured as the ratio between RF output power and DC input power. The Drain Efficiency (η) and Power Added Efficiency (PAE) are two popular terms used to define the power amplifier's efficiency. These two terms are closely related to each other in such a way η is normally greater than PAE because PAE takes the RF input power into account. Equations (2.24) and (2.25) respectively will illustrate these two measures.

$$\eta = \frac{[P_{out}]_{RF}}{[P_{in}]_{DC}} \times 100\% \quad (2.24)$$

$$PAE = \frac{[P_{out}]_{RF} - [P_{in}]_{RF}}{[P_{in}]_{DC}} \times 100\% \quad (2.25)$$

In the case of Class A operation, the maximum efficiency happens at maximum output power. This figure is calculated as follows,

$$\eta = \frac{[P_{out}]_{RF}}{[P_{in}]_{DC}} \times 100\% = \frac{\frac{1}{2}\overline{V_{DS}} \times \overline{I_{DS}}}{\overline{V_{DS}} \times \overline{I_{DS}}} \times 100\% = 50\% \quad (2.26)$$

Theoretically, the maximum achievable efficiency for Class A is only 50%. However, it can provide the best linearity among those existing class of operations. This work focuses on the best compromise between efficiency and linearity, and hence Class A is not suitable to be used in high efficiency applications. The way in which fundamental input power and fundamental output power are related will define the linearity of power amplifiers. Ideally, intermodulation products do not exist in the power amplifiers that are 100% linear. However, small nonlinearities still occur and distortion products remain in practice. Therefore, the term “linear” is just relative to the application requirements as it is usually being defined by certain standards. In spite of the efficiency, power amplifiers with Class A operation still is being used in some applications where the excellent signal quality is extremely vital, like in the preamplifiers as well as in some military applications for instance [19].

2.4.2 Class B

Basically, all Class B power amplifiers are biased with a voltage at pinch-off in such a way that the transistor is not dissipating any power in the absence of an input signal which means $\overline{I_{DS}}$ is equal to zero. By contrast, Class A power amplifiers

are biased at the operating point between pinch-off and saturation resulting in the DC current flow and dissipation for nothing even if there is no input voltage. As with Class A power amplifiers, the Drain voltage $\overline{V_{DS}}$ for Class B of operation is between the knee voltage V_k and breakdown voltage V_b . Although the load-line for a Class B power amplifier is different than that of Class A, however, it is still capable of producing the same maximum output power. Fig. 2.13 shows the relationship between input and output signals.

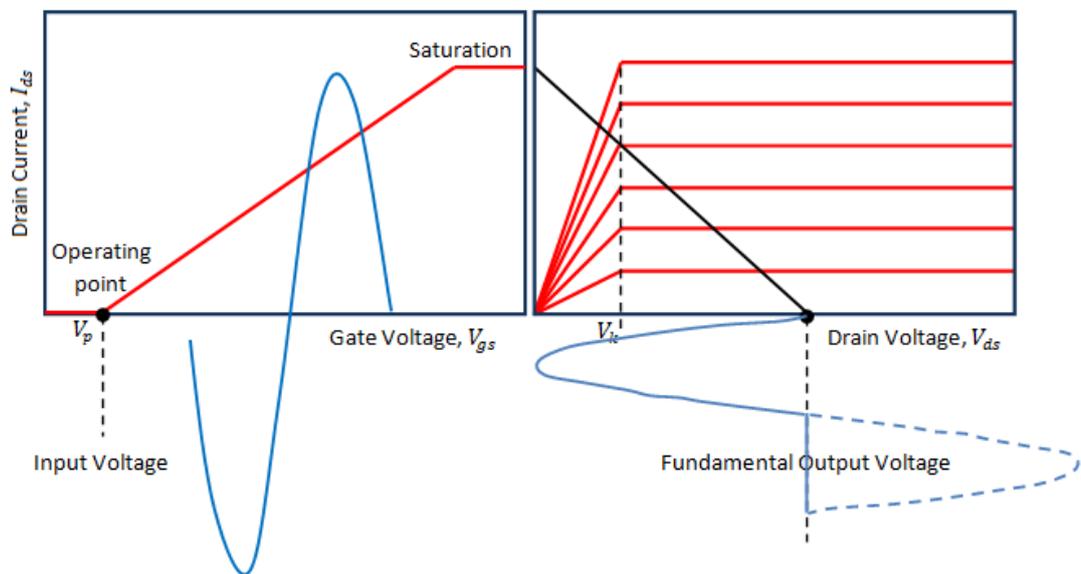


Fig. 2.13: The relationship between input and output waveforms of Class B power amplifier.

Even though a Class B power amplifier might produce the same maximum output power as Class A, however, the way it is being driven is different. A Class B power amplifier requires such input power four times higher than in Class A in order to get the same output. Due to that, the power gain of Class B power amplifiers is only one quarter of that Class A power amplifiers. Note that the power gain (G) of a power amplifier is as follows,

$$G = \frac{[P_{out}]_{RF}}{[P_{in}]_{RF}} \quad (2.27)$$

When designing power amplifiers especially in Class B working condition, the maximum output power at the fundamental frequency is desired to be achieved. In order to do that, it is important to ensure higher order harmonics are properly being shorted out so that input voltage swings at its maximum over the fundamental frequency to produce such high power at the output. However, these shorting harmonics will slightly give effects on the bandwidth limitations but it is not too severe since the main aim is for getting maximum output power at fundamental frequency.

Fourier series expansion is used to derive the DC, fundamental and harmonics contents in a Drain current I_{DS} waveform. By applying a Fourier transform to the half sinusoid, the equation will be as follows:

$$\overline{I_{DS}} = \frac{1}{2\pi} \int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} I_{max} [\cos(\theta)] d\theta \quad (2.28)$$

$$I_{ds_n} = \frac{1}{\pi} \int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} I_{max} [\cos(\theta)] \cos(n\theta) d\theta \quad (2.29)$$

Where, I_{ds_n} will be a term for amplitude of the current of n -th harmonic. Note that the signal is assumed to be symmetric around the y -axis. Hence, it does not

contain any sine terms and it genuinely consists of cosine terms provided that the signal function is even. If the signal function was not even then an additional term is required to describe the signal correctly. Thus, the DC component can be written in terms of I_{max} as,

$$\overline{I_{DS}} = \frac{1}{2\pi} \int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} I_{max} [\cos(\theta)] d\theta = \frac{I_{max}}{\pi} \quad (2.30)$$

While the amplitude of the fundamental ($n = 1$) can written as,

$$I_{ds1} = \frac{1}{\pi} \int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} I_{max} [\cos(\theta)] \cos(\theta) d\theta = \frac{I_{max}}{2} \quad (2.31)$$

The efficiency of a Class B power amplifier is calculated by substituting the terms I_{max} and V_{max} as follows:

$$\eta = \frac{[P_{out}]_{RF}}{[P_{in}]_{DC}} \times 100\% = \frac{\frac{1}{2} \frac{V_{max}}{2} \times \frac{I_{max}}{2}}{\frac{V_{max}}{2} \times \frac{I_{max}}{2}} \times 100\% = \frac{\pi}{4} \times 100\% \cong 78.5\% \quad (2.32)$$

The truth of a statement that Class B power amplifiers are considered as linear in terms of the input and output power levels have been denied by other claims which can be found from the literature. The previous section has stressed that the linearity of power amplifier is not just based on the voltage and current waveforms but it is actually based on the relationship between input and output power levels at

fundamental frequency. Even though Class B operation produces harmonic content due to the fact that the current is half a sinusoid, it does not produce any intermodulation products unless the amplifier saturates and enters the knee region. However, in practice, the non-idealities often exist within the transistor circuitry such as soft turn-on voltage and non-linear g_m which causes the power amplifier to behave non-linearly.

2.4.3 Class AB

It has been mentioned in the earlier section, ideally by biasing the Gate of a transistor exactly at its pinch-off, the maximum achievable efficiency could be enhanced up to 78.5% which is very promising when compared to that of Class A. On the other hand, there is a class of operation which is so-called Class AB where the Gate terminal is biased at one particular point between the operating points of Class A and Class B. The power amplifiers with Class AB operation is a way to compromise between the good efficiency of Class B and take advantage of the linearity and maximum output power of a Class A. In other words, it is seen as a hybrid of Class A and Class B power amplifier with a conduction angle of $\pi < \theta < 2\pi$.

As mentioned before, an assumption has been made from an ideal transistor model that a Class B power amplifier is theoretically considered as linear. Under the same assumption, Class AB power amplifier is not linear for all power levels. The reason is that for every input power the conduction angle is most likely to change

depending on bias voltages and currents. When the conduction angle change, the power gain also change leading to a nonlinear relation between input and output fundamental powers. Yet in practice, a Class AB power amplifier is more linear than Class B power amplifier and there is no way to illustrate this through ideal transistor model since the nonlinearity characteristic of a device is technology dependent. Fig. 2.14 shows the relationship between input and output signals.

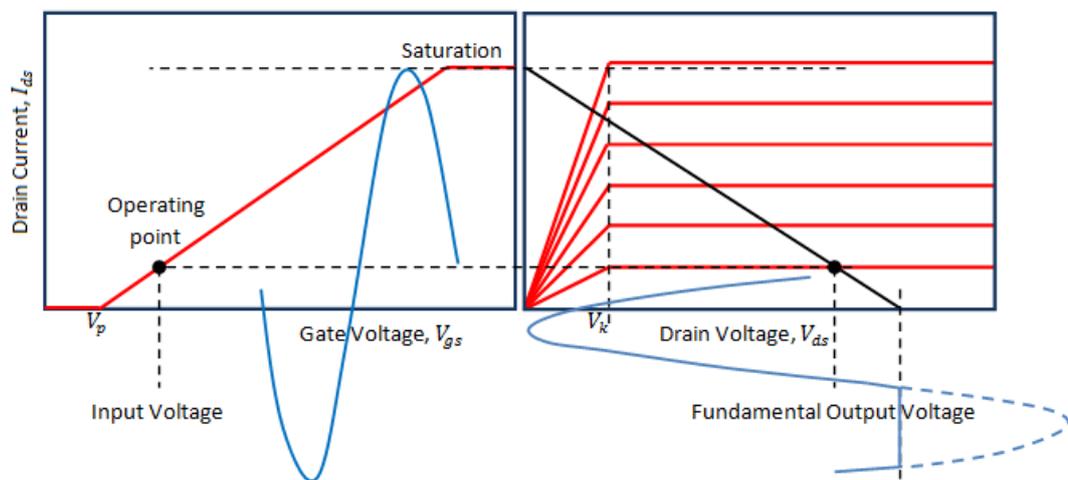


Fig. 2.14: The relationship between input and output waveforms of Class AB power amplifier.

2.4.4 Class C

Power amplifiers that are biased in Class AB or Class B mode of operation are also known as a reduced conduction angle mode. There is another variation of reduced conduction angle which is power amplifier that is working in Class C. It has a gate bias voltage below the pinch-off voltage which means the conduction angle for Class C is below π where the transistor does not conduct for more than half of the

cycle. The efficiency of the power amplifier that is working properly in Class C is higher than that of Class B because of its gate bias voltage below the pinch-off which makes it further increase the ratio of the fundamental component to the DC component of I_{DS} .

Regardless of the potential high efficiency of Class C, this class of operation also suffers from major drawbacks because of its highly nonlinear behaviour. Any signals below the threshold would not be amplified in which that threshold value usually is very technology dependent. The higher order harmonics and intermodulation distortion (IMD) products will make Class C power amplifier even worse, hence the reason why the maximum achievable output power of a Class C power amplifier is always lower than that of Class A. Besides, due to a very low conduction angle ($\theta < \pi$), power amplifier has low power gain.

2.5 Integrated Circuit Antenna

An integrated circuit antenna could be seen as a module made by combining two different basic constituent parts. In other words, these elements are categorised as two recognizably different in nature according to their shared functionality or characteristics. For example, traditionally the research and development on communication radio systems was performed by two individual or separate respective groups of researchers. The boundary between these two groups and this

created a situation where knowledge on technology transfer was restricted and limited.

Copeland et al [20] initially made an effort to breakdown those barriers in order to achieve such favourable advantageous cooperation between those two groups. Although the agreement to cooperate has been well accepted, there were factors which have delayed and impeded the progress or action on the development of integrated circuit antennas. The introductory feature of a printed antenna which is also known as microstrip antenna has further impeded the development of integrated circuit antennas. This is due to different requirement as well as performance imposed by the antennas and circuits on the selection of dielectric substrates [21, 22] hence, making it very complicated to incorporate those two elements on the same board.

In recent decades, there were quite serious events as well as research activities that have pushed forwards the integration of RF circuits with antennas. This has led to a vigorous research activity with determined attempts to produce as well as generate such real and tangible power for a system application at millimetre-wave frequency band. The correlation between frequency band and aperture size which is inversely proportional to each other thus, making it very hard to build and generate sufficient power that complies with the requirements. As a result, the research activities became even greater especially on active integrated antennas and active power combining [23–25].

The branch of knowledge concerned with the single chip transceiver has inspired the main theme of this thesis. Every constituent part including transmitter,

receiver and antenna are built on a single piece of semiconductor substrate. In other words, only required signal and biasing voltage are applied to the port and terminals respectively. Some good references that are closely related to this research have shown similar ideas [26, 27]. Furthermore, an advanced approach mentioned above can be used with the aim of integrating digital signal processing functionality into the same circuit configuration. Realising this involves different kinds of passive and active devices such as resistors, capacitors, inductors, transistors, PIN diodes, schottky diodes and varactors. All the above mentioned devices are necessary when designing integrated circuit and each of them will be serving distinct functions like amplifying, mixing, switching, oscillating and tuning.

An overview of a few kinds of integrated circuit antennas such as amplifying antennas, quasi-optical power combining, self-oscillating active antennas, frequency tuneable and converting antennas, and active transceiver antennas is given in the following subsections.

2.5.1 Amplifying Antennas

As the name amplifying antenna implies, a microstrip patch can be seen like as an antenna being integrated with a transistor as an amplifier. This kind of configuration could probably be applied at the receiver or transmitter in order to either amplify the received or transmitted signals. Besides, this configuration might be good for transmitting antennas because the transmitted power could be increased to the desired level. On the other hand, such a configuration might not be good for

receiving antennas and potentially degrading the front-end system performance because the noise level is increased as well. An et al [28] reported on active array microstrip antenna in which both amplifier and antenna were fabricated on different substrates. This structure has a ground plane in between the two stacked substrates and a coupling probe is used to connect the amplifier with the array of microstrip patch antennas. This configuration benefits from having a range of substrates to allow circuit and antenna requirement to be met without compromise.

Another version of amplifying antenna has been introduced by Robert et al [29] in that it comprises everything including transistor on the same substrate. This upgraded version had a transistor integrated right on a patch, with no extra room required for the transistor. In other words, regardless of the complexity, the compactness is up to another level with reduced loss due to integration between amplifier and antenna, leading to a better absolute front-end system performance in return.

Research and development continues on seeking for a particular quality that will feature amplifying antennas advancement. It becomes more challenging when a relatively small antenna is going to be integrated with an RF circuit. Highly efficient active small antennas have been a motivation for Ellis et al [30] to make practical and effective use of planar inverted F antenna (PIFA) with Class F amplifier. A similar demonstration was reported in [31], where a highly efficient Class F amplifier was integrated with a wideband microstrip slot antenna. On the other hand, Gao et al [32] came up with original ideas using other potential antennas as well as another highly efficient type of amplifier. Gao et al have proven on their practical work that

the integration of a broadband circularly polarised antenna with Class E amplifier is possible.

2.5.2 Quasi-optical power combining and self-oscillating active antennas

Limited space has been a major driver for research into circuit integration. The introduction of technology on integrated solid-state devices opened up new possibilities to every circuit designer. Since then, the circuit size reduction could be achieved more simply and thus, realising a more compact version of fully integrated RF circuit became possible. For example, this technology makes it feasible to integrate an oscillating circuit with an antenna so that one single block of oscillating active antenna is formed.

Modern communication systems in the microwave and millimeter-wave bands typically require more transmitted power than can be produced by a single solid state device. Therefore, alternatively by having several active devices working in parallel could probably generate sufficient power so that the requirements could be met. There are few techniques of combining power from the outputs of multiple active devices which have been introduced and published by Chang et al [33]. The combined power then is channelled through a radiating element for transmitting.

However, techniques of combining power from multiple active devices using combines fabricated on microstrip boards are not efficient at higher frequencies such

as microwave and millimeter-wave bands for instance, where they suffer from severe effects due to conductor and substrate losses which degrade the efficiency of the whole system performance. Staiman et al [34] have discovered a reliable technique in dealing with the aforementioned losses by combining the power in free space. In order to realise this, there should be a proper method to bring about phase compensations between those radiating elements. This method of power combining is called as quasi-optical.

Chang et al [35] have successfully designed and developed self-oscillating active antenna using FET source integrated with microstrip patch antenna in which the microstrip patch itself performs a duty as a radiating element whilst the FET serves as an amplifier where the input and output respectively stay connected with microstrip patch. In order to perform like a self-oscillator, a positive feedback is applied to the FET. Furthermore, there are many more advanced research works on active antennas using quasi-optical as power combining techniques that have been carried out and some published works in this area can be found in [36 – 41].

Another important development, the discovery of a new type of oscillating antenna, was introduced by Fusco and Drew [42]. It uses a locking signal as well as a phase modulator controlled by a variable DC bias voltage applied to the active antenna. The locking signal could be at fundamental, second harmonic or sub-harmonic frequency. A similar concept of active antenna phase control is shown through experiment and it uses sub-harmonic frequency as a locking signal [43]. On the other hand, Cryan et al [44] have performed investigation on analysis of harmonic radiation from an active integrated antenna.

2.5.3 Frequency tuneable and converting active antennas

Bhartia and Bahl [45] have demonstrated another type of active antenna which is equipped with frequency tuning ability. The advantage of this microstrip antenna is that it is capable of tuning as well as reconfiguring the desired frequency using active devices quickly and easily. Moreover, this active microstrip antenna can be tuned down to its lower resonance even though it still uses the same patch dimension. The key success of this frequency tuneable active microstrip antenna is the configuration which is made up of two varactor diodes that are always connected to the edges of radiating elements. With such a configuration, biasing the varactor diodes with variable voltage, changes the radiating element effective electrical length and thus, produces a desired and intended transmit frequency. An active oscillating antenna can also be integrated with a tuning diode so that the oscillation frequency could be tuned dynamically by varying the bias voltage across the diode. Haskins et al [46] have proven this idea is possible in real practice. Another similar work to this has been reported in [47] where the varactor diodes are used as tuning diodes. In this work, a variable voltage across the varactor diodes is a key of determining the polarisation of the active radiating element.

Except for frequency tuneability in an active antenna, another capability of interest is frequency conversion. An active antenna also can be integrated with frequency converter. Stephan et al [48] have published “a quasi-optical polarisation duplexed balanced mixer for millimeter wave applications”. In this work, a simple planar slot-ring antenna is incorporated with two diodes and thus, forming an integrated planar antenna-mixer structure. This structure is then being tested by

receiving the RF and LO signals from another two transmitting antennas. The result shows that 6.5dB losses were obtained from the mixers' frequency conversion at 10GHz. On the other hand, a new compact frequency doubling active antenna was published in [49]. A push-pull technique is used in that it comprises two identical non-linear active devices cascaded in parallel within the configuration. The out-of-phase signals are then separately amplified and recombined those with phase arranged so that the fundamental is suppressed while second harmonic is enhanced. About 6dB conversion gain was obtained from the measurement. Another similar work has been done and reported by Linden and Fusco [50] in which the only difference from the previously mentioned was an anti-phase shifter in the input stage within the configuration.

2.5.4 Active transceiver antennas

Cryan and Hall [51] have presented an interesting new “integrated active antenna with simultaneous transmit-receive operation”. This structure comprises two square patches as radiating elements in which each one of them is integrated with oscillator and a MESFET as an amplifier that are mounted orthogonally at the centre on the edges of a patch. Such integrated active antenna configuration provides “dual linear polarisation as well as sequential rotation” for simultaneous transmit-receive operation. Another previously published work by Cryan and Hall [52] was a “fully duplexed transceiver with transmit and receive operation at the same frequency with the same polarisation”. This structure is actually the integration of an active circulator and quarter-wave short-circuited patch antenna. Also, this active

transceiver antenna is able to be used effectively over short distance communication systems.

Ma et al [53] have reported a “zero-IF detection active antenna” where a zero-IF receiver is tightly incorporated with the integrated active antenna. This active antenna design was actually made up of schottky diodes and two radiating elements which are functioning as the mixers. Therefore, this innovative invention is able to perform both direct-conversion demodulation and direction finding simultaneously.

2.6 Microstrip Patch Antennas

In 1953, Deschamps [54], for the first time proposed an idea on the concept of microstrip radiators and this created something that promoted such intense activities, interest as well as enthusiasm to researchers. Gutton and Baissinot [55] had taken advantage of the proposed concept by issuing the first patent on antennas using microstrip as a radiating element in 1955. This technology did not become practical until the 1970s when it was developed further by researchers such as Howell [56], Munson [57] and others using low-loss soft substrate materials that were just becoming available. There are many good and appropriate research periodicals with critical articles on current activities as well as trends that could be found in [22, 58 – 65].

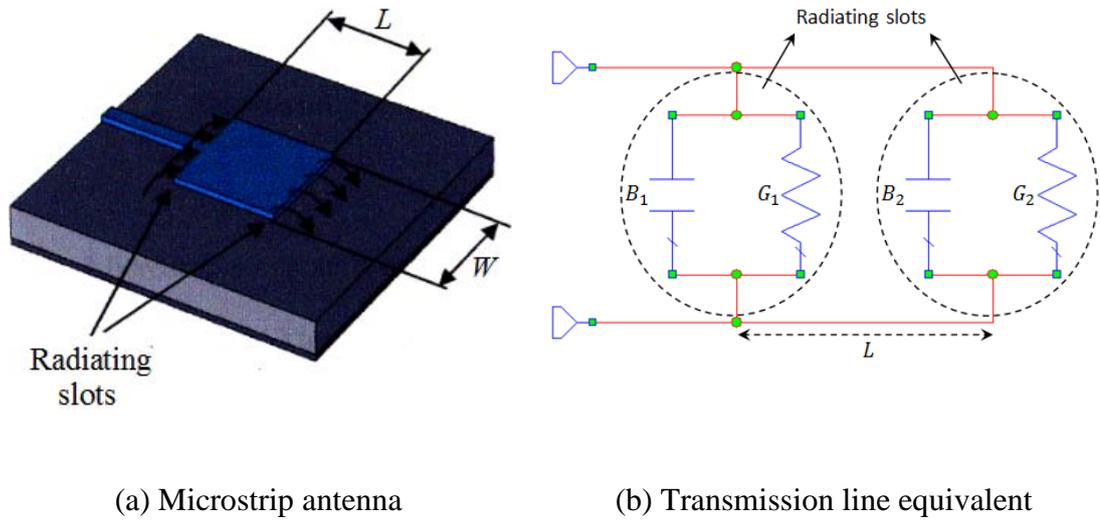


Fig. 2.15: Rectangular microstrip patch and its equivalent transmission line model [66].

A plain and uncomplicated design of microstrip antenna can be easily understood. The configuration is composed of a substrate which is sandwiched between a single patch as the radiating element and a metal sheet as the ground plane. Fig. 2.15 shows the example of rectangular microstrip patch and its equivalent transmission line model. According to Balanis [66], there are many choices in the range of substrates within certain dielectric constant $2.2 \leq \epsilon_r \leq 12$ which could be selected for designing microstrip antennas. Besides, there are numerous shapes of microstrip element that could be potentially used as conductors for radiating patch, as shown in Fig.2.16. As for the simplicity with quite straightforward analysis including layout design and fabrication as well as pleasing radiation characteristic of low cross-polarisation, the shapes of radiating elements such as squares, rectangles and circles will be a good choice for most antenna designers [66]. However, to investigate a wider choice of shapes such as circular ring, disc sector and so on, the numerical analysis methods like Finite Element Method (FEM), Finite Difference Time

Domain (FDTD) or Method of Moments (MoM) are often used to determine the resonant frequencies and modes.

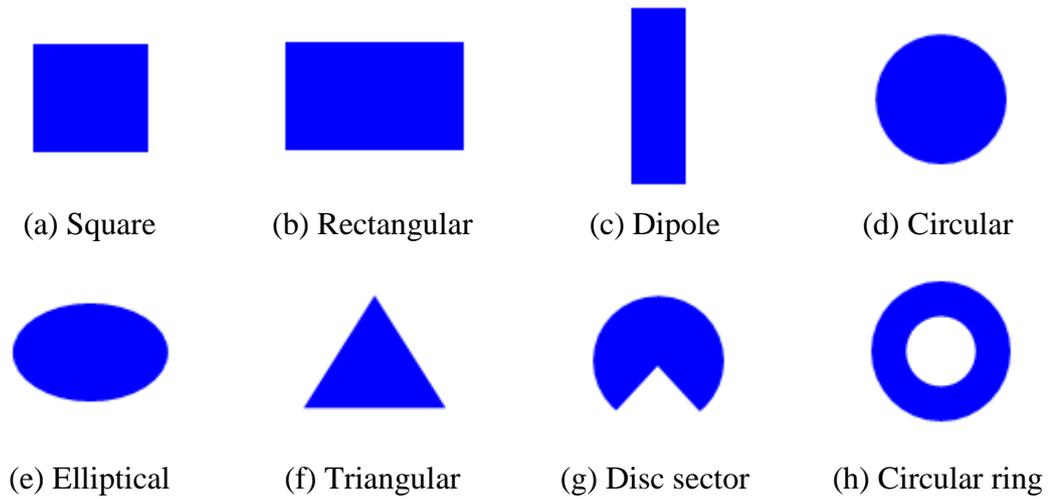


Fig. 2.16: Representative shapes of microstrip elements [66].

Table 2.2: The difference of geometries that could be potentially used as conductor shapes [66].

	Pros	Cons
Square, Rectangular and Dipole	<ul style="list-style-type: none"> - Most utilised patch conductor geometries. - Rectangular patches tend to have the largest impedance bandwidth. - Square patches can be used to generate circular polarisation. 	<ul style="list-style-type: none"> - These geometries are larger than the other shapes.
Circular and Elliptical	<ul style="list-style-type: none"> - Second most common shapes. - These patches are slightly smaller than their rectangular counterpart. 	<ul style="list-style-type: none"> - Slightly have lower gain and bandwidth.

Triangular and Disc sector	<ul style="list-style-type: none"> - These geometries are smaller than their rectangular and circular counterparts. - Dual-polarised can be developed. 	<ul style="list-style-type: none"> - Expense of further reduction in bandwidth and gain. - Tend to generate higher cross-polarisation level due to lack of symmetry in the configuration. - The bandwidth is typically very narrow.
Annular / Circular ring	<ul style="list-style-type: none"> - This geometry is the smallest conductor shapes. 	<ul style="list-style-type: none"> - A complex process is required to excite the lowest order mode in order to obtain a good impedance match at resonance. - The gain is very low and yet it has narrow bandwidth.

Microstrip antennas have distinctive qualities unlike the conventional microwave antennas. Microstrip antennas are lightweight, low profile, conformable on uneven surfaces, simple yet not costing a great deal to manufacture. Moreover, microstrip antennas have enormous potential in working closely with monolithic microwave integrated circuits (MMIC). Such qualities and features arouse intense interest of numerous researchers to employ these advantages into the applications such as satellite communication, aircraft, spacecraft, military and other applications where physical configuration, cost, performance and maintenance issues are important [66].

Regardless of the favourable attributes held by microstrip antennas, there are some conditions limiting the system performance that need to be considered. The

restrictions include narrow bandwidth, low efficiency, high quality factor (Q), low power handling ability and spurious radiation by the feed. Even though the substrate thickness might affect the extent of bandwidth, there is always tendency such as surface waves which are likely to cause harm to the antenna systems performance. In other words, the thicker the substrate, the more severe the harmful effects become, even though the covered bandwidth is wider. Furthermore, an inappropriate substrate's dielectric constant could be detrimental to the RF front-end circuitry especially when it comes to integration of MMIC with microstrip antennas. Therefore, in order to achieve very high levels integration, it is more desirable as well as preferable for the microstrip antenna to be etched on a reasonably high dielectric constant substrate and hence, avoiding from being with poor efficiency and narrow bandwidth [64]. Since the usage of microstrip is favourable and very popular in designing antennas as well as RF and microwave circuits, a good compromise is required over the whole RF and microwave front-end system performance depending on the applications' concerns.

As can be seen in Fig. 2.15(b), the equivalent microstrip antenna could be represented by a transmission line model. This transmission line model is analysed to represent two slots with their respective width, w , and height, h , which is separated by a distance of l [66].

On the other hand, there are quite few feeding techniques that are suitable and famously being used for feeding the microstrip antennas. Each one of them has pros and cons depending on the configurations and applications. Since the microstrip antennas have flat surfaces, they could be perhaps fed either using direct feed from

the microstrip line itself or a coaxial probe from underneath the substrate. Besides, there are other variations of feeding technique which are evolved from the earlier version such as co-planar, aperture-coupled, proximity-coupled as well as coplanar waveguide. The elaborations regarding these feeding techniques are discussed in the following sections. Furthermore, there is detailed coverage of feeding to be found in the literature [21, 59–60, 64].

2.6.1 Coaxial Probe

Coaxial probe is a prominent technique that is frequently used to feed microstrip patch antenna. There are three main elements that build a complete coaxial probe which includes shield, isolation and core. The shield and core usually are conductors and both made up of copper whereas isolation is made up of non-conducting material like Teflon to insulate the shield from the core. The shield should always be attached as well as connected to the ground plane while core should be put into contact with the radiating patch. A cross section of how the coaxial probe being used as a feeding technique for microstrip patch antenna is shown in Fig. 2.17.

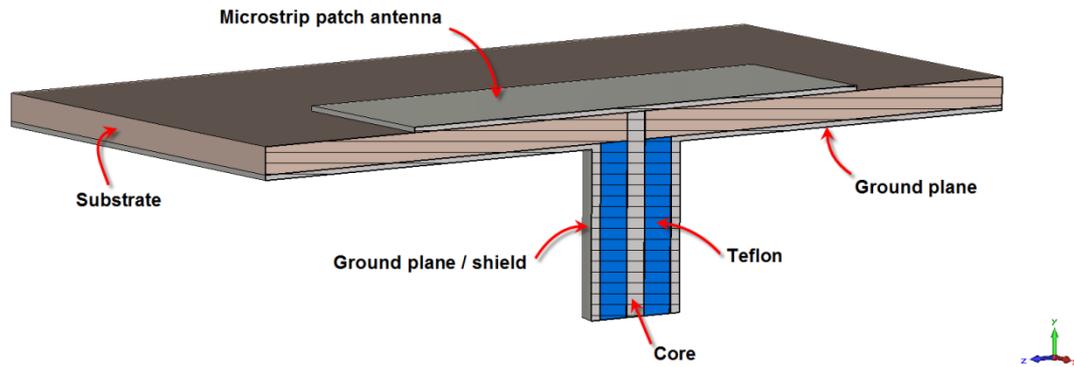


Fig. 2.17: Coaxial probe for feeding a microstrip patch antenna.

As can be seen in Fig. 2.17, it is a simple feeding technique for a microstrip patch antenna. The feed point on a radiating patch could simply be chosen and adjusted according to the input impedance matching. However, there is still a limitation which restricts the usage of such feeding technique on microstrip patch antenna array. This will cause patch antenna array to be fully occupied with large number of coaxial probes underneath the ground plane and solder joints on top of all patches and thus, involving considerable difficulty or hardship in construction. Furthermore, coaxial probe is not practical and suitable to be used as a feeding technique especially for multi-stacked structures. The idea of thickening the substrate is to improve the bandwidth but however, this will require a coaxial probe with a longer core in order to excite the patch antenna at the top. Consequently, this will create the unwanted spurious radiation and surface wave even greater and more severe which could give such bad effects on the whole antenna performance. There are other several references that looked into details about this kind of feeding technique in [67–69].

2.6.2 Microstrip line

Microstrip feed lines are natural choice for microstrip antenna designers. Ease of fabrication makes this feeding technique a favourite option since both microstrip line and patch antenna could be etched on the same substrate at the same time. Fig. 2.18(a) illustrates this method of feeding for microstrip patch antenna. Although it is simple, it has to compromise to some extent. Impedance mismatch happens at a point where narrow microstrip line (50Ω) is simply connected with a wide patch's radiating edge (high input impedance). Therefore, in order to ensure the maximum power transfer from the microstrip line to the radiating patch, impedance matching is absolutely necessary at a point which has caused the mismatch.

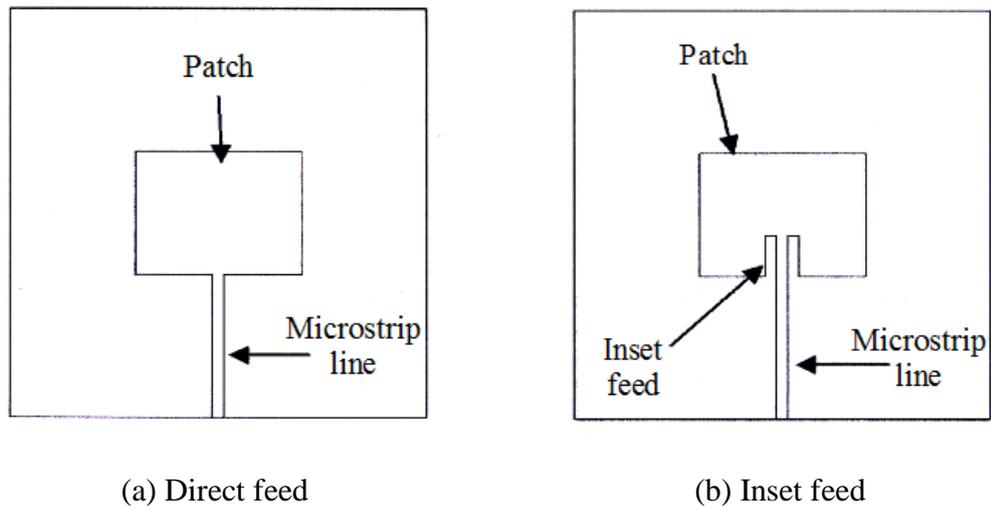


Fig. 2.18: Microstrip line for feeding technique.

The aforementioned impedance matching is done in a simple manner by having a microstrip line inseted within the patch's radiating edge as can be seen in

Fig. 2.18(b). The best feeding point on a patch antenna is being picked out such that the input impedance is 50Ω . The resulting feeding point using inset feed is also similar to that used for a coaxial feed. A detailed investigation and analysis of inset feeding point for patch antennas with rectangular boundaries can be found in [70]. Although microstrip line and coaxial probe are frequently chosen for feeding microstrip patch antennas, these two feeding techniques possess attributes which could be able to generate high order modes that cause cross-polarised radiation to happen [66]. One approach to deal with those problems is to adopt an alternative approach such as contact-less aperture coupled microstrip feed technique.

2.6.3 Aperture Coupled Microstrip Feed

In 1985, Pozar came out with a thought of bringing contact-less aperture coupled feeding technique into effective action. The work written in [71] described in detailed about this contact-less feeding technique by coupling electromagnetic energy from a microstrip line to microstrip patch antenna through a slot or narrow aperture. Basically, in this technique, the slotted ground plane is sandwiched by two substrates in which the radiating patch antenna and feed line are etched on them separately as seen in Fig. 2.19. Generally, this method of feeding is considered as contact-less since the radiating patch antenna and feed line are etched on the separate substrates. Therefore, the side-effects of cross-polarised radiation due to higher order modes could be reduced. Furthermore, it is more versatile because the substrate material selections for radiating patch and feed line can be made independently.

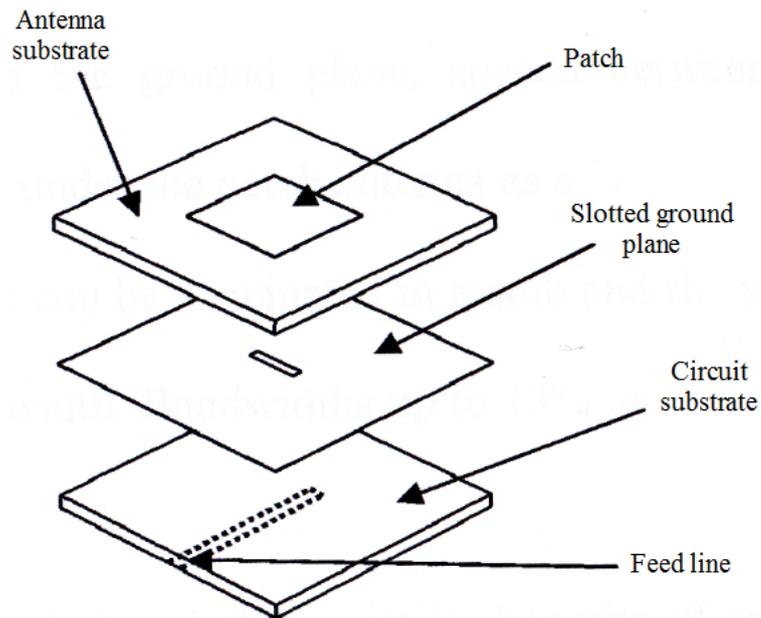


Fig. 2.19: Aperture coupled microstrip-fed patch antenna

A favourable RF and microwave performance could be expected with the advantages of freedom on substrates selection. Different substrates with different material properties in which the circuit and antenna are etched onto substrate with high and low dielectric constant respectively might give optimum result to the whole system performance. In addition, sufficient room or space can be reserved to accommodate any other components especially for tight integration between circuit and antenna modules. A precise manufacturing approach is required in order to align the circuit, slotted ground plane and radiating patch into correct relative positions. Besides, the requirement for extra component parts such as vias in the assembly process no longer exists.

A distinctive attribute of this contact-less aperture coupled feeding technique that came from the coupling through a narrow rectangular aperture is the ability to give significant impact on the intensity of coupling energy between the feed line and

the radiating patch. Unlike round apertures, rectangular shaped apertures as a coupling slot have been widely employed in most aperture coupled microstrip antennas as this gives better strength of coupling effect. However, there are other slot shapes such as H-shaped, dog-bone or bow-tie which have been inspired from the original rectangular shape that can perform even better with improved coupling effect [72, 73]. A detailed explanation on this feeding technique using cavity model and integral equation approach are shown in [71, 74–76] while [77] briefly describes aperture coupled microstrip antenna using transmission line model.

2.7 Microstrip Slot Antennas

A microstrip slot antenna is a type of antenna which has particular shared characteristics with an aperture antenna. Fundamentally, this kind of antenna is simply made up by creating slit of aperture in a rectangular metal sheet as can be seen in Fig. 2.20(a). In spite of the fact that slot antenna is not identical to a conventional dipole antenna to some extent, however, they have many shared characteristics and properties as shown in Fig. 2.20(b). The generalization and extension of Babinet's (Ba-bi-nay's) principle to any slot-based structure has been shown in [78]. A slot can be represented by its equivalent form either in wires or strips which makes it easy to predict the patterns and impedances of the corresponding slots.

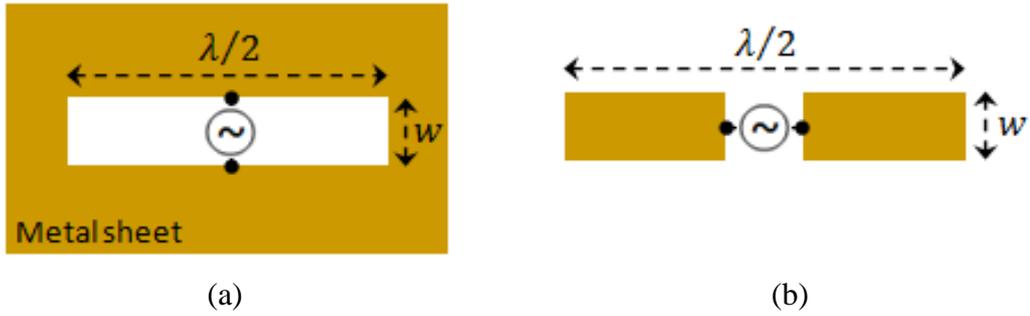


Fig. 2.20: (a) Slot antenna (b) Equivalent dipole

Fig. 2.21(a) shows a clear example of a slot antenna using two $\lambda/4$ closely spaced resonant stubs, connected to a two-wire transmission line and hence, causing it to behave like an inefficient radiator. The spacing between those two $\lambda/4$ -long wires which represent the width of slot, w where $w \ll \lambda$ will be the cause of currents which seem to flow in the opposite direction. As for this reason, no radiation can be expected as the fields within the flowing currents carried by the wires are cancelled out. The other two-end wires can radiate as the currents flow in the same direction, however, those wires are too short ($w \ll \lambda$) to provide such good radiation efficiency.

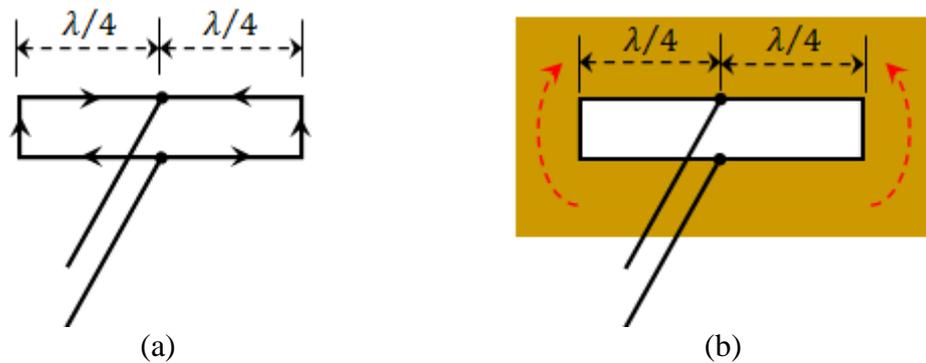


Fig. 2.21: (a) Two $\lambda/4$ resonant stubs (b) $\lambda/2$ slot

A rectangular metal sheet with a $\lambda/2$ -long slit of aperture in the middle as shown in Fig. 2.21(b) is practically more efficient than the wire version. Without being affected by the width of aperture which is particularly very narrow ($w \ll \lambda$), the currents can flow all over the surface of that rectangular metal sheet, giving better performance in term of radiation efficiency since the radiation is equally distributed on both sides of the sheet [79].

2.7.1 Coaxial Probe

A coaxial probe can be used to feed the slot antenna in which the outer part of the coaxial probe is connected to that metal sheet. Fig. 2.22 illustrates the example of coaxial-fed slot antennas. As can be seen in Fig. 2.22(a), the impedance seen by the coaxial probe at the centre of a given slot size is high. Kraus et al in [79] suggested a manner of reducing such high impedance by placing that coaxial probe a little bit away from the centre of a corresponding slot. Fig. 2.22(b) shows the offset coaxial-fed slot antenna where the offset distance is denoted as “s”.

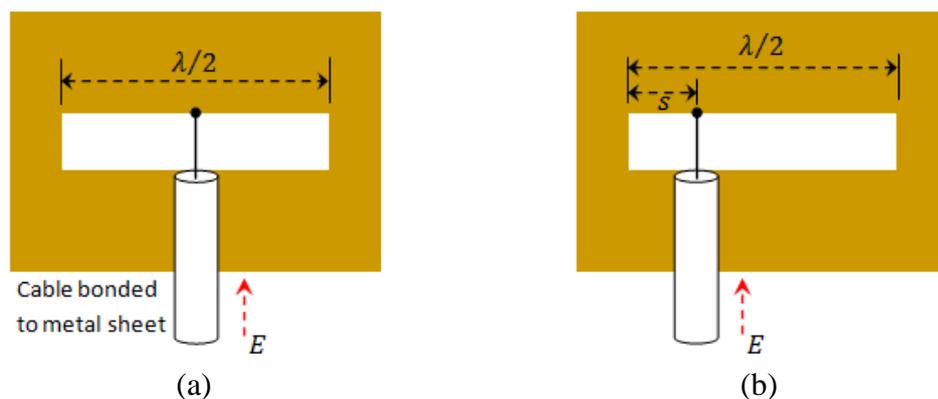


Fig. 2.22: (a) Coaxial-fed slot antenna (b) Offset coaxial-fed slot antenna

2.7.2 Microstrip Line

A very famous method of feeding using a microstrip line can also be used to excite microstrip slot antenna as shown in Fig. 2.23. This microstrip line is placed underneath and purposely being short-circuited with the slot's edge through the substrate as seen in Fig. 2.23(a). Similar to the slot antenna which is using coaxial probe as a method of feeding, the position of microstrip line also is required to be adjusted slightly off the centre in order to achieve satisfactory impedance matching requirement [80]. However, there is another possible technique to obtain such a good impedance matching without changing the feed's position from centre to another. Fig. 2.23(b) shows this alternative is being done by extending microstrip line approximately with $\lambda/4$ -long beyond the edge of slot in such a way that microstrip line is terminated in an open-circuit. This is actually creating an effective virtual short-circuit in the middle of slot and hence, the shorting strip through the substrate is no longer required.

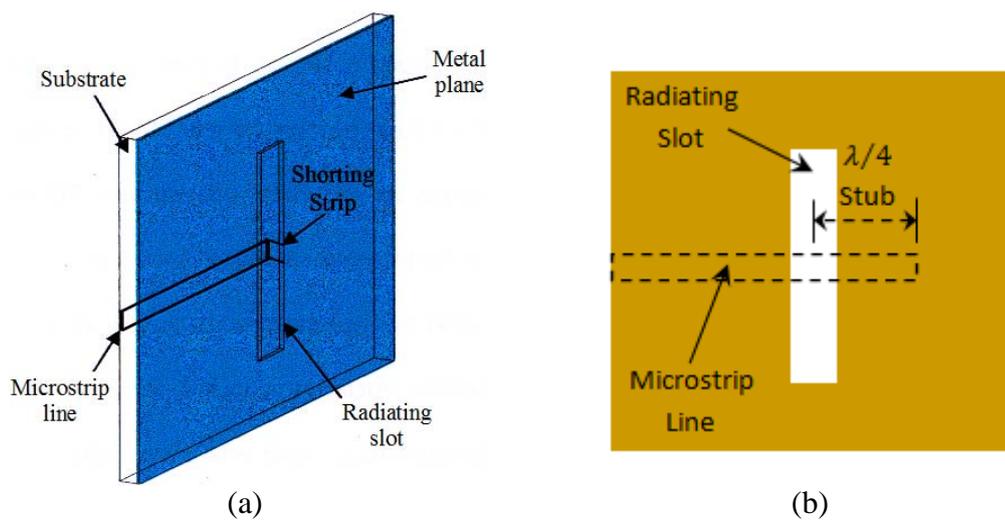


Fig. 2.23: (a) Microstrip-fed slot antenna with shorting strip (b) Microstrip-fed slot antenna with $\lambda/4$ -long stub

Pozar has given a practical demonstration of the stub-tuning technique in that it controls the antenna's reactive load and as a result of that, it can be adjusted to cause the resonant frequency changed simultaneously [81]. Basically, the tuning is done such that input resistance of the stub and microstrip feed line's impedance match at its new resonance. There are several fairly accurate models which have been previously used in designing those kinds of antennas efficiently. Axelrod et al. in [82] have proposed to model the microstrip-slot junction using an ideal transformer and radiated power from the corresponding slot is predicted by its equivalent radiation resistance. In contrast, Himdi et al. in [83] estimated the radiated power from the slot including radiation conductance as well as the attenuation constant using a lossy transmission line model. Other related works on modelling the networks for microstrip-fed slot antennas can be found in [84, 85].

2.8 Balanced Fed Antennas

Earlier in the previous sections, different types of antennas were introduced and their methods of feeding have been briefly described. Those antennas have been using quite similar unbalanced methods of feeding. The radiation from this kind of configuration was contributed evenly by the antenna and its ground plane. Consequently, the antenna performance will become out of tune as if the parameters vary or any other elements and devices on the ground plane are modified. As for that reason, the antenna is in absolute need to be rebuilt. In addition, the cost of

modification in order to suit a particular individual task is not cheap and it is not worth-doing when the antenna is integrated with other RF active devices.

A way of dealing with a problem associated with unbalanced feeding is to use a balanced fed antenna. Sasaki et al. in [86] have shown the work on balanced fed planar dipole antenna for handset in which the currents in the ground plane have reduced effectively. This is due to inverted version of the antenna itself is seen as a reference plane by the currents. Therefore, the currents which have been previously flowing into ground plane are now effectively being channelled to another path.

The unbalanced antennas are still relevant in modern communication systems as long as the RF front-end networks are used to feed them. By doing this, the unbalanced antennas appear to be like a balanced fed antenna since most RF front-end network's signalling mechanism are differential in which the systems can take advantage of the benefit on differential feeding technique that is high immunity from crosstalk. The push-pull power amplifier (PA) configuration as shown in [87] used a differential feeding technique in that it uses two 180° hybrid at both ends (input and output stage) for the purpose of splitting the signal to become out-of-phase before feeding into two transistors and recombine the outputs from the transistors before feeding to the antenna as seen in Fig. 2.24(a). The fact of 180° hybrid being used at the input stage as a power splitter that will definitely contribute to losses, the added losses due to 180° hybrid as a power combiner degrades the front-end system performance and makes it bulkier. Therefore, in order to reduce the losses and achieve increased efficiency simultaneously, the 180° hybrid at the output stage should ideally be removed. Complying with the active integrated antenna concept,

this offers advantages of neat and tight integration of a push-pull transmitting power amplifier as shown in Fig. 2.24(b). Besides, the push-pull configuration itself has its own benefit in which the output power is twice that of a traditional single-ended power amplifier [87].

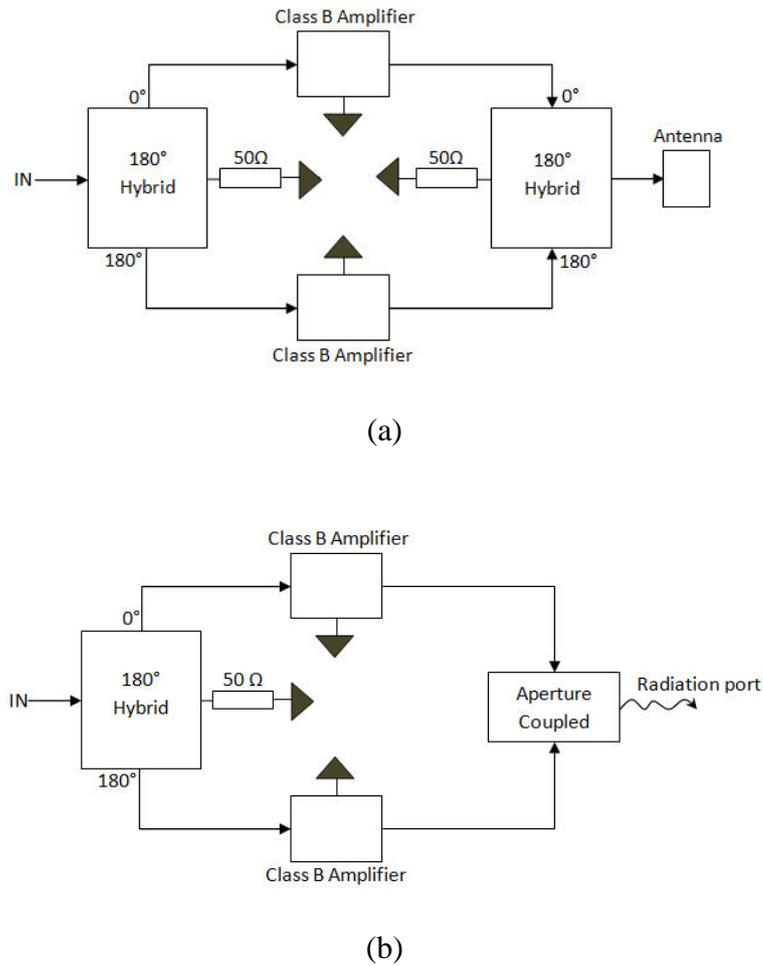
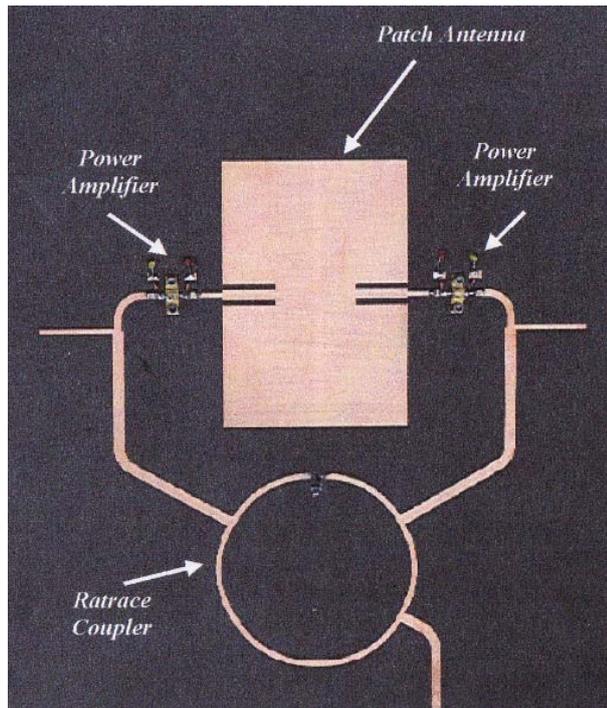


Fig. 2.24: Architecture of: (a) traditional and (b) integrated-antenna push-pull power amplifier front-end.

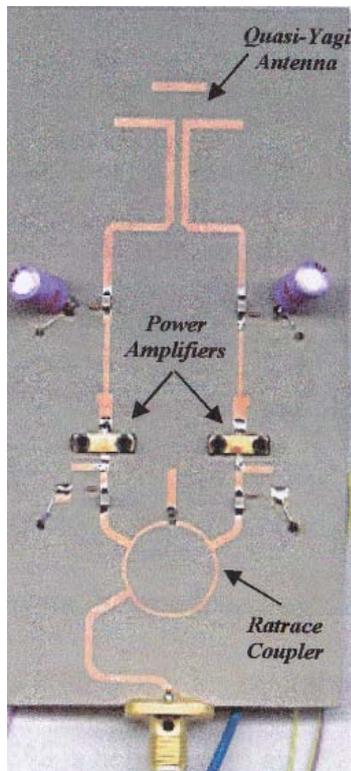
Fig. 2.25 shows the examples of previous developments on the integration of RF circuit with antenna front-end which have involved push-pull power amplifier configuration and balanced antennas. As can be seen in Fig. 2.25(a), the dual-feed

microstrip rectangular patch antenna has replaced the use of 180° hybrid within the push-pull power amplifier configuration and this prototype has been fabricated on a single dielectric slab. As reported in [12], this prototype was measured at the operating frequency of 2.5 GHz and the maximum achievable power-added-efficiency (PAE) was 55% within its typical narrow microstrip antenna's bandwidth.

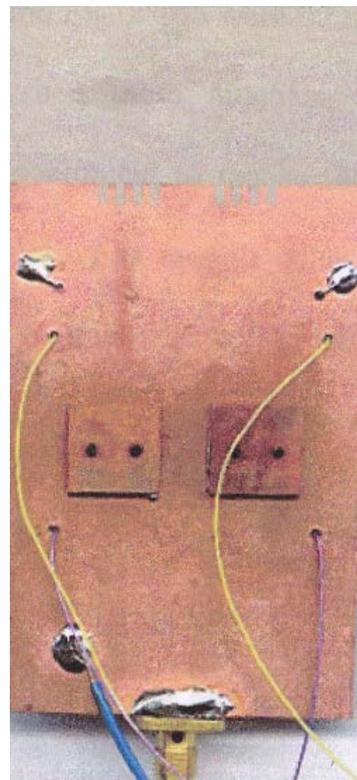
Fig. 2.25(b) shows a quasi-yagi antenna integrated with push-pull power amplifier. The push-pull circuit and quasi-yagi antenna are etched on the same substrate. Both circuit and antenna shared the same ground plane except for the truncated part which is dedicated for quasi-yagi antenna as a typical reflector to produce endfire radiation. There are some parts at the edge of the truncated ground plane which are corrugated. This is specially tuned to perform as 180° hybrid (power combiner) as well as harmonic termination. Basically, the feed-line that leads to the yagi is seen like a monopole and this has caused a noticeable radiation at higher order harmonics. The truncated ground plane is purposely being shaped into alternate ridges or corrugations at $\lambda/4$ depth with respect to the second harmonic so that the unwanted radiation due to corresponding harmonic could be suppressed. This prototype has been measured to have good return loss which is $S_{11} < -10 \text{ dB}$ over 50% its operating bandwidth [88].



(a)

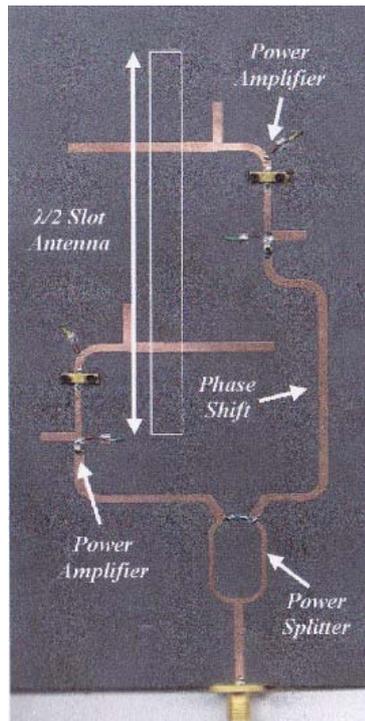


Top

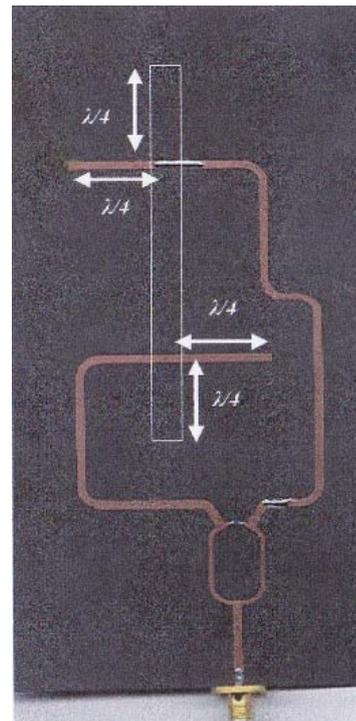


Bottom

(b)



Active integrated antenna



Passive antenna

(c)

Fig. 2.25: Push-pull integrated front-end: (a) Patch antenna [12], (b) Quasi-yagi antenna [88], (c) Slot antenna [12]

The first two push-pull integrated antenna front-ends shown in Fig. 2.25(a) and Fig. 2.25(b) were constructed on the same layer of substrate. Those two prototypes are relatively big, making it uneconomical and wasteful to manufacture or to realise onto semiconductor substrate. Therefore, it has been suggested in the previous chapter as a viable option to build the antenna and its front-end circuit separately. Fig. 2.25(c) shows how the dual-feed slot antennas were fed differentially using a backend circuit through an open-circuited microstrip line. As for impedance matching between the slot antenna and its feeding mechanism, a microstrip line $\lambda/4$ -long beyond the edge of slot is terminated in an open-circuit. This will create such alternate coupling of electromagnetic energy in the middle of slot and hence creating

a good transmitter. The active integrated version has been measured at 2.46 GHz and appeared to have maximum achievable PAE of 63% which was better than passive antenna version as reported in [12] about 55% within 8% their operating bandwidth.

Table 2.3: Performance comparison of push-pull integrated front-end using rectangular patch antenna [12], quasi-yagi antenna [88] and slot antenna [12].

Patch antenna	Quasi-yagi antenna	Slot antenna
$f_o = 2.5 \text{ GHz}$	$f_o = 4.15 \text{ GHz}$	$f_o = 2.46 \text{ GHz}$
$Max \text{ PAE} = 55\%$	$Max \text{ PAE} = 60.9\%$	$Max \text{ PAE} = 63\%$
$BW = 3 - 4\%$	$BW = 50\%$	$BW = 8\%$
<i>Build:</i> Antenna and its front-end circuit were fabricated on the same layer of substrate.		<i>Build:</i> Antenna and its front-end circuit were fabricated separately on a single layer substrate.
<i>Size</i> is relatively big due to 180° hybrid at the input stage.		<i>Size</i> has been further reduced by using a Wilkinson power divider and 180° delay line.
Antenna feeding mechanism provides three functions at the same time, a radiating element, a power combiner and a harmonic tuner.		

2.9 Summary

Due to the challenges in achieving a highly integrated single chip transceiver solution, this chapter has provided an overview of the integrated circuit-antenna concept and presented the variants of this concept. Besides, the background and overview which include microwave theory, conventional power amplifier classes have been reviewed. The different antennas that were used in this thesis were also

presented with brief explanations of their operations and feeding methods. Both single-ended and balanced fed antennas were shown. Single-ended antennas require matching networks when connected to most communication systems that are largely differential.

Current implementations in modern communication systems shown in section 2.8, which use balanced fed antennas, have the potential for easy matching with RF front-end circuitry. There are significant advantages in terms of designs and cost effectiveness which result in the RF front-end circuitry and antennas being on the same substrate. In other words, the integrated RF circuit-antenna is fabricated using on-chip technology. However, due to the cost factors and aperture size, the on-chip circuit-antenna has been largely compromised on the performance like gain, bandwidth and efficiency. This suggests a reasonably small off-chip or externally built antenna is still a viable option to be differentially fed using MMIC through contactless coupling technique.

CHAPTER 3

DESIGN OF PUSH-PULL CLASS B POWER AMPLIFIER

3.1 Introduction

In the previous chapter, the background and overview which include microwave theory, conventional power amplifier classes as well as early innovations and developments on active integrated circuit antennas have been presented. In the rest of this thesis, the most important part is about a push-pull integrated antenna front-end in which the differential feeding technique is employed on an antenna which is normally driven unbalanced, so that the unbalanced antenna will behave like a balanced fed one despite having the same advantages of high immunity on crosstalk and twice the output power through power combining.

This chapter will present the design procedure based on the research flow charts and the simulation technique for a single-ended power amplifier and the implementation of a push-pull power amplifier configuration. The results from the simulation were obtained using available simulation software which is AWR Design Environment Microwave Office (AWRDE MWO) by National Instruments. Two different types of transistor were proposed to undertake the load pull analysis as a single-ended power amplifier which are NEC NE722S01 Low Noise / Low Power

MESFET and NITRONEX NPTB00004 RF Power GaN HEMT. These two active devices have been randomly picked from the software's library, since the proposed concept for direct integration of amplifier and antenna has been claimed that it could be applied to any devices and bias conditions. These devices are employed separately in a push-pull circuit configuration and the simulated results are compared in terms of the theoretical maximum achievable Power Added Efficiency (PAE) as well as their Total Power (PT).

First and foremost, the history of push-pull output will be briefly introduced and the operation of the push-pull power amplifier is generally explained. This is then followed by a design routine introduced by Cripps [19, 89] about load pull design procedure.

3.2 History of Push-pull Output

Nowadays, there are many amplifier output design stages inspired by the push-pull circuit configuration. This technique was already well-known among the electronics engineers and its principle of operation had been first documented in 1895 [90]. An example to demonstrate this technique had been described in Colpitts's patent with the arrangement using double-ended of identical audion tubes which was granted in 1915 [91]. In 1924, a balanced amplifier was formed using push-pull amplifier in that it used two identical low-power vacuum tubes. The result was found very promising during those days with acceptable low power consumption

[92]. This fruitful technique continues to be employed on today's radio communication engineering systems.

3.3 Design Architecture of Push-pull Amplifier

A push-pull output is a type of electronic circuit that uses a pair of active devices that alternately supply current to a connected load. This is such a good alternative in order to achieve better performance instead of using only one transistor to drive the load especially in the environment where low distortion is vital. How well a single ended amplifier might be designed, a push-pull amplifier will always be the best in terms of low distortion, high output power and good fidelity. Therefore, push-pull amplifiers are superior over single ended amplifiers.

The principle of operation for a push-pull amplifier begins with the signal being divided into two signals with the same magnitude and 180° phase difference. Generally, the signal is divided by using a 180° hybrid, coupling transformer or balun. In this work, 180° hybrid is used and it is arranged in such a way that one signal is injected to the gate of transistor while the out-of-phase signal is injected to the gate of the other transistor. Fig. 3.1 shows the typical configuration of push-pull power amplifier using 180° hybrid couplers as the power splitter and the combiner respectively.

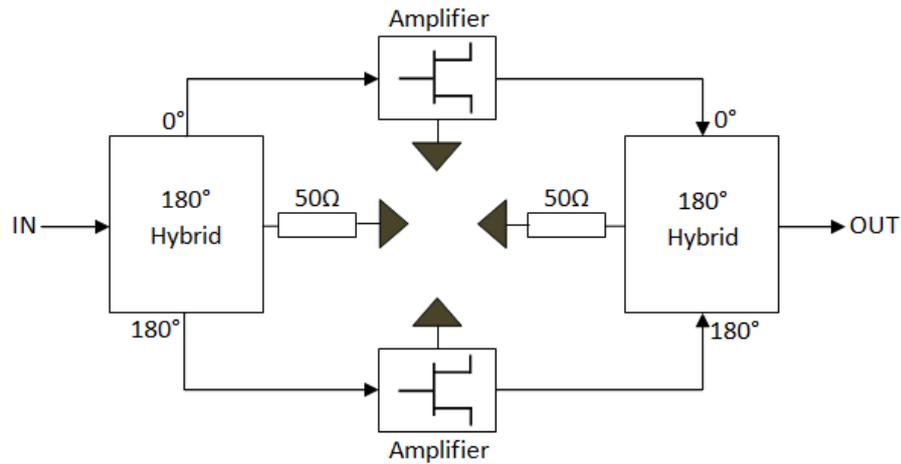
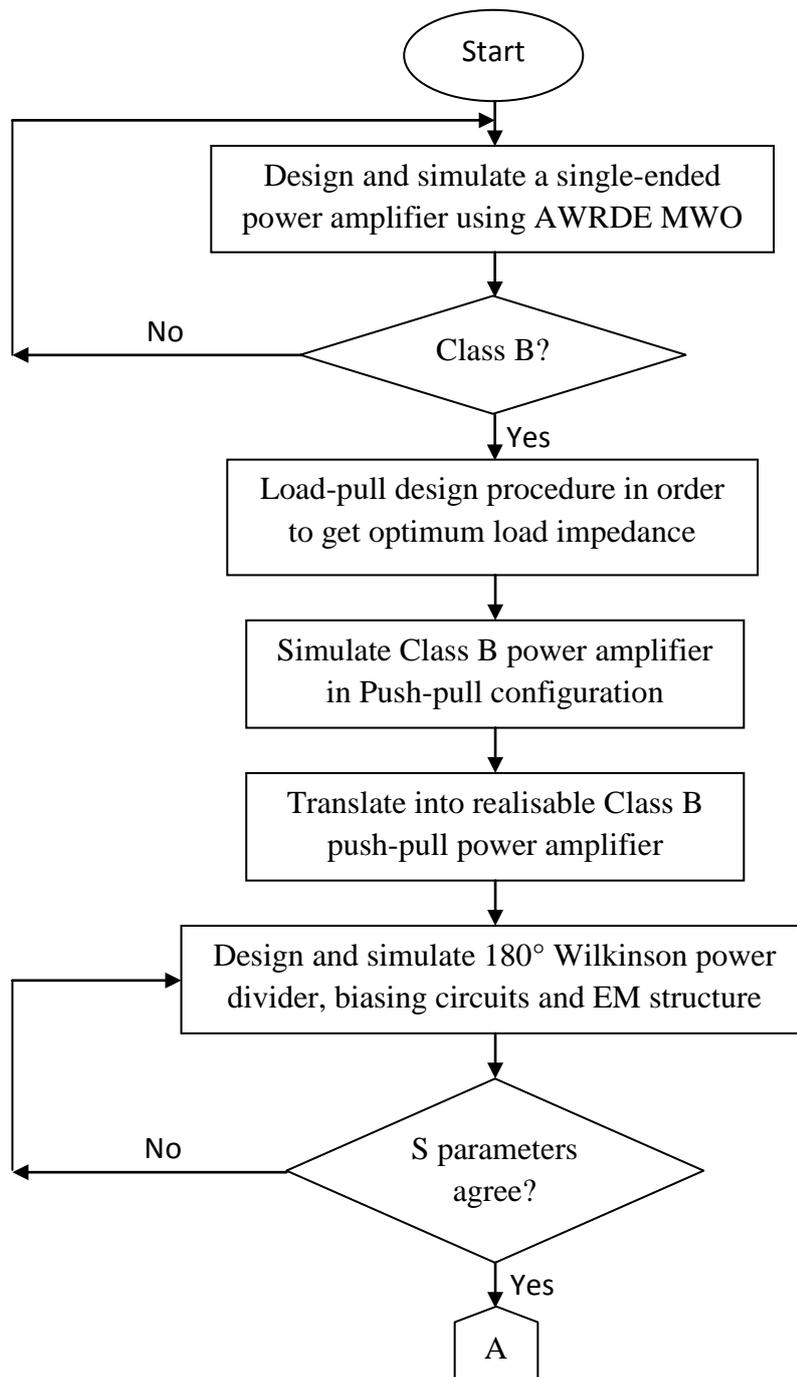


Fig. 3.1: Push-pull power amplifier configuration.

Another advantage that push-pull has including the cancellation of ripples due to power supply voltage and hence, it produces low an unwanted signal at the output. Meanwhile, the disadvantages of the push-pull configuration, there should be two identical transistors working in order and the requirement of hybrid coupler which is loss and adds to complexity, hence restricting the whole system performance. Furthermore, distortion is not only restricted due to non-linearity of the transistor dynamic transfer characteristic. It might happen when the two halves of the input waveform un-synchronisely amplified because one of the greatest challenges in designing push-pull power amplifier lies within the balun design. The desired balun will need to have several characteristics such as low amplitude and phase imbalances, symmetrical balanced ports (impedances looking into the balanced ports are required to be identical), high return losses at all three ports for achieving high push-pull power amplifier gain and high balanced ports isolation for good push-pull power amplifier stability. Besides, the distortions happened because of the transistors used in the configuration are not identical or they do not share similar characteristic.

3.4 Research Design Flow Chart

The research design flow is divided into two different flow charts. They are research flow charts for the active device part which is a Class B push-pull power amplifier design and a research flow chart for the EM structure, which involved the aperture coupling technique. These are shown in Fig. 3.2 and Fig. 3.3 respectively.



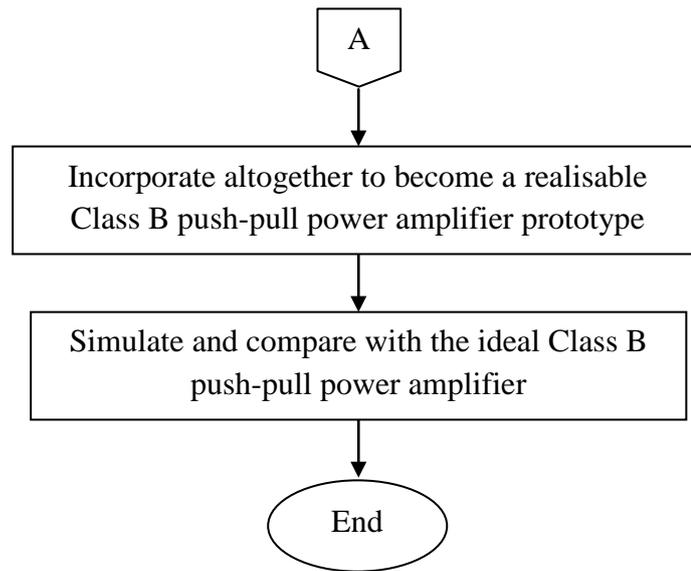
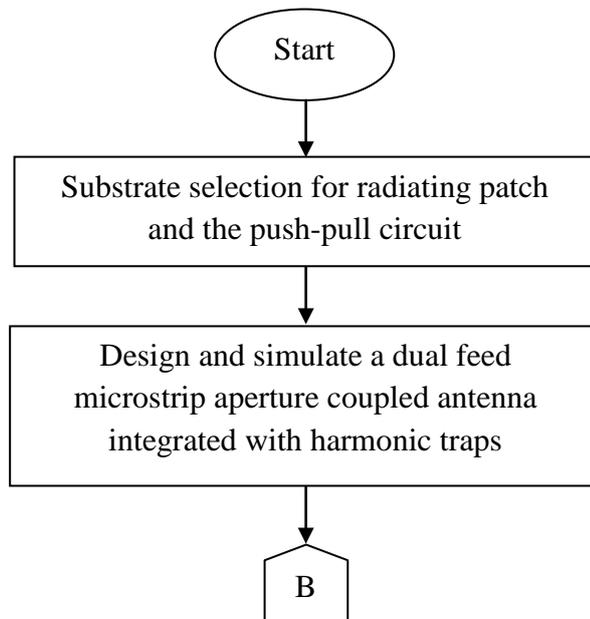


Fig. 3.2: Flow chart of designing push-pull Class B power amplifier.



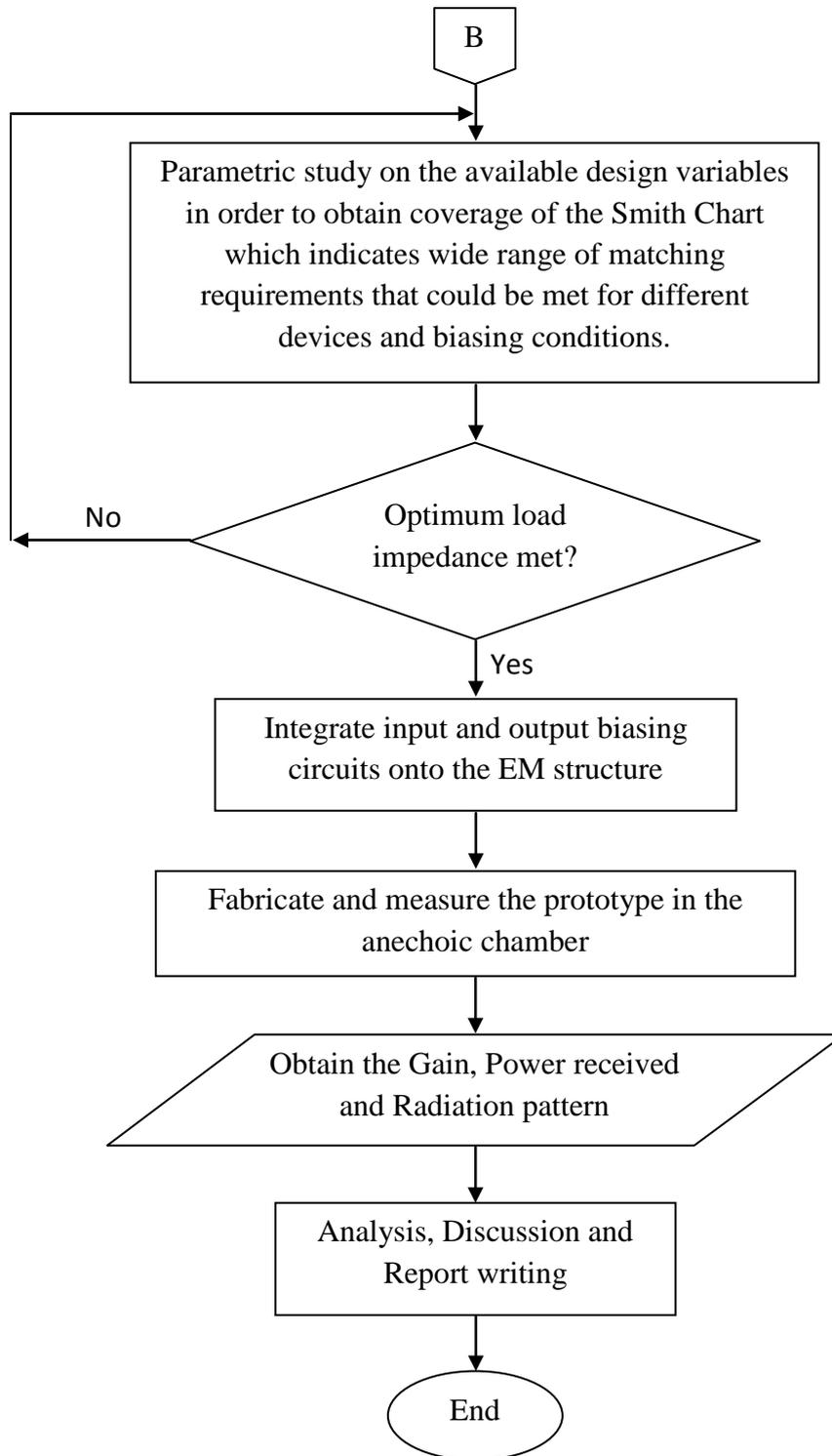
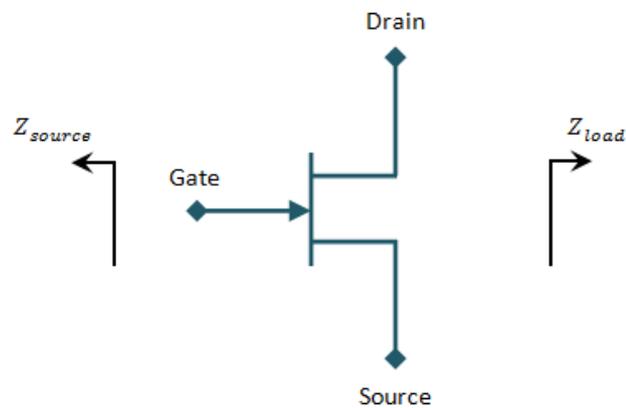


Fig. 3.3: Flow chart of designing EM structure using aperture coupled technique

3.5 Design Procedure

Transistor manufacturers typically publish experimentally derived optimal impedances for source and load terminations at given frequencies and bias conditions. An example is given in Fig. 3.4. If a non-linear device model is available, it can be used to determine these parameters for arbitrary frequencies and bias conditions. Note that device example given below is for a reader general knowledge purposes as this device will not be used and not related in the remainder of this thesis. However, in this work, Modelithics Inc. from Tampa, Florida will supply the required non-linear device models under an educational licence and AWRDE MWO is used to demonstrate the procedure.



Frequency (GHz)	Z_{source}	Z_{load}
0.5	$20.2 + j16.18$	$51.7 + j15.2$
1.0	$8.38 + j9.46$	$41.4 + j28.5$
1.5	$7.37 + j0$	$28.15 + j29$
2.5	$3.19 - j4.76$	$19 + j9.2$
3.5	$3.18 - j13.3$	$14.6 + j7.46$

Fig. 3.4: Example of experimentally derived optimal source and load impedances of a transistor. (Source: Cree Inc., CGH40010 Rev. 3.3)

The design procedure illustrated here is using a single-ended Class B amplifier example. The transistor used in this section is Modelithics' non-linear model NEC NE722S01. The operating frequency is simply chosen at 2.06 GHz. Since at the beginning, we have started the works using this device (NEC NE722S01), hence the following sections will be about the aforementioned device. When it comes to realisation, this device (NEC NE722S01) is known as no longer produced by the manufacturer. However, we prefer to keep the findings related to this device and therefore, in the remainder of this chapter, there will be analysis on this device to design a single-ended Class B amplifier and ultimately forming a push-pull transmitting amplifier in the end. However, on the other hand, a device model Nitronex NPTB00004 will undergo the same procedure with different bias conditions but it will be not shown in this thesis. Table 3.1 shows the difference between two proposed devices used in this work. There is only one device will be chosen to be developed as a prototype which is using device model Nitronex NPTB00004. Although the whole procedure is fully performed using simulation software, it is also applicable to an experimental approach with a real non-linear device.

Table 3.1: The difference between two proposed devices.

	NEC NE722S01	NITRONEX NPTB00004
Device Technologies	GaAs	GaN
Operating Frequency (GHz)	<i>C</i> to <i>X</i> Band 4 – 12	<i>DC</i> to 6
Output Power at 1dB Gain Compression Point, <i>P1dB</i> (dBm)	15	34.6
Power Gain, <i>G</i> (dB)	$V_{DS} = 3 V, I_{DS} = 10 mA,$ $T = 25^{\circ}C, f = 4 GHz$ $G = 12$	$V_{DS} = 28 V, I_{DS} = 50 mA,$ $T = 25^{\circ}C, f = 2.5 GHz$ $G = 15.5$

3.5.1 Input Matching Setting

The matching approach used for the input matching network design is approximately equivalent to a conjugate impedance matching problem, maximising the gate voltage swing on the input terminal of the transistor. The approximation arises because the transistor input impedance is power dependent, so the appropriate drive level must be used in the simulation. Therefore, a fix drive level input power as well as exact bias conditions has been specified at which the simulation / measurement was conducted.

Note that the settings for the input power and bias conditions are only applicable to this particular device NEC NE722S01 at resonant frequency 2.06 GHz. In this case, the input power of 10 dBm is used while at the gate bias voltage and drain bias voltage have been specified to be at $-1.8 V$ and $3 V$ respectively. These settings are purposely to ensure that amplifier will be working efficiently in Class B. The circuit configuration shown in Fig. 3.5 is for getting appropriate input impedance with its conjugate impedance match, giving simulated result shown in Fig. 3.6 as $\Gamma_{in} = 0.9323\angle -50.22$, hence its conjugate $\Gamma_{source} = 0.9323\angle 50.22$. This conjugate impedance match value will be substituted within the input HBTUNER2 and this value is also used for further simulation especially in load-pull analysis.

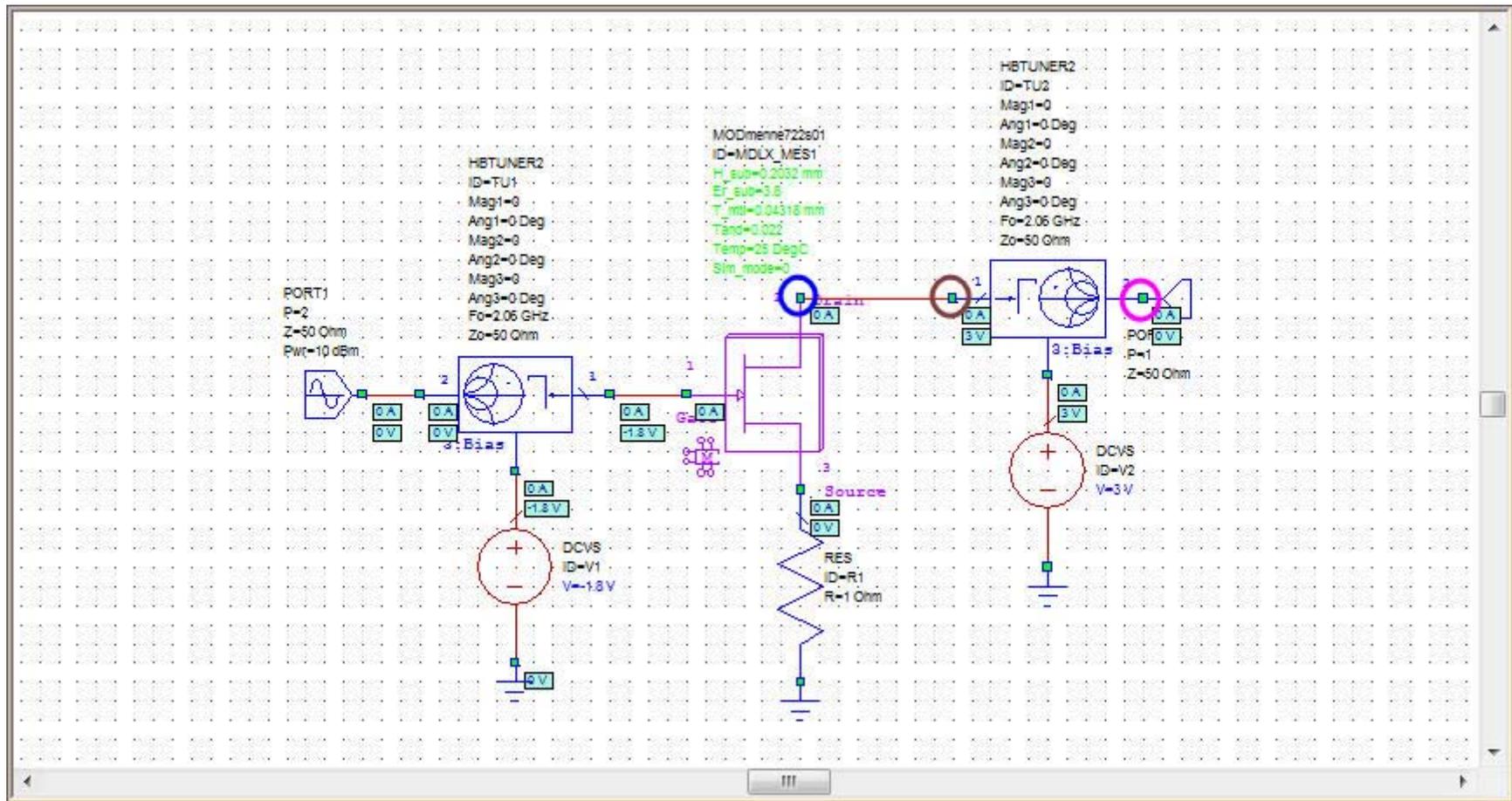


Fig. 3.5: Circuit configuration for input matching setting.

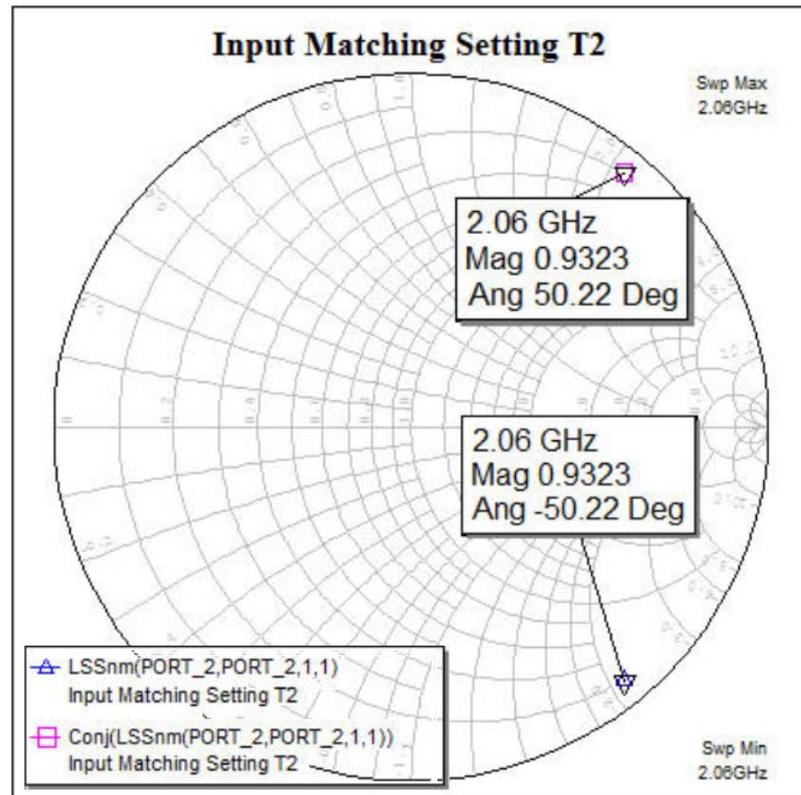


Fig. 3.6: Simulated input impedance matching.

3.5.2 I-V Analysis

The transfer characteristic shown in Fig. 3.8 is derived from analysis of the circuit schematic shown in Fig. 3.7, with multiple traces corresponding to different drain bias voltages (V_{ds}) which are listed as parameters from p1 to p10 in unit Volt (V). The differences in the traces are due to the thermal effects which are included in the model. However, the threshold gate voltage (V_{th}) and V_{max} which values respectively are $-2.09 V$ and $0.9 V$, are almost independent of the drain bias voltages. In this case, the drain voltage is kept relatively low ($V_{ds} = 3 V$) in order to reduce thermal problem to get into demonstration.

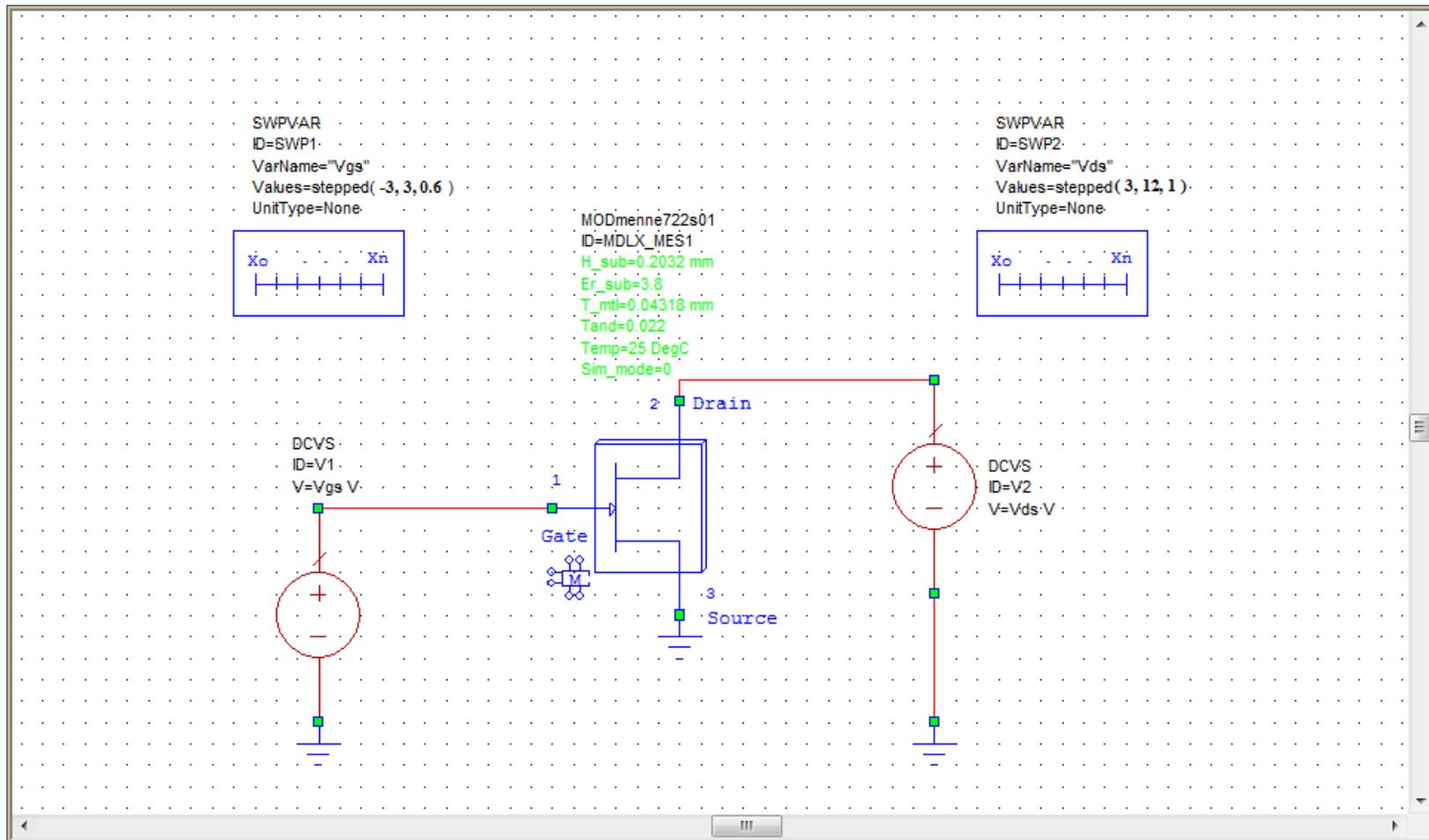


Fig. 3.7: Circuit schematic for deriving a transfer characteristic of the transistor.

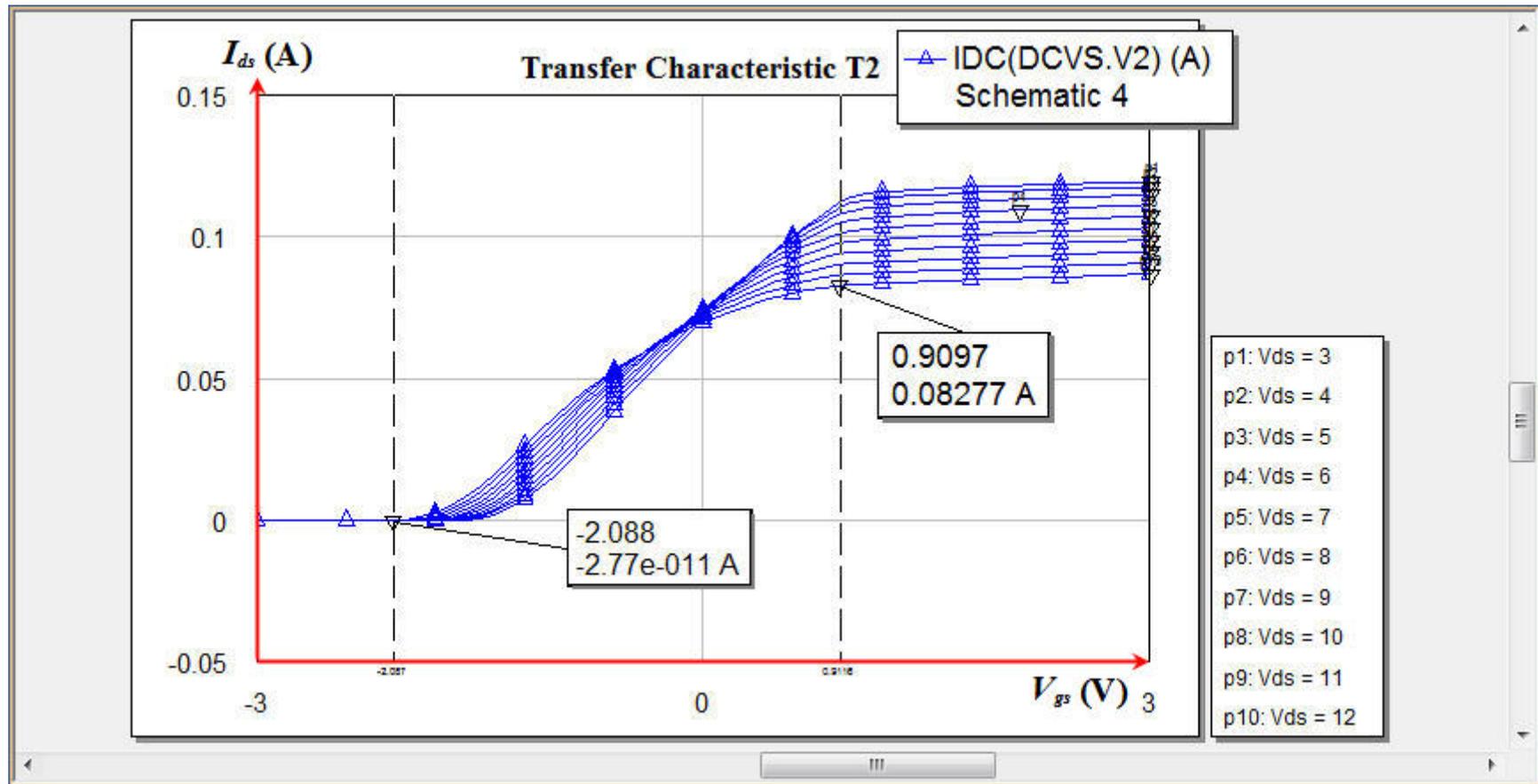


Fig. 3.8: Transistor NEC NE722S01 transfer characteristic.

Generally, V_{th} is where $I_{ds} \approx 0 A$. I_{ds} in this case is also known as drain quiescent current. In a case of not concerning about the class of operation for that particular transistor, the gate bias voltage can be simply chosen between V_{th} and V_{max} ($V_{th} \leq V_{gs} \leq V_{max}$) whose values are $-2.09 V$ and $0.9 V$ approximately. In this work, Class B is chosen as a class of operation. Therefore, a bias gate voltage V_{gs} is set at where the drain quiescent current is almost equal to zero. As for this case, $V_{gs} = -1.8 V$ while at this point the quiescent current is still near to zero ($I_{ds} \approx 0 A$).

On the other hand, the circuit schematic as in Fig. 3.5 is also used to compute the I-V curve and I-V Dynamic Load Line (IVDLL) shown in Fig. 3.9. Note that the parameters on the DC Voltage Source (DCVS) of both tuners have been set up for Class B operation. As can be seen in Fig. 3.5, there is no current flowing in the drain to source of the device ($I_{ds} = 0 A$) which means the amplifier is already in the Class B mode. Fig. 3.10 shows the Class B half-rectified current waveforms at three different reference device planes (reference circuit is shown in Fig. 3.5). Ideally, we need to look at the waveform on the package model. Due to limitation, the waveform at the device plane also gives an indication of working in Class B. It would be more clearly if we could do all impedance synthesis within the package model by looking at their intrinsic waveforms. Besides, in term of device stability analysis, since we do not have bias dependant S-parameters and therefore a proper stability analysis cannot be done. If designer wish to prove to full working design, it would be necessary to perform a proper stability analysis at this stage.

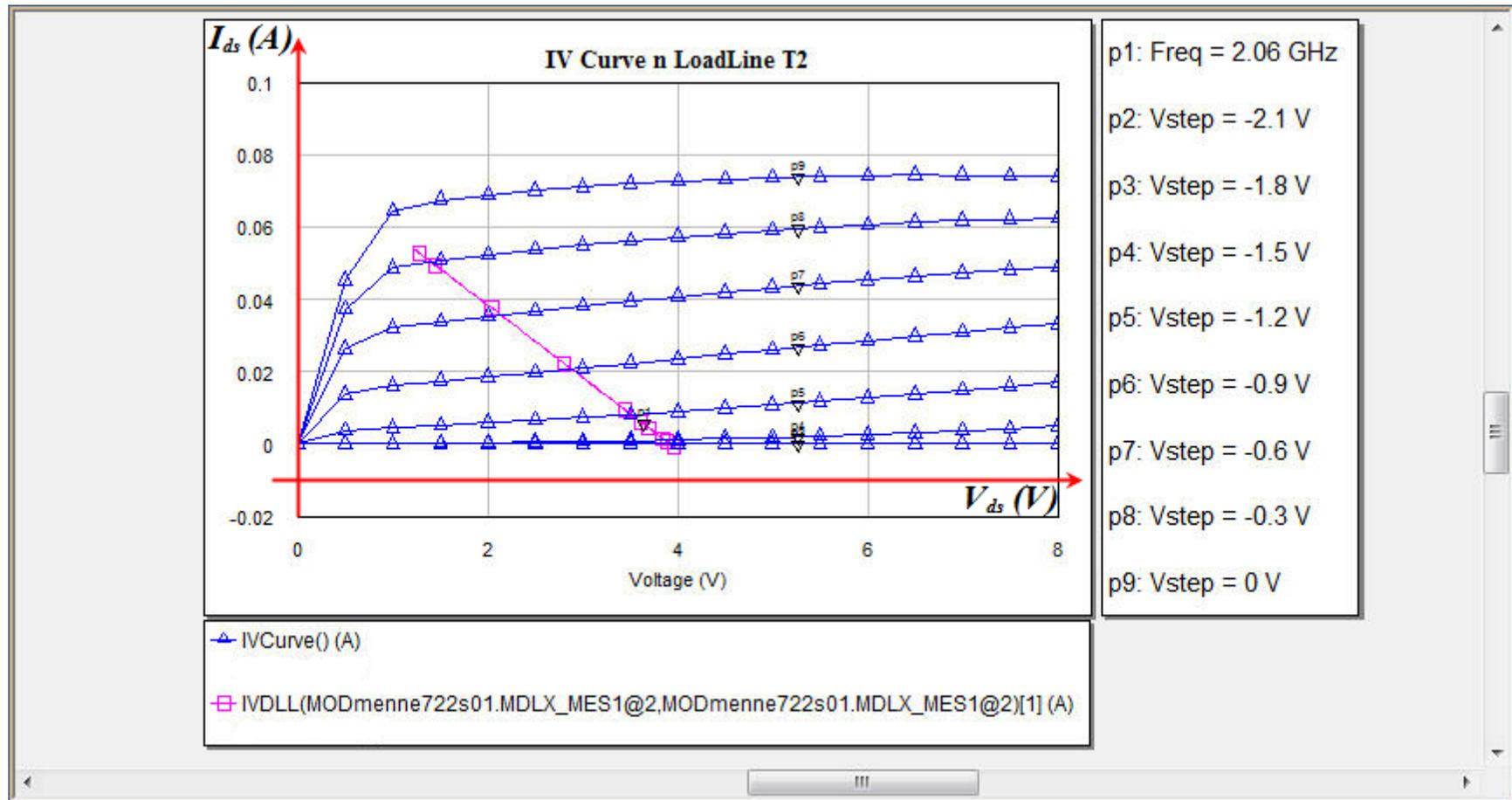


Fig. 3.9: DC-IV plot of the device NEC NE722S01.

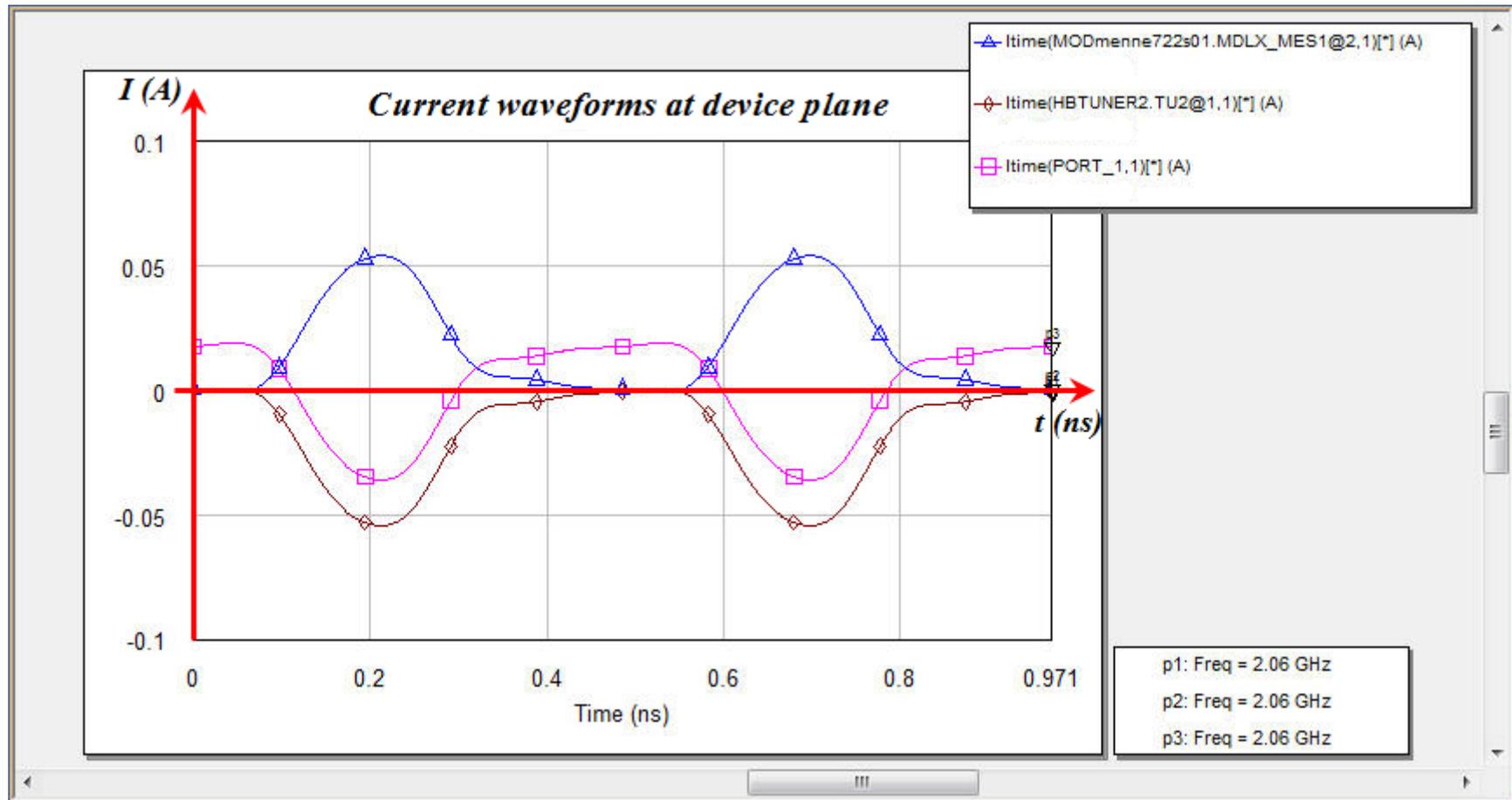


Fig. 3.10: The Class B current waveforms at three different reference device planes.

3.5.3 Optimum Load Impedance

In non-linear RF circuit simulation, harmonic balance or frequency domain analyses are widely used mainly for two reasons. First, time domain or transient analyses, in the case where there are harmonics or closely-spaced frequencies, the simulation must be run for long enough to observe one full period of the lowest frequency present since the minimum time step must be compatible with the highest frequency present. Secondly, the harmonic balance method is a powerful technique for the analysis of high-frequency nonlinear circuits such as power amplifiers, mixers and oscillators. It is well-suited for simulating analogue RF and microwave circuits, since these are naturally handled in the frequency domain. In this work, the harmonic balance method is used to perform power amplifier load-pull contour analyses. Fig. 3.11 shows the circuit schematic used in obtaining the optimum load impedance. The reflection coefficient that is looking into the Gate of the transistor has been configured only at fundamental frequency according to simulated input impedance matching as shown in Fig. 3.6. Besides, the reflection coefficients that are looking into the Drain of the transistor will be configured only at the 2nd harmonic and 3rd harmonic frequencies. Note that device NEC NE722S01 will be used in this load-pull analysis and the same technique applied for any devices as well. With all the specified user-defined parameters (reflection coefficient) at both input and output tuners together with an input power of 10 *dBm* maintained as constant, basically this procedure will be sweeping the load in order to find the best potential load impedance at the fundamental which could give maximum Power Added Efficiency (PAE) and maximum Total Power (PT). The value of this potential load impedance will be used to design aperture coupled antenna for direct integration later on.

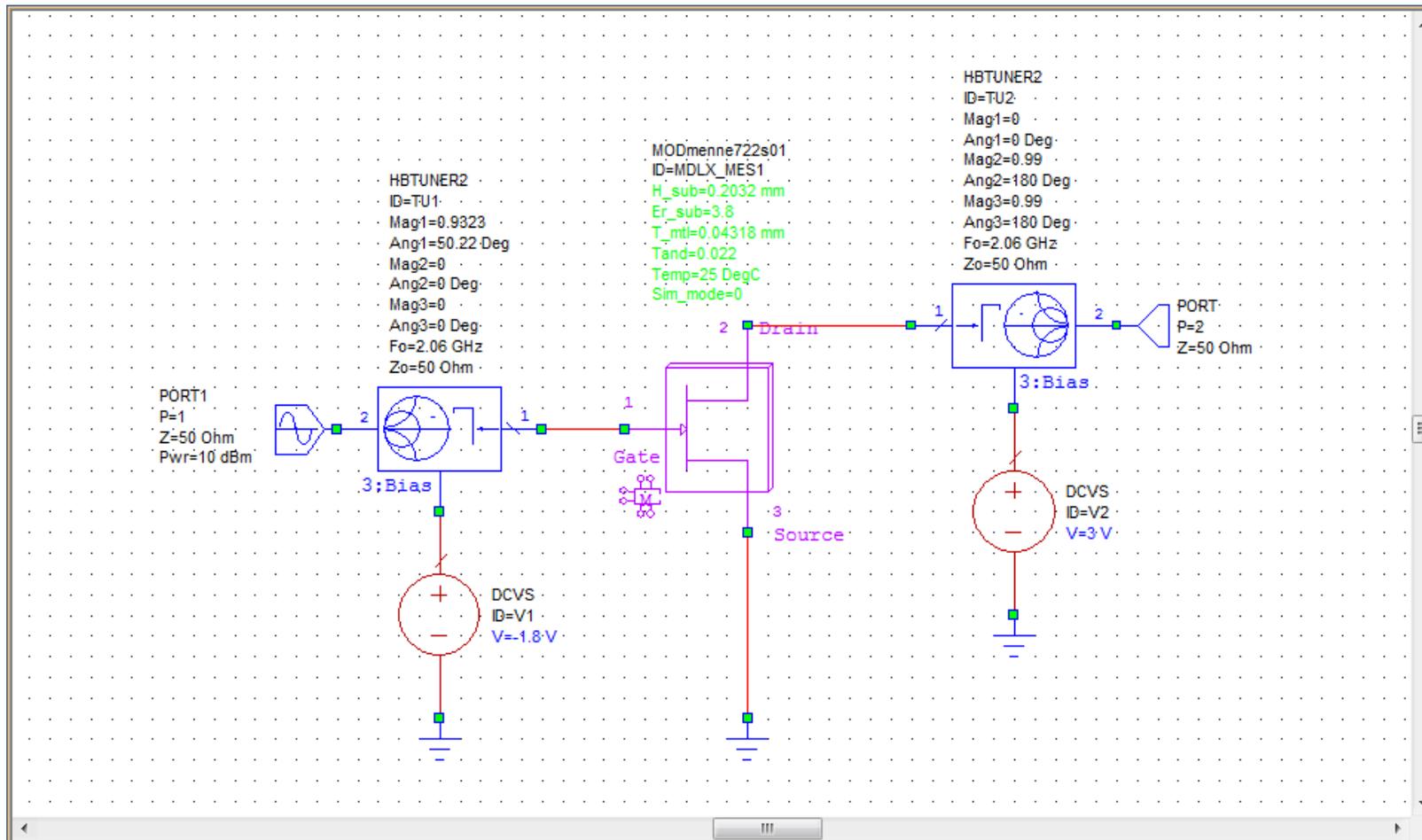


Fig. 3.11: Load-pull circuit configuration.

The next step is to optimise load impedance Z_{load} for maximum output power. The maximum output power here is actually referring to simulated measurements of Total Power (PT) delivered at the output port and Power Added Efficiency (PAE). A lossless network incorporating a Bias Tee is used, which transforms the impedance at its port 2 into a user-defined impedance at its port 1. As a Class B amplifier, it required harmonic short at the output up to the third harmonic. Therefore, the second and third harmonic reflection coefficients are set to be $\Gamma_{2f_o} = \Gamma_{3f_o} = 0.99\angle 180^\circ$. Since the reflection coefficient at the fundamental frequency Γ_{f_o} is going to be swept, the start value for the reflection coefficient in the schematic can be anything, as seen in the example shown in Fig. 2.11; it is set to be default which is $\Gamma_{f_o} = 0\angle 0^\circ$. Note that all user-defined parameters mentioned above are specified for the lossless HBTUNER2 TU2.

A simulated output power measurement is performed to plot the contour. Since the contour is in two dimensional (2-D), there should be only one measurement value for each of output impedance point, and this is set to be at the frequency of interest, $f_o = 2.06\text{ GHz}$. Note that the simulation sometimes will fail to converge at certain output impedance points. This is due to non-linearity of the transistor becomes severe as the fundamental input impedance $\Gamma_{f_o} = 0.9323\angle 50.22^\circ$ has been set in the first place to cause the maximum Gate voltage swings, hence making the Drain current reach its maximum. Generally, a convergence failure happens in highly non-linear transistor simulation due to converged impedances point density. In order to avoid the convergence failure, the converged impedance point density needs to be reduced. As a result, a rough contour at first attempt load-pull analysis which indicates the optimum load impedance can be plotted as shown in Fig. 3.12.

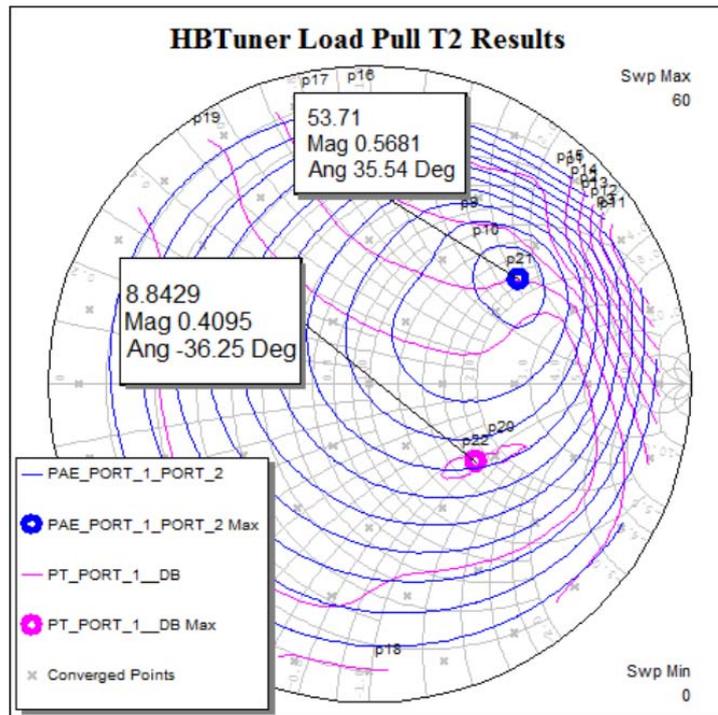


Fig. 3.12: Rough contour on the Smith chart at first attempt load-pull analysis.

Based on the coarse contour shown in Fig. 3.12, impedance at p22 might be able to deliver about 8.8 dBm total power for the system. In order to get more accurate estimation of the load impedances for the maximum achievable PAE and PT, another load pull analysis is performed with a refined converged impedance points that focus at where the optimum load impedances of maximum PAE and PT might be. Fig. 3.13 shows a refined sweeping region of the converged impedance points and the result for this load pull analysis is shown in Fig. 3.14. As can be seen in Fig. 3.14, a much smaller contour indicates p23 to deliver 17.25 dBm which is 8.4 dB more output power than the first attempt of load-pull analysis. At this stage, any point on the contour could be chosen as the optimum load impedance which is able to give high PT, PAE or good compromise between PT and PAE depending on the designer's specification.

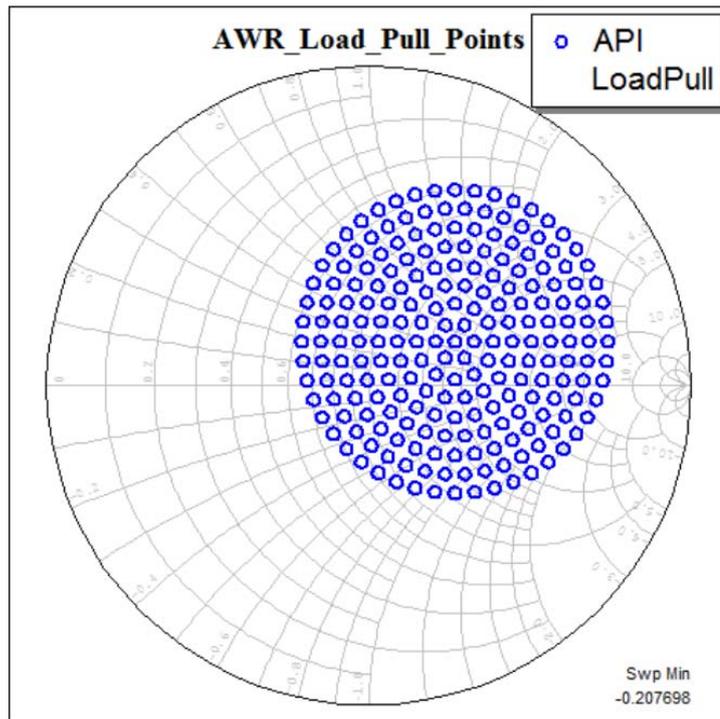


Fig. 3.13: Shrunk sweeping region of converged impedance points.

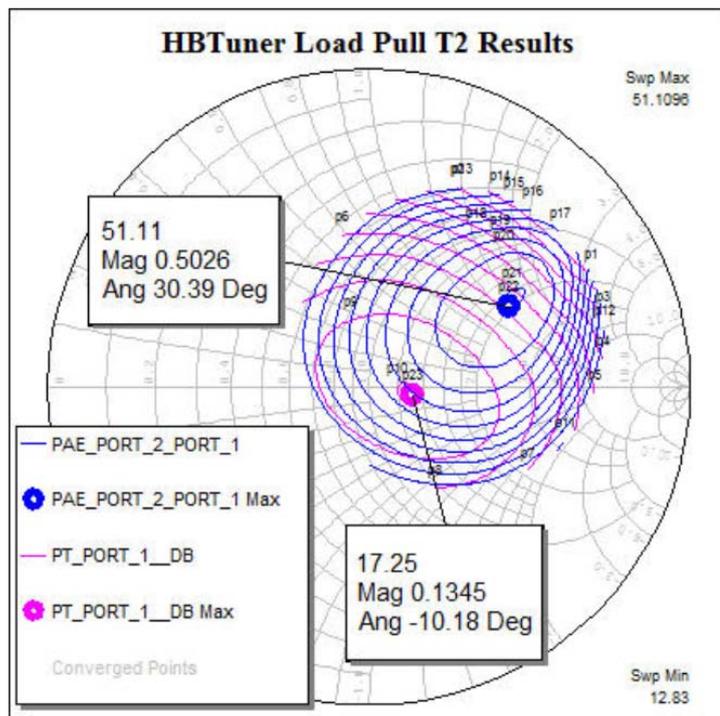


Fig. 3.14: Second attempt load-pull analysis with shrunk sweeping region.

3.5.4 Integrated Biasing and Matching Networks

There are several design variants for matching networks. In this work, the choice of a matching network is limited by parameters such as design variables and the availability of components. A point that has been chosen for optimum load impedance is substituted in HBTUNER2 as seen in Fig. 3.15. It shows one possible configuration of an integrated biasing and matching networks based on ideal components. In addition, these networks play an important role in establishing stable operation. Basically, as for the matching networks, according to Tian He in [93], there should be a capacitor in series at the Gate and Drain terminals respectively in order to avoid the DC current to flow into the source and load. Meanwhile, the harmonic trap lies at the load side of the transistor which present an open circuit at design frequency 2.06 GHz, and a short circuit at certain harmonics. Therefore, it would be only the fundamental frequency power is transmitted [93]. All the parameters mentioned above which include the input matching impedance at the fundamental ($\Gamma_{f_0} = 0.9323\angle 50.22^\circ$), harmonic terminations ($\Gamma_{2f_0} = \Gamma_{3f_0} = 0.99\angle 180^\circ$) and load impedance ($\Gamma_{f_0} = 0.1345\angle -10.18^\circ$) that capable of delivering highest total power were represented as being incorporated into the HBTUNER2.

Note that this configuration is only valid for a constant input power which maintained at 10 *dBm*. Besides, the implied bias decoupling networks used here are ideal. In any real circuit implementation, it would be necessary to simulate the effect of bias decoupling networks on the stability.

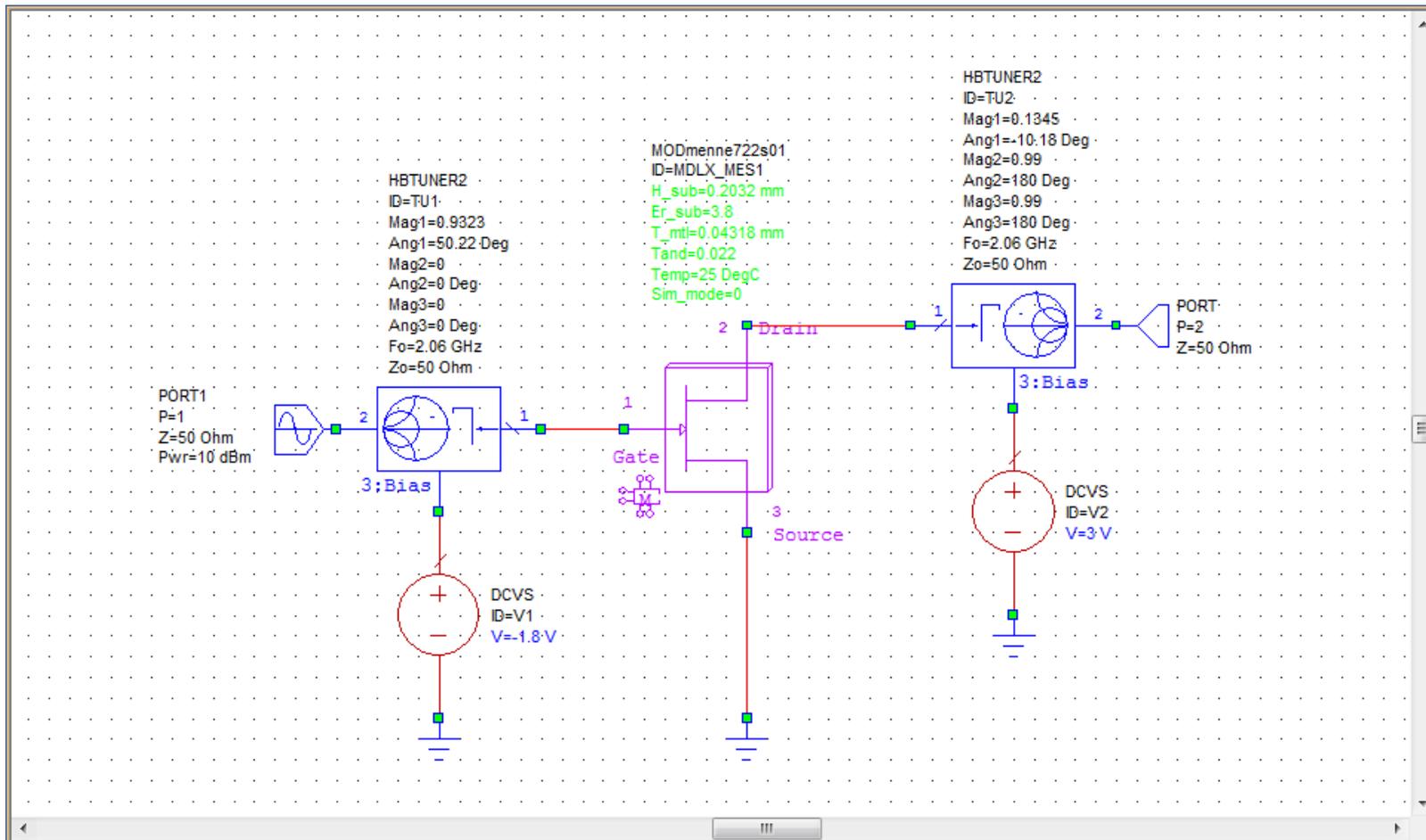


Fig. 3.15: Configuration of single-ended Class B power amplifier.

3.5.5 Power Splitter and Combiner

Fig. 3.16(a) shows details of what is in the SubCKT while Fig. 3.16(b) shows the ideal configuration of push-pull transmitting amplifier where SubCKT is actually a sub-circuit of single-ended power amplifier without harmonic terminations. Two 180° hybrids have been used in this push-pull configuration. One of them is used as a power splitter at the input side while the other one is used at the output side as power combiner. This configuration enables a pair of single-ended power amplifiers to be incorporated into an amplifier using the push-pull principle of operation. In Fig. 3.16(b), the red-dashed line is a point where the current waveform of a Class B push-pull transmitting power amplifier with harmonic filtering up to 3rd harmonic is verifiable by observation through simulation. The simulated current waveform at this particular point is shown in Fig. 3.17. It is found that there are many ripples due to higher order harmonics. The theory to support the assertion that those ripples are caused by higher order harmonics will be given in the next section. Ideally, the current and voltage waveforms should be viewed at the device plane, by de-embedding a full package model, as a means of determining whether true Class B mode of operation has been achieved. Without a full package equivalent circuit model, this was not possible. However, the current waveform seen at the output plane gives an indication of Class B operation with additional current ripple associated with harmonic displacement currents, mainly into C_{ds} in the transistor model.

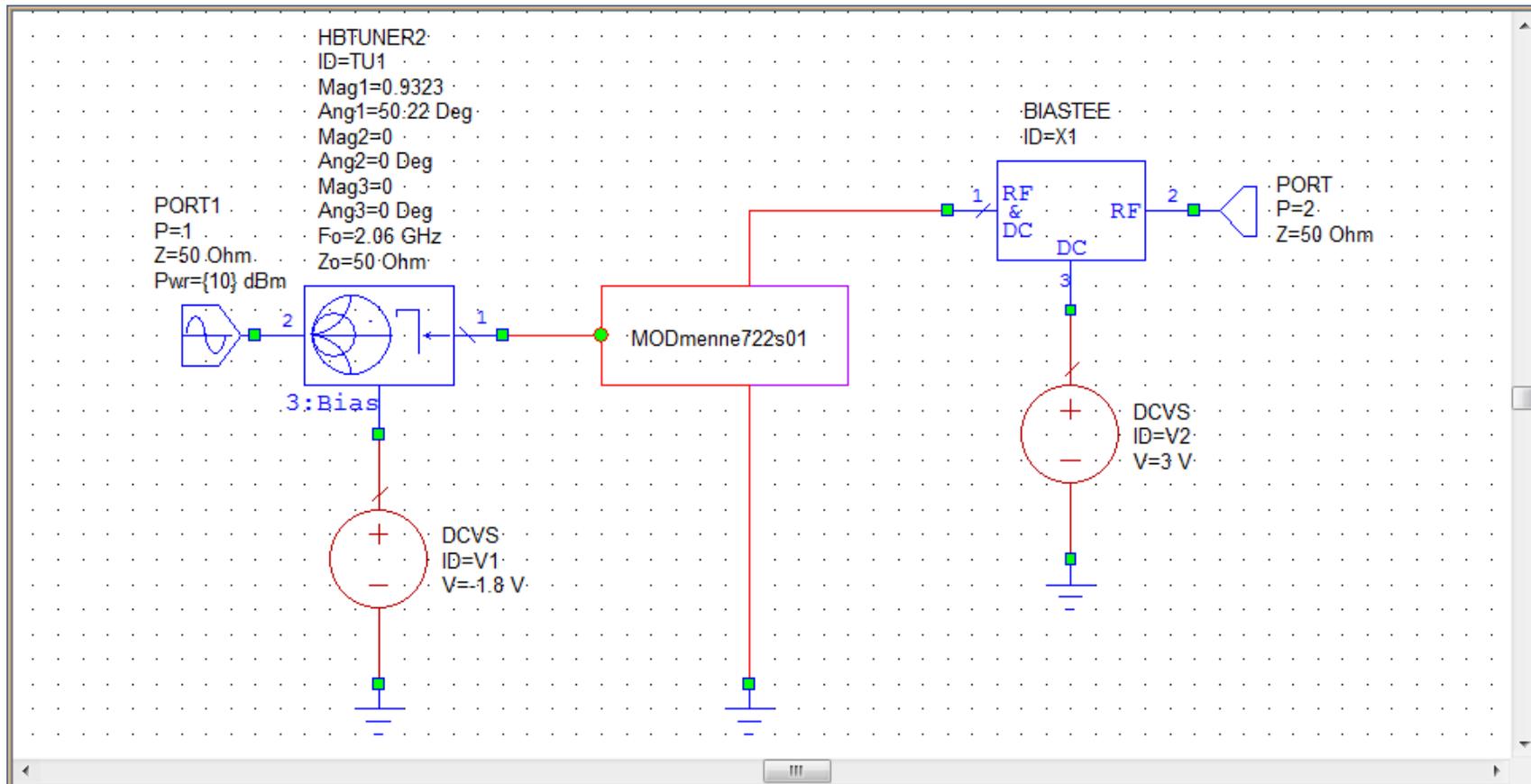


Fig. 3.16(a): Single-ended power amplifier without harmonic terminations.

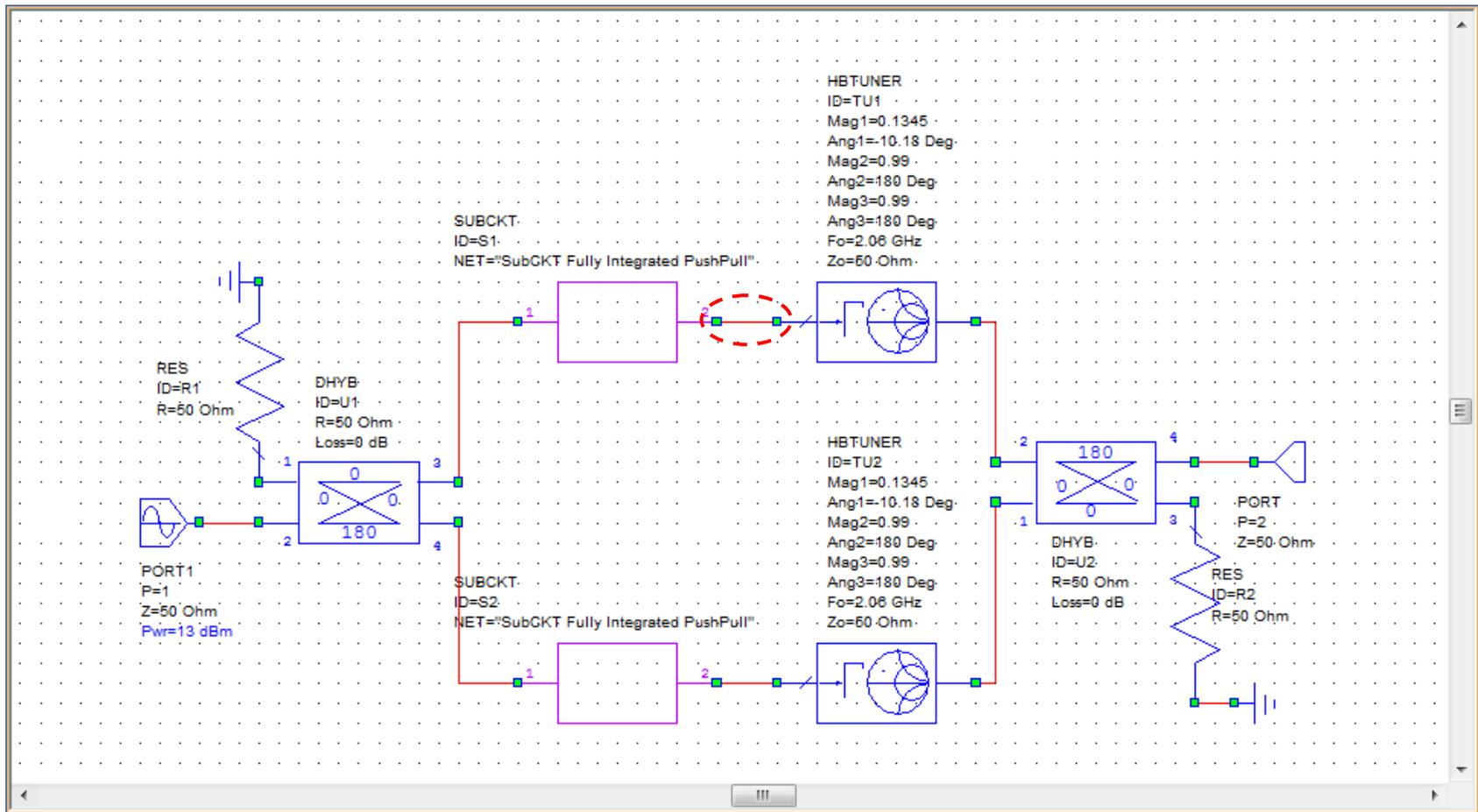


Fig. 3.16(b): Ideal configuration of push-pull transmitting power amplifier with harmonic filtering up to 3^{rd} harmonic.

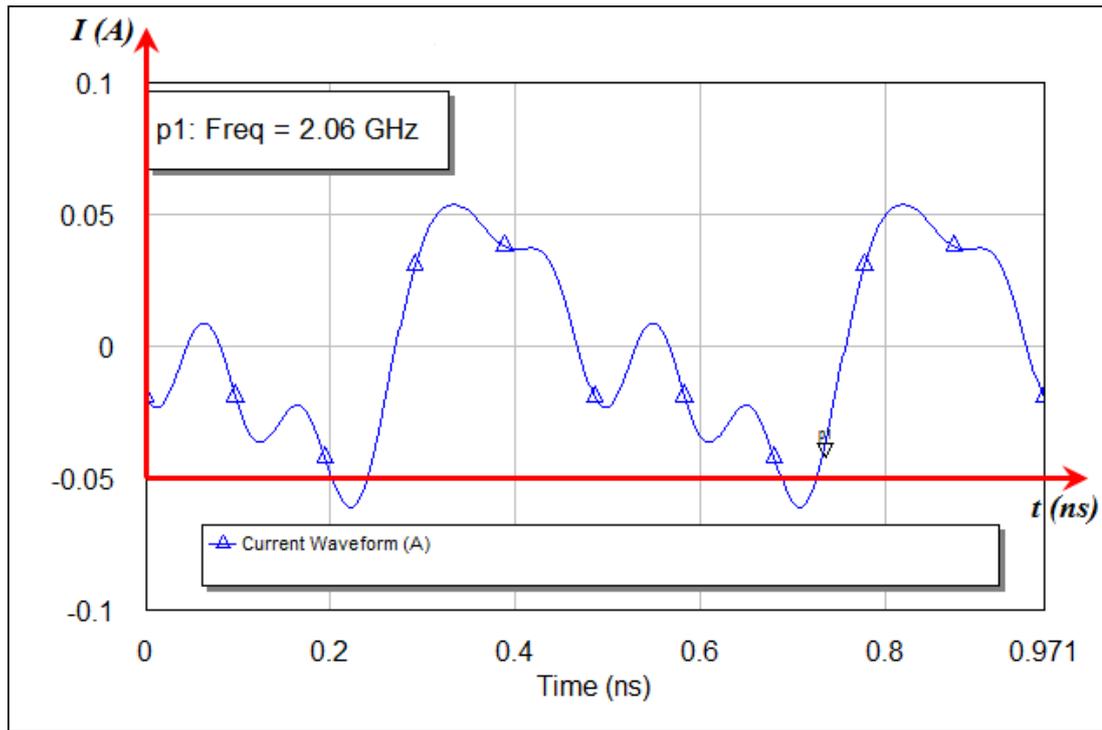


Fig. 3.17: Waveform of a Class B power amplifier with up to 3rd harmonic suppressed.

3.5.6 Optimisation with Lossy Components

The final version of circuit schematic for the prototype in simulation will be replaced with the realistic lossy components. The elements which need to be replaced with lossy components include the input stage power splitter with 180° phase shift, the bias decoupling circuits, the output stage HBTUNER2, the output power combiner. The input power splitter will be represented in a form of Wilkinson splitter and phase shifter while bias decoupling circuits will be realised using lumped elements and microstrip lines. Furthermore, a differentially fed microstrip antenna using aperture coupled technique incorporating the output matching networks into the combined filters and power combiner will replace the use of the output stage

HBTUNER2 and 180° hybrid in an ideal configuration. All of the above elements except for the input Wilkinson splitter and phase shifter will be integrated on the antenna structure, hence, becoming a 2-port multilayer active integrated antenna. However, this would require further tuning and optimization, the details of which are covered in the next chapter.

3.6 Effect of Higher Order Harmonics Filtering

Earlier in the previous section, it has been mentioned that only up to 3rd harmonic is taken into consideration in the design procedure. This section will show the effect of higher order harmonics filtering when those higher order harmonic traps are being employed in a push-pull configuration through simulation. Fig. 3.18(a) shows the configuration of push-pull transmitting power amplifier with integrated harmonic traps up to 7th order. Fig. 3.18(b) shows the details of the harmonic trap sub-circuits for the 4th and 5th harmonics while Fig. 3.18(c) shows for the 6th and 7th harmonics. As can be seen in Fig. 3.19, most ripples that have appeared before employing further harmonic traps are well reduced. This generally supports the assertion that those ripples are caused by higher order harmonics such as 8th, 9th and so on so forth. However, the residual ripple shown in Fig. 3.19 does not give significant interference impact on the overall system performance. In fact, the 8th, 9th and other higher harmonics are considered separated by a quite far distance from the desired operating frequency.

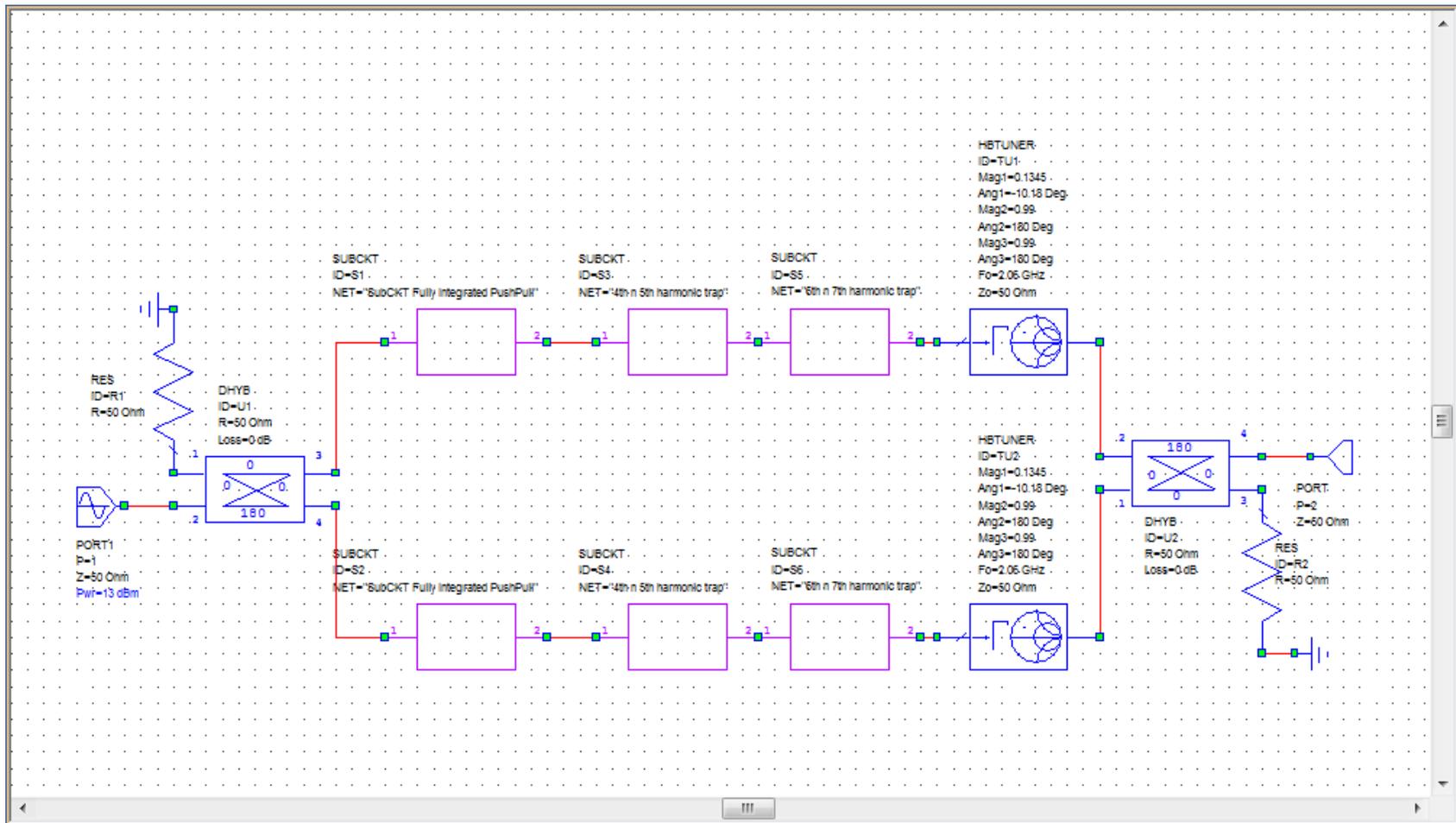


Fig. 3.18(a): Push-pull power amplifier with integrated higher order harmonic traps.

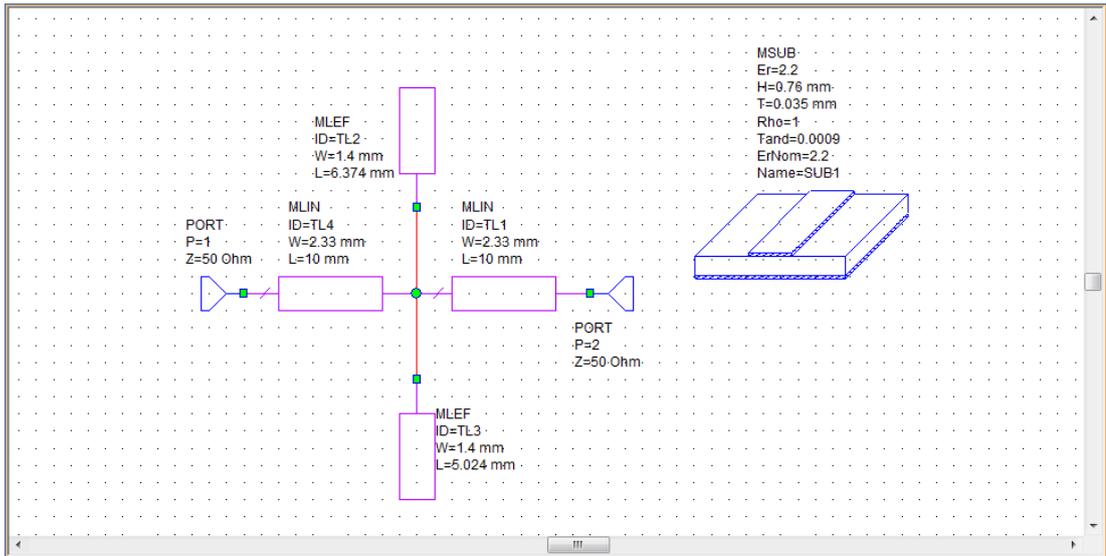


Fig. 3.18(b): The 4th and 5th harmonic trap subcircuit.

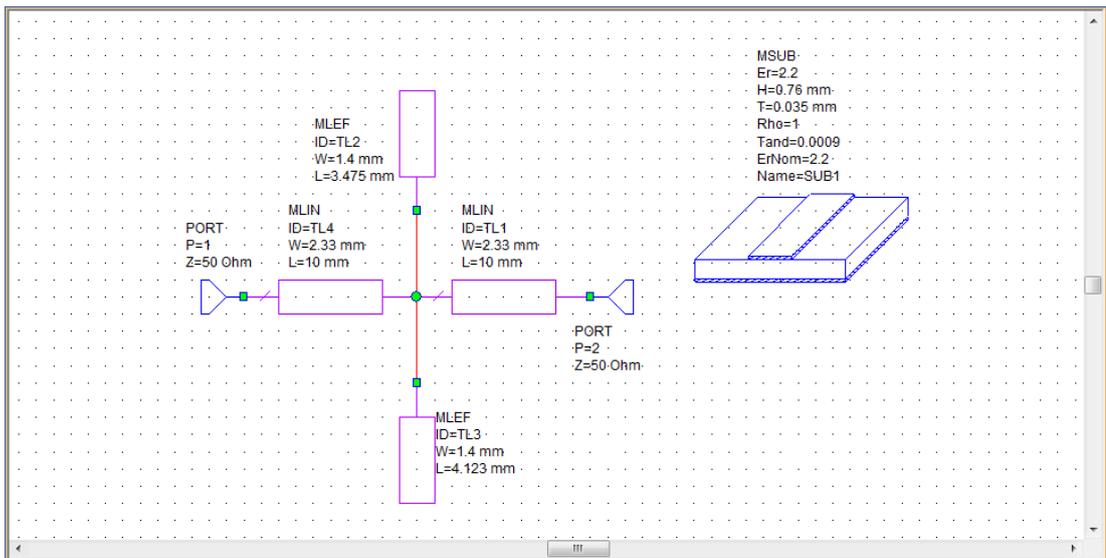


Fig. 3.18(c): The 6th and 7th harmonic trap subcircuit.

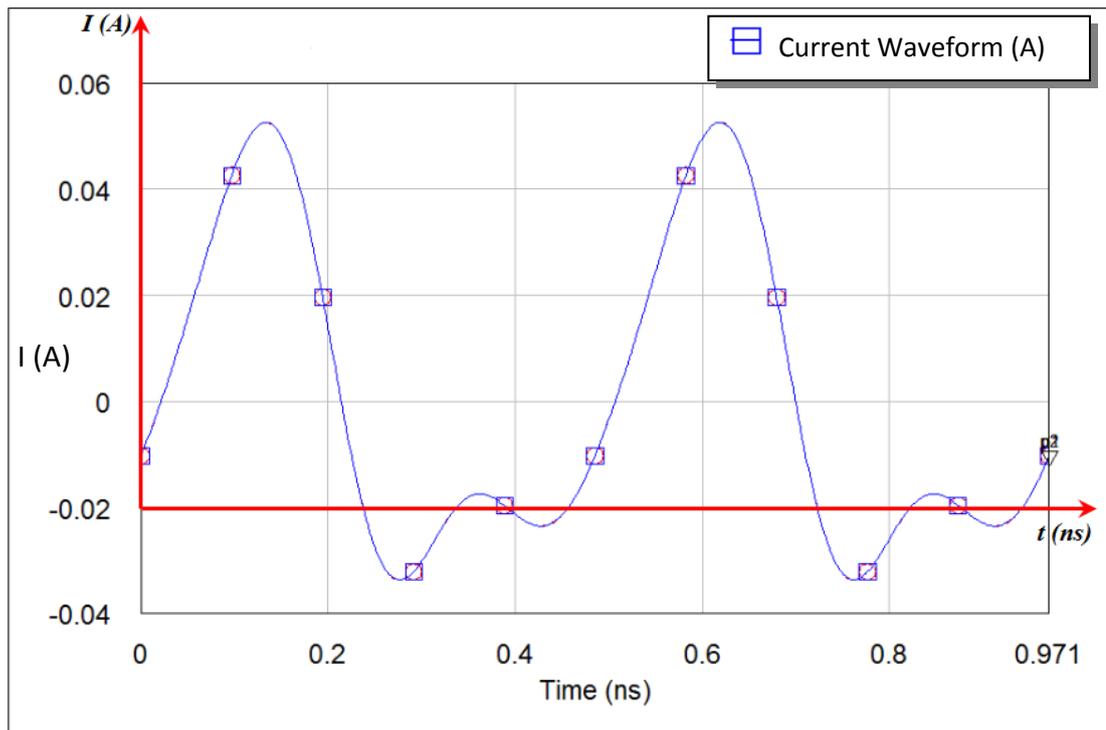


Fig. 3.19: Waveform of a Class B power amplifier with up to 7th order harmonic suppressed.

3.7 Summary

First and foremost, the history of push-pull output has been briefly introduced and the operation of a push-pull power amplifier well as its design architecture was generally explained. Besides, two research design flow charts which cover two different designs which are push-pull Class B power amplifier and EM structure; aperture coupled patch antenna are presented. An investigation of the effect of higher order harmonics filtering in a push-pull configuration was also presented.

The design procedure based on the research flow charts and the simulation technique for a single-ended power amplifier as well as the implementation of push-pull power amplifier configuration has been presented and explained in details. Two different types of transistor were proposed to undertake the load pull analysis as a single-ended power amplifier which are NEC NE722S01 Low Noise / Low Power MESFET and NITRONEX NPTB00004 RF Power GaN HEMT. These two active devices have been used separately in a push-pull circuit configuration and the simulated results are compared in terms of theoretical maximum achievable Power Added Efficiency (PAE) as well as their Total Power (PT). The simulated load-pull analysis example shown in this chapter is using NEC NE722S01 as amplifier. The same sequence of procedures applies on the analysis for the transistor NPTB00004 but it is not shown in this thesis.

CHAPTER 4

DIFFERENTIALLY FED APERTURE COUPLED ANTENNA FOR PUSH-PULL TRANSMITTING AMPLIFIER

4.1 Introduction

The history of push-pull output and the design architecture of push-pull power amplifiers has been briefly described and explained in chapter 3. Besides, there are research design flow charts that have covered two different designs which are push-pull Class B power amplifier and differentially fed aperture coupled microstrip antenna. The most important part which has been thoroughly explained in the previous chapter was the design procedures. Apart from that, an investigation into the effect of higher order harmonics filtering in a push-pull configuration also is demonstrated through simulation.

This chapter describes a novel optimum power combiner adapted from an aperture coupled technique, in which differential signals from a transmission line are spatially coupled to an antenna structure via an aperture for a push-pull transmitting power amplifier configuration. A differential feed network is used to generate maximum current, or a virtual short circuit in the middle of the narrow aperture under the patch antenna.

Two differentially fed multilayer antenna designs will be presented. The first uses the power combiner concept applied in a push-pull transmitting amplifier using transistor NEC NE722S01 Low Noise / Low Power MESFET. Secondly, the same concept is applied to another transistor, the NITRONEX NPTB00004 RF Power GaN HEMT in which a reduced size and compact version of push-pull amplifier-antenna module is obtained.

Furthermore, there are parametric studies on the existing design variables for two different slot / aperture designs. These explain more about the technique in order to set the odd-mode fundamental frequency impedance to a value required for the class B load-line of a given transistor which effectively incorporates the output matching circuit into the combined filters, power combiner and differentially fed aperture.

4.2 Differential Aperture Coupling Technique for Push-pull Transmitting Amplifier

This section will briefly explain the principle of operation of a single fed aperture coupled microstrip patch antenna. This is then followed by introducing the designs of two types of differentially fed aperture coupled passive antennas based on the odd-mode fundamental frequency impedance requirement of a given transistor. Both were designed and simulated with a finite ground plane using CST Microwave Studio (CST MWS) with the assistance of AWR Microwave Office software and the

prototypes were fabricated for measurements. One design is realised with the integration of double-ended Class B power amplifier to form a push-pull transmitting amplifier configuration. These two types of differentially fed aperture coupled passive antennas are labelled as *Structure A* and *Structure B* respectively. Structure A is designed for 50Ω odd mode impedance, while Structure B gives the freedom to choose arbitrary odd mode impedance.

Fig. 4.1 shows an example of an ideal configuration of a push-pull transmitting power amplifier which is used in the following sub-sections. More generally, Fig. 4.1 suggests the idea of replacing a circuit within the red dashed-line block with proposed Structure A and Structure B.

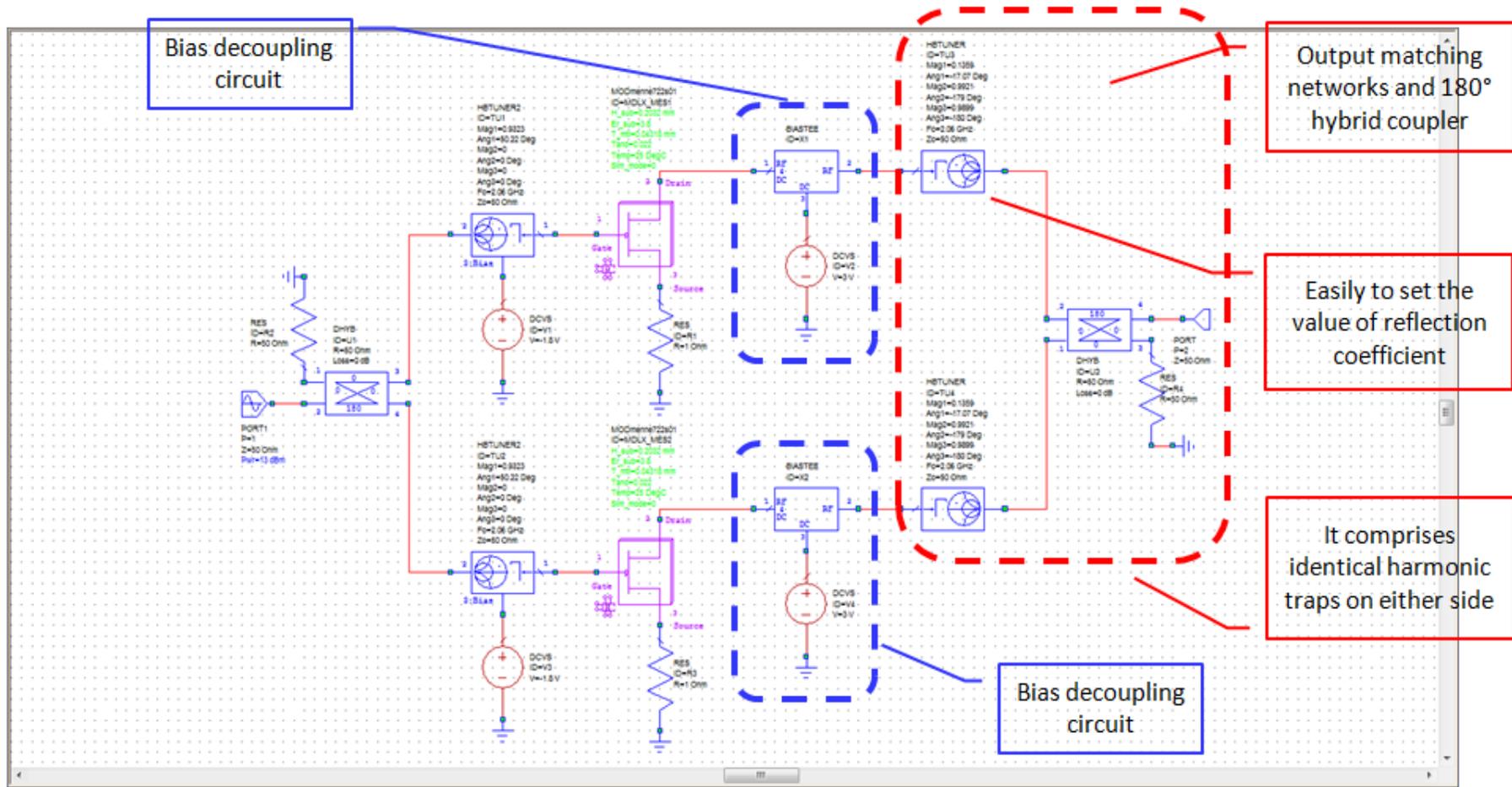


Fig. 4.1: Ideal configuration of push-pull transmitting power amplifier.

4.2.1 Concept of Single Fed Aperture Coupled Antenna

The previous section briefly discussed the concept of microstrip-fed slot antenna with a $\lambda/4$ stub in which it has particular shared characteristics with that of aperture coupled antenna. The single fed aperture coupled antenna uses an extended microstrip line with approximate length of $\lambda/4$ beyond the edge of slot/aperture and terminated in an open-circuit, as first demonstrated by Pozar [71]. This is actually creating an effective virtual short-circuit in the middle of the slot/aperture where the current is maximum. As a result, the maximum strength current is electromagnetically coupled to the microstrip patch antenna upon top of it. The aforementioned concept of antenna feeding technique makes use of the open-short circuit transmission line theory [94]. Fig. 4.2 shows a terminated lossless transmission line with the length, ℓ .

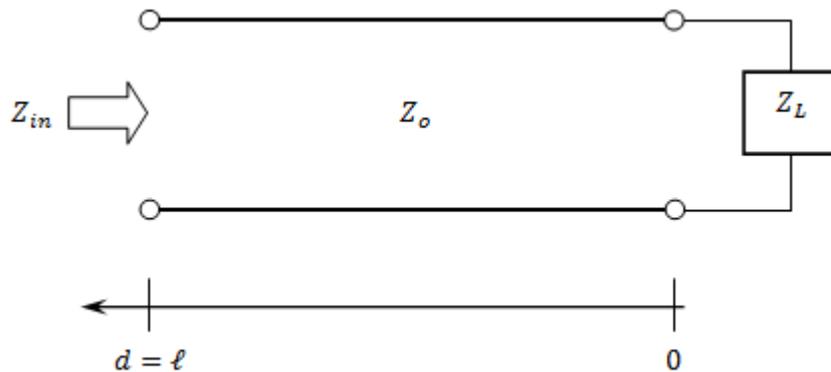


Fig. 4.2: A lossless transmission line terminated in the impedance Z_L .

At a distance, $d = \ell$, from the load with impedance Z_L , the input impedance Z_{in} given by the expression is

$$Z_{in}(\ell) = Z_o \frac{Z_L + jZ_o \tan(\beta\ell)}{Z_o + jZ_L \tan(\beta\ell)} \quad (4.1)$$

Let the load impedance, $Z_L = \infty$ (open-circuit condition). Hence, (4.1) becomes

$$Z_{in}(\ell) = -jZ_o \cot(\beta\ell) \quad (4.2)$$

When a distance from the load, $\ell = \frac{\lambda}{4}$, thus

$$Z_{in}\left(\frac{\pi}{2}\right) = -jZ_o \cot\left(\frac{\pi}{2}\right) = 0 \quad (4.3)$$

Equation (4.3) shows that at a distance of $\lambda/4$ from the microstrip line end (open-circuit), the input impedance $Z_{in} = 0$ which indicates the current intensity at this point is maximum, effectively creating a virtual short circuit, thereby allowing strong coupling of electromagnetic energy to the patch antenna via an aperture. The separated layers perspective of a single fed aperture coupled microstrip antenna with an open-circuit stub is shown in Fig. 4.3.

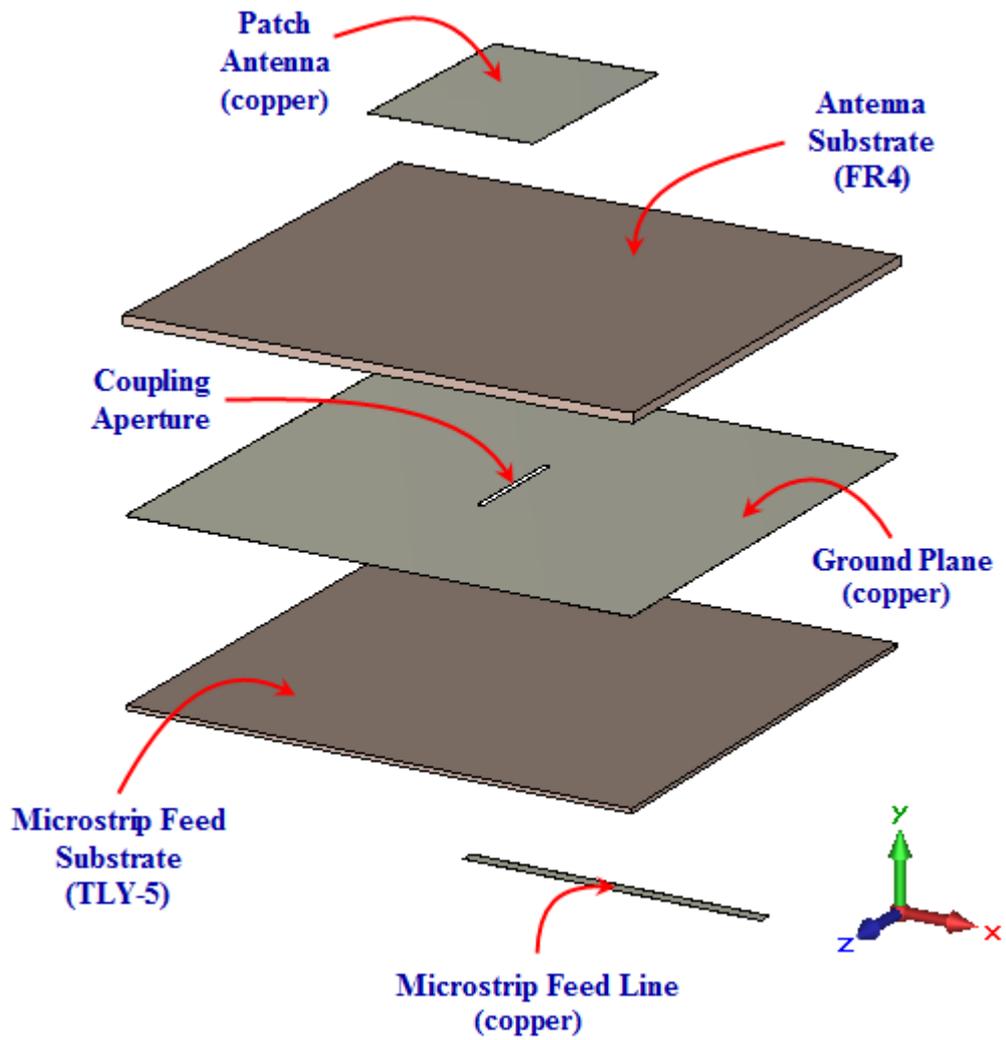


Fig. 4.3: Separated layers of a single fed aperture coupled microstrip antenna.

4.2.2 50Ω Differential Input Version

The differential fed aperture coupled half-wavelength patch antenna was designed as shown in Fig. 4.4 and it has resonance at $f_o = 2.062$ GHz. In this structure, the top layer consists of an FR-4 substrate ($H_1 = 1.6$ mm, $\epsilon_{r1} = 4.4$, $W_{sub} = L_{sub} = 100$ mm) with the rectangular patch antenna ($W_p \times L_p = 37 \times 28$ mm) etched on it. The bottom layer as shown in Fig. 4.4 is another substrate from Taconic TLY-5

($H_2 = 0.8$ mm, $\epsilon_{r2} = 2.2$, $W_{sub} = 100$ mm, $LL_{sub} = 285.4$ mm) supporting the ground plane with a slot ($W_a \times L_a = 20 \times 1$ mm) sandwiched between these two substrates. The microstrip feed line is etched on the bottom layer.

In this study, an external Class B (NEC NE3210S01 PHEMT) push-pull power amplifier was used to generate the differential signals to drive the aperture coupled antenna using a concept first mentioned in [95]. Theoretically, when the out-of-phase signals are fed into the two ends of microstrip feed line, a virtual short circuit ($V = 0V$) or maximum current (I_{max}) is formed in the middle of that microstrip feed line [96]. Thus, electromagnetic energy is efficiently coupled from the aforementioned microstrip feed line to the patch antenna via a single aperture or slot.

The push-pull class B amplifier configuration uses a differential feeding technique. Therefore, this technique is used to demonstrate the fruitful use of a new proposed power combiner adapted from the previous aperture-coupled differential antenna structure published in [95, 96]. This approach has the potential to achieve increased efficiency and improved battery life for wireless systems. This structure differs from the previous aperture-coupled technique in that it comprises identical harmonic traps on either side of the aperture, using resonant stubs to form bandstop filters (BSF).

Since the amplifiers are integrated, harmonic terminations should be taken into consideration. Hence, bandstop filters were designed in order to control the harmonics. In this study, only 2nd ($2f_o$) and 3rd ($3f_o$) harmonics were taken into account. The bandstop filters (BSF) employed in the configuration as shown in Fig.

4.5, will cause a further mismatch at fundamental (f_o). Therefore, the 50Ω lines which are connected to the both ends of microstrip feed line need to be optimised and neatly tuned by adjusting their electrical length in order to use the filter's susceptance to match the antenna.

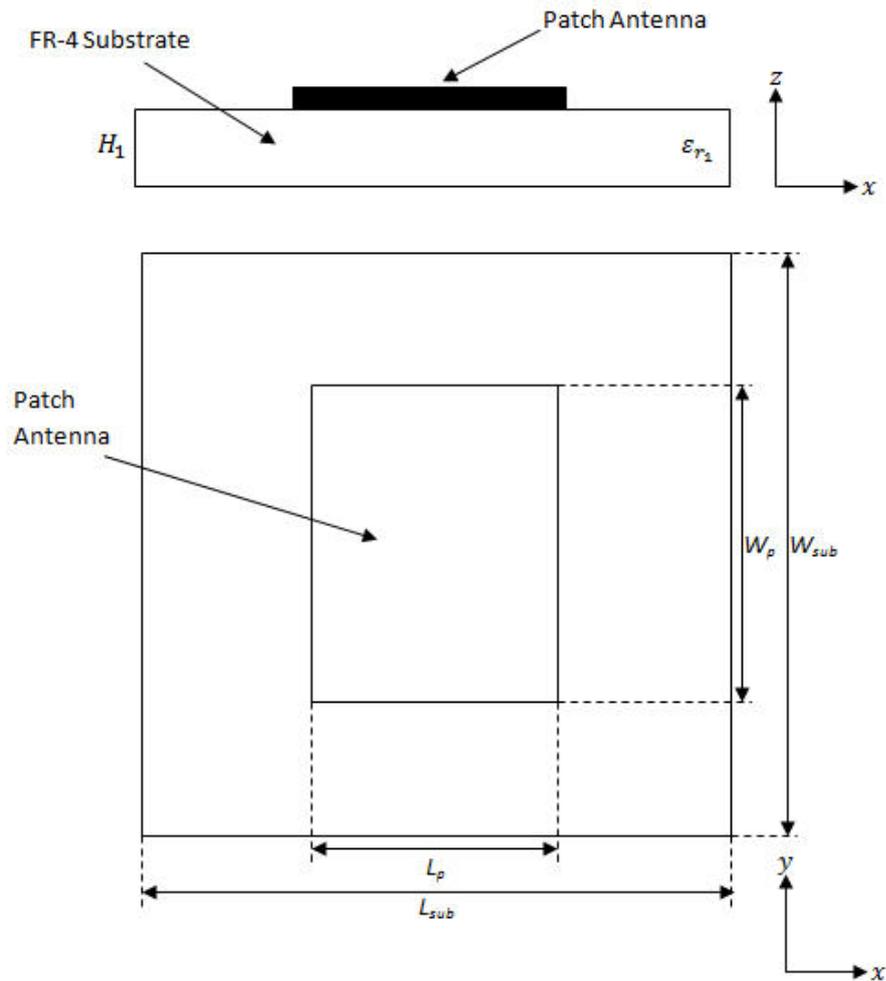


Fig. 4.4: Layout of Structure A (top layer).

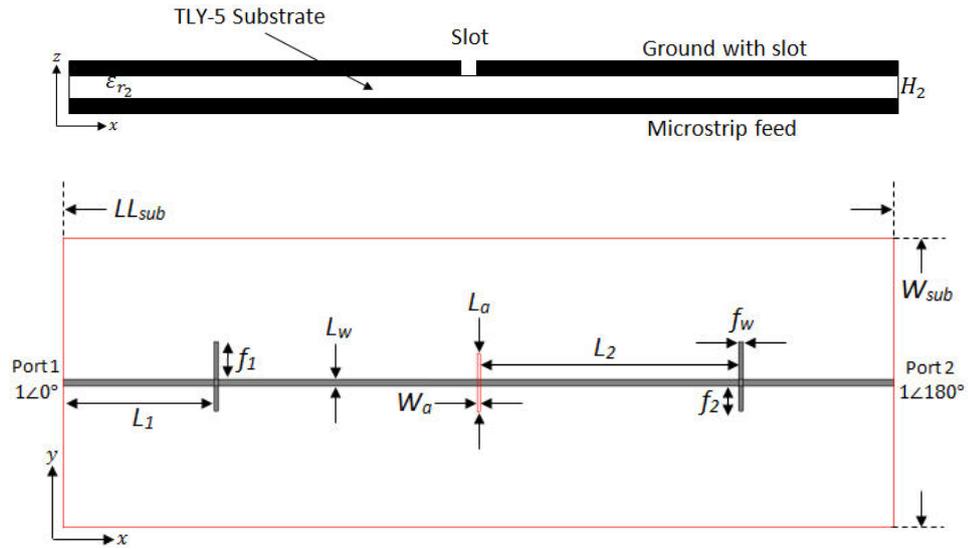


Fig. 4.5: Layout of Structure A (bottom layer).

In this structure, two open-circuit stubs act as the harmonic traps with different lengths which are $f_1 = 12.975\text{mm}$ ($\lambda/4$ at $2f_0$) and $f_2 = 8.595\text{mm}$ ($\lambda/4$ at $3f_0$) respectively and the same width, $f_w = 1.4\text{mm}$. The line length $L_1 = 51.925\text{mm}$, $L_2 = 89.375\text{mm}$ and $L_w = 2.33\text{mm}$. The line length L_1 should provide 180° phase compensation in the electrical length so that the reflection coefficient at the respective harmonics will be seen like a short circuit (Magnitude = 1, Angle = 180°). The line length L_2 is an optimised 50Ω line length to ensure the fundamental (f_0) at its best state whereas for this case, the lowest possible reflection magnitude is close to zero (Magnitude = 0) is desired to be achieved. This is unlike the previous differentially fed aperture coupled active antenna whereby no harmonic trap was integrated within the circuit configuration. It was just active devices were simply integrated with the aperture coupled antenna without taking into consideration the harmonic impedances presented to the non-linear devices.

The following will present the simulation results of the previous structure which is using aperture-coupled technique without harmonic termination and our new proposed structure adopted from aperture-coupled technique with built-in harmonic termination using Band Stop Filter (BSF). As can be seen in Fig. 4.6, at fundamental frequency ($f_o = 2.062 \text{ GHz}$) the reflection magnitude is not even close to zero (mismatched). Although it was mentioned in [12] that the aperture-coupled antenna structure is like a matching network and 0 dB power combiner, but still the reflection coefficient at the fundamental is considered very poor. Also from Fig. 4.6, the reflection coefficient at harmonics ($2f_o = 4.124 \text{ GHz}$ and $3f_o = 6.186 \text{ GHz}$) does not show any signs of perfectly suppressed ($0.99 \angle 180^\circ$).

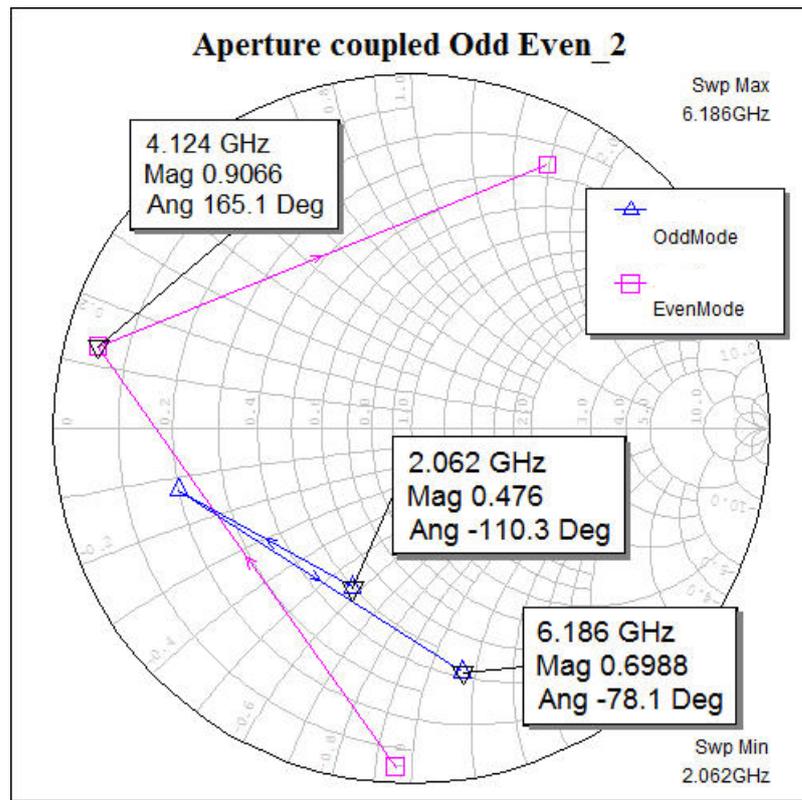


Fig. 4.6: Simulation results of the structure without harmonic termination.

In Fig. 4.7, a good match at fundamental is achieved where the reflection coefficient magnitude is almost equal to zero. The 2nd ($2f_0$) and 3rd ($3f_0$) harmonics were suppressed perfectly as they were seen like a short circuit where both the magnitude and angle were close to unity and almost equal to 180° ($\approx 0.99\angle 180^\circ$) respectively. The improvement at fundamental frequency is achieved by adjusting L_2 while harmonic suppression is done by adjusting the line length L_1 . Overall, high efficiency amplifier design is about designing harmonic impedances so that waveforms ($0^\circ \leq \theta \leq 180^\circ$) are set up depending on which amplifier class that will enable high efficiency. As for this case, the power amplifiers should be working in class-B in which harmonic impedances required to be seen as short circuit ($0.99\angle 180^\circ$).

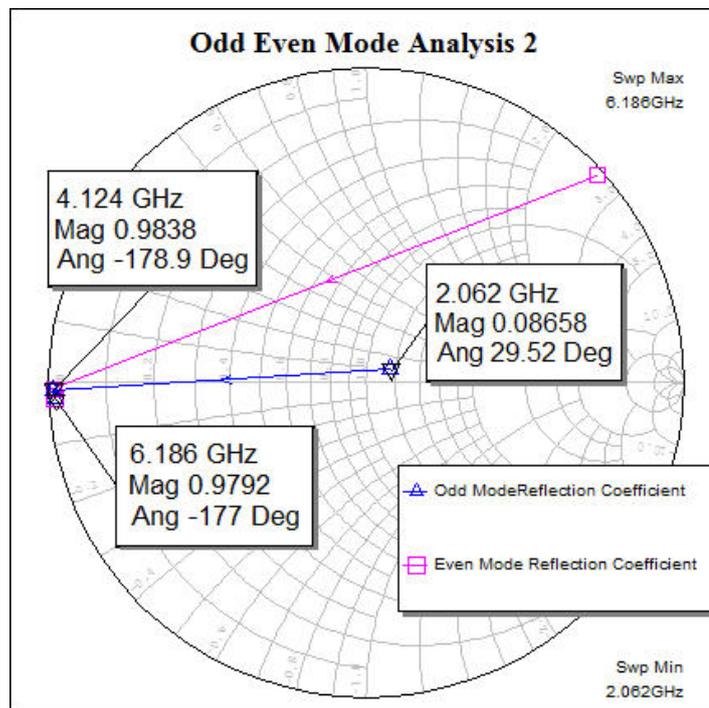


Fig. 4.7: Simulation results of the new proposed structure with built-in harmonic termination.

On the other hand, Fig. 4.8 shows the comparison between measured and simulated return loss of the structure with 50Ω differential input. A 2-port S-parameter measurement was conducted using Agilent 8720ES network analyzer and the odd-mode return loss, S_{odd} was obtained using Eqn. (2.14). This structure was originally designed at resonant frequency of 2.06 GHz. However, the measured result shows the resonant frequency is shifted up to 2.111 GHz, a 2.5% frequency shift from the simulated resonance. This frequency shift is due to the tolerances of dielectric constant from both substrates which are FR-4 and Taconic TLY-5.

Overall, the difference between the measured (2.111 GHz) and simulated (2.06 GHz) first resonant frequency amounts to an error of about 2.5%. Possible causes include:

- Tolerance in the dielectric constants of either or both substrates.
- Dimensional errors in etching the lines. Slight over-etching would be expected to push the frequency upwards, through reduced distributed capacitance.
- Alignment errors between the layers. Misalignment could push the frequency upwards by reducing interlayer capacitance
- Small air gaps between the layers, which would also be expected to increase the frequency by reducing the effective overall dielectric constant.

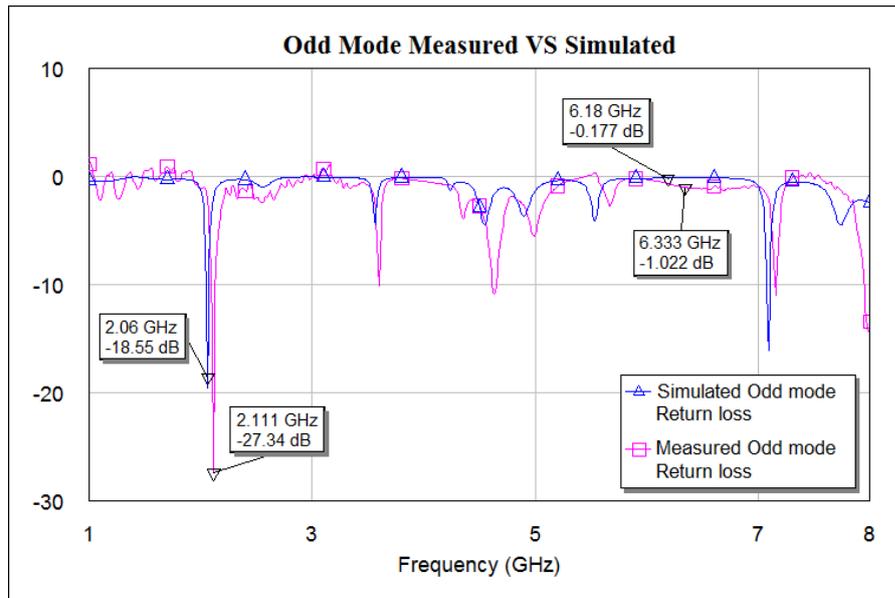


Fig. 4.8: Comparison of the odd mode return loss for Structure A.

Furthermore, Fig. 4.9 shows on a Smith chart the measured odd and even mode reflection coefficient at fundamental, 2nd harmonic and 3rd harmonic frequencies. The measurement results appear to have a good match at fundamental as the reflection coefficient magnitude is seen close to zero where the impedance is around 45.9 Ω when it is denormalized to 50 Ω . Besides, the 2nd and 3rd harmonics seem to have been considerably well suppressed since the reflection coefficient magnitude and their angle respectively are 0.831 \angle 177.1 $^\circ$ and 0.8888 \angle - 178.4 $^\circ$ which is close to unity and 180 $^\circ$. In terms of harmonic impedance, both 2nd and 3rd harmonics are considered of having reasonably small impedances. According to the Ohm's Law ($V = IR$), where I is a current when there is small resistance (R) / impedance (Z) exists, the voltage drops across that resistance / impedance will be almost equal to zero voltage ($V \approx 0 V$) and in some cases, this voltage can be simply neglected. Hence, the 2nd and 3rd harmonics are considered well suppressed since there is no voltage ($V \approx 0 V$) drops across them.

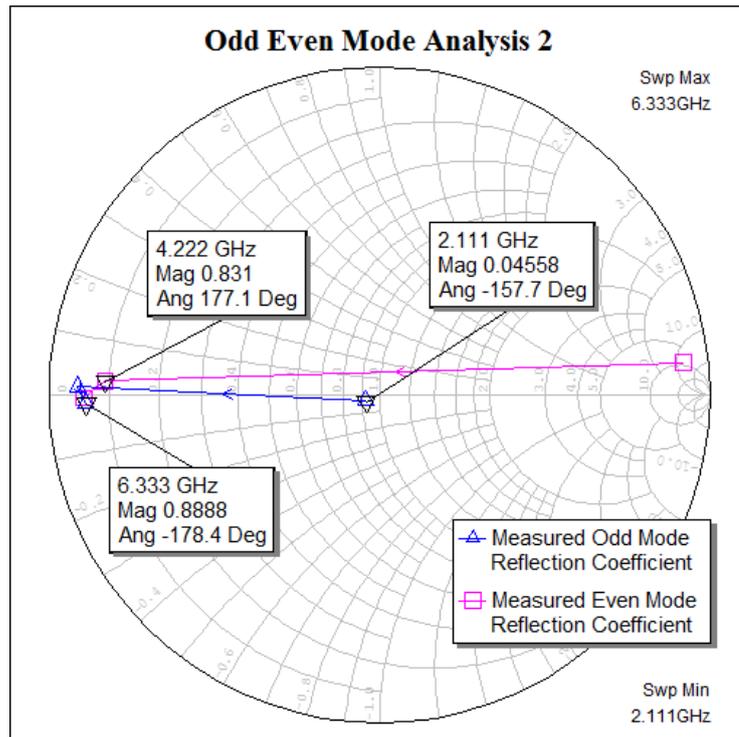


Fig. 4.9: Measured odd mode reflection coefficient of Structure A

4.2.3 Complex Arbitrary Input Impedance Version

The previous Structure A was purposely designed particularly to comply with the standard 50Ω environment. However, this unique advantage of universal connectability also has some drawbacks and it has been highlighted and explained in the previous Chapter 2. This section will present another design of a differentially fed aperture coupled microstrip antenna that involves a complex impedance requirement. This new proposed structure can be used to set the odd-mode fundamental frequency impedance to a value required for the class B load-line of a given transistor which is effectively incorporating the output matching circuit into the combined filters and power combiner.

Similar to Structure A, the design of Structure B used the same substrate material with the same properties such as thickness and dielectric constant for both top and bottom layers. The difference in Structure B is that it is a reduced-size version of Structure A, in which the optimised 50Ω line length L_1 and L_2 in Structure B are $\lambda/2$ shorter than that of Structure A where the line length $L_1 = 27.175$ mm and $L_2 = 13.875$ mm respectively. Besides, while keeping the original slot length, L_a as well as slot width, W_a in Structure A, the straight line slot is replaced by a new slot shape with added two slots ($LL_a = 6$ mm each), forming a cross shape.

In this structure, the top layer consists of an FR-4 substrate ($H_1 = 1.6$ mm, $\epsilon_{r1} = 4.4$, $W_{sub} = 80$ mm, $L_{sub} = 85.9$ mm) with the rectangular patch antenna ($W_p \times L_p = 37 \times 28$ mm) etched on it whereby the configuration is exactly as shown in Fig. 4.4 except with the dimensions mentioned above. The bottom layer as shown in Fig. 4.10 is another substrate from Taconic TLY-5 ($H_2 = 0.8$ mm, $\epsilon_{r2} = 2.2$, $W_{sub} = 80$ mm, $L_{sub} = 85.9$ mm) supporting the ground plane with a new cross shaped slot ($W_a = 1$ mm, $L_a = 20$ mm) sandwiched between those two substrates. The microstrip feed line is etched on the bottom layer. Again, note that as a Class B amplifier, it requires a harmonic short or Band Stop Filter (BSF) at the output side. These harmonic shorts are generated by the two open-circuit stubs with dimensions similar to those used in Structure A.

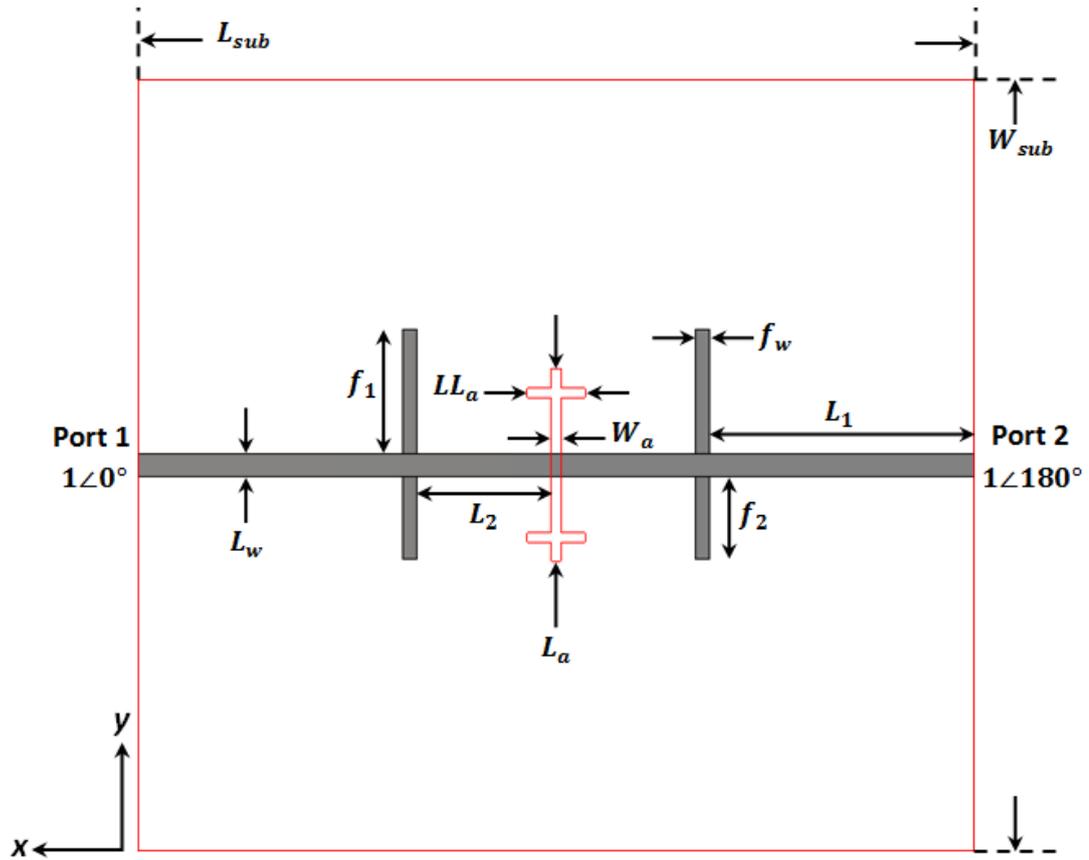


Fig. 4.10: Layout of Structure B (bottom layer).

The susceptance of the BSF elements is used in the fundamental frequency matching network by optimising the lengths of the 50Ω lines between the slot and the stubs. This new technique makes use of the odd-mode fundamental signal to generate maximum current under the antenna and efficiently couple the electromagnetic energy from a microstrip feed line to the antenna via an aperture or slot. The proposed design suppresses harmonic voltages at $2f_o$ and $3f_o$, whilst also optimising the load line impedance seen by the two amplifiers at the fundamental frequency in odd mode at f_o (2.06 GHz).

As can be seen in Fig. 4.10, the line length L_1 is a non-zero value in order to establish a proper microstrip mode before the junctions with the harmonics stubs. In order to provide a short circuit at the harmonics, the L_1 is either made 180° long or its effect is de-embedded in order to give impedance at the junction with the stubs. The line length L_2 is a variable that can be used to tune the reflection coefficient at the fundamental (f_0) to the required value of odd mode impedance requirement for the amplifier performance.

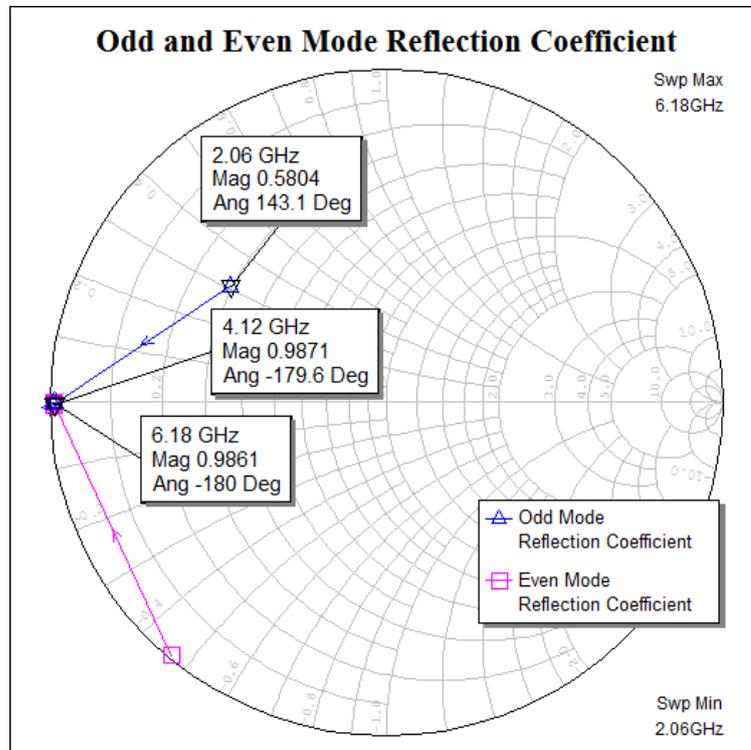


Fig. 4.11: Simulated results of odd and even mode reflection coefficients.

Fig. 4.11 shows the simulated results of odd and even mode reflection coefficients at fundamental frequency, 2nd harmonic and 3rd harmonic for the proposed design shown in Fig. 4.10. This Structure B has been specifically designed

to meet the impedance requirement of a given transistor (NPTB00004) at fundamental frequency with simultaneously suppressed harmonics.

In order to demonstrate how the new proposed structure is used to set the odd mode fundamental frequency impedance by simulation, the line length L_2 in Structure B has been varied and specifically tuned so that it will comply with the impedance requirements imposed by NPTB00004 RF Power GaN HEMT. In this case, a good compromise between achievable maximum Power Added Efficiency (PAE) and Total Power (PT) is concerned. Fig. 4.12 shows a simulated load-pull contour of shrunk sweeping range for that particular transistor which indicates where desired optimum load impedance might be for PT at the output and PAE respectively.

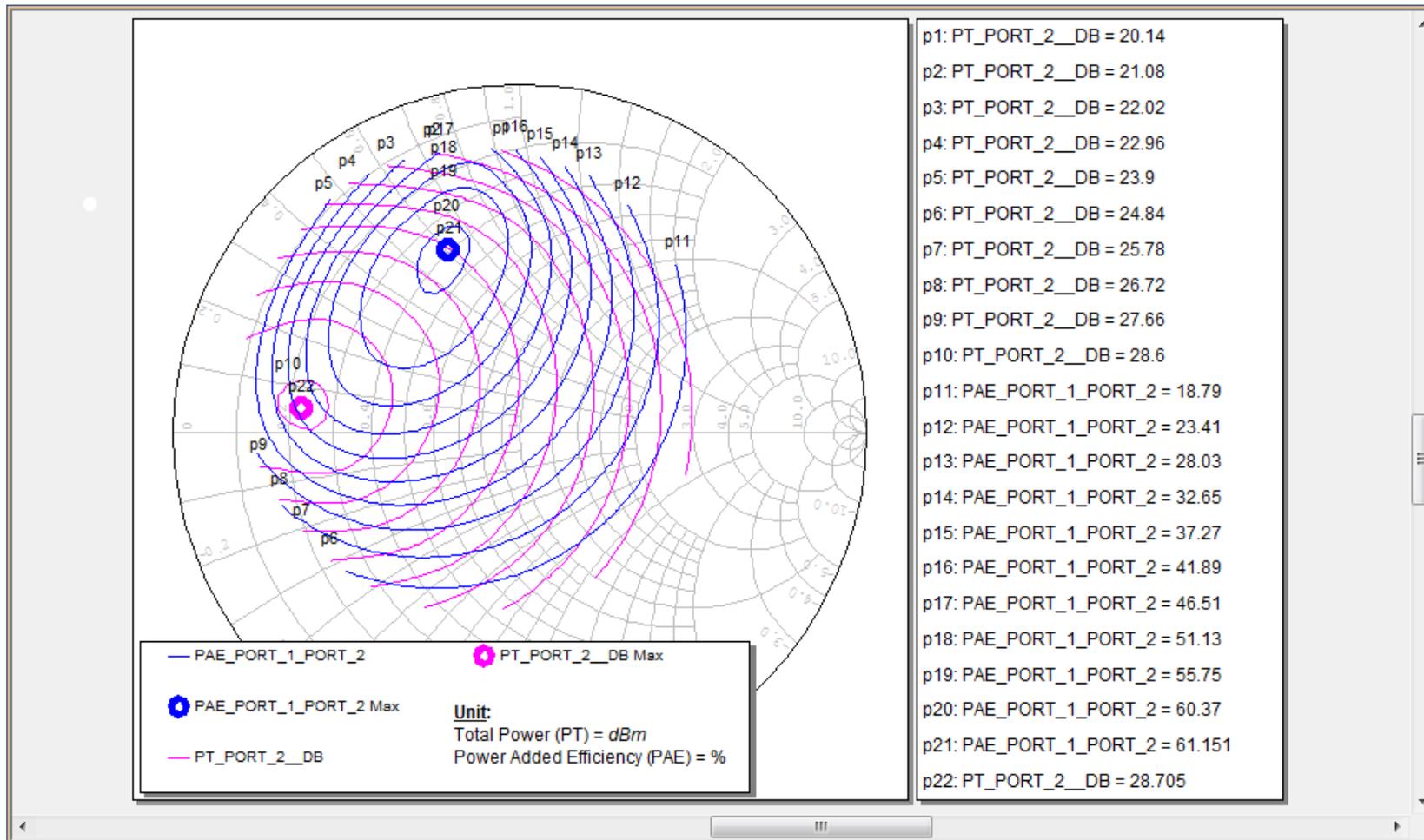


Fig. 4.12: Load-pull contour of NPTB00004 RF Power GaN HEMT.

Fig. 4.13 shows a trajectory of the odd mode reflection coefficient for the proposed structure on a Smith chart. There are nineteen red squares on the Smith chart resulting from nineteen different L_2 values moving towards the slotted ground plane whilst keeping all other parameters constant. This is what we would expect when we move a fixed capacitance (the stub reactance) up and down a fixed length of transmission line. Based on Fig. 4.12 and Fig. 4.13, we can see there is at least one point which falls onto the requirement of optimum load impedance for getting a very good compromise between PT and PAE. More generally, the trajectory suggests that the design variables available here including the size and shape of the aperture and the 50Ω line length, allow good coverage of the Smith so that a wide range of matching requirements could be met particularly for different devices and bias conditions. As for our proposed design of Structure B shown in Fig. 4.10, the reflection coefficient at 2.06 GHz is chosen to be at $0.5804\angle 143.1^\circ$ which will give a considerably good PAE as well as reasonably high PT.

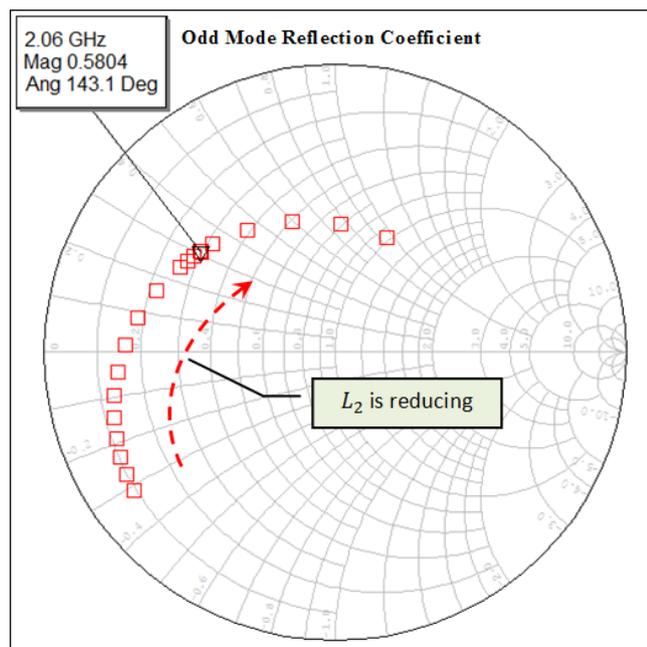


Fig. 4.13: Trajectory of the odd mode reflection coefficient.

Generally, the Structure B shown in Fig. 4.10 is designed using CST software and hence, it is not showing any other devices attached on the Structure B in the simulation. This is because of the integration of push-pull amplifier using two identical transistors (NPTB00004 RF Power GaN HEMT) and Structure B will be made and done in AWR MWO software. Basically, the line length L_1 of Structure B is purposely made 180° before the junctions with the harmonic stubs in order to establish a proper microstrip mode and thus, providing harmonics short effects. The simulated reflection coefficients for the odd- and even-mode shown in the previous Fig. 4.11 are the resulting of the line length L_1 effects is de-embedded in order to give impedance at the junction with the harmonic stubs. As a result, the 2nd (4.12 GHz) and 3rd (6.18 GHz) harmonics are seen as a short circuit and considered as perfectly suppressed since the reflection coefficient is $0.9871\angle -179.6^\circ$ and $0.9861\angle -180^\circ$ respectively. Simultaneously, the reflection coefficient or impedance at the fundamental (2.06 GHz) is tuned at $0.5804\angle 143.1^\circ$ in which it complies with the impedance requirements imposed by the transistor NPTB00004 RF Power GaN HEMT based on the simulated load-pull shown in Fig. 4.12. In other words, a point at where the junctions with the harmonic stubs will present impedance matching or reflection coefficients as mentioned above. Since both amplifiers have been specifically designed to be working in Class B where harmonics should be seen as short circuit ($0.99\angle 180^\circ$) and based on the transistor's simulated load-pull at the fundamental frequency, the differential signals generated by these amplifiers can be directly injected at the aforementioned point. This whole configuration has the potential to form a new push-pull transmitting amplifier and it is shown in Fig. 4.14. This could be best if compared with the conventional push-pull amplifier's version shown in Fig. 4.1 using ideal user-defined HBTUNER at the output stage.

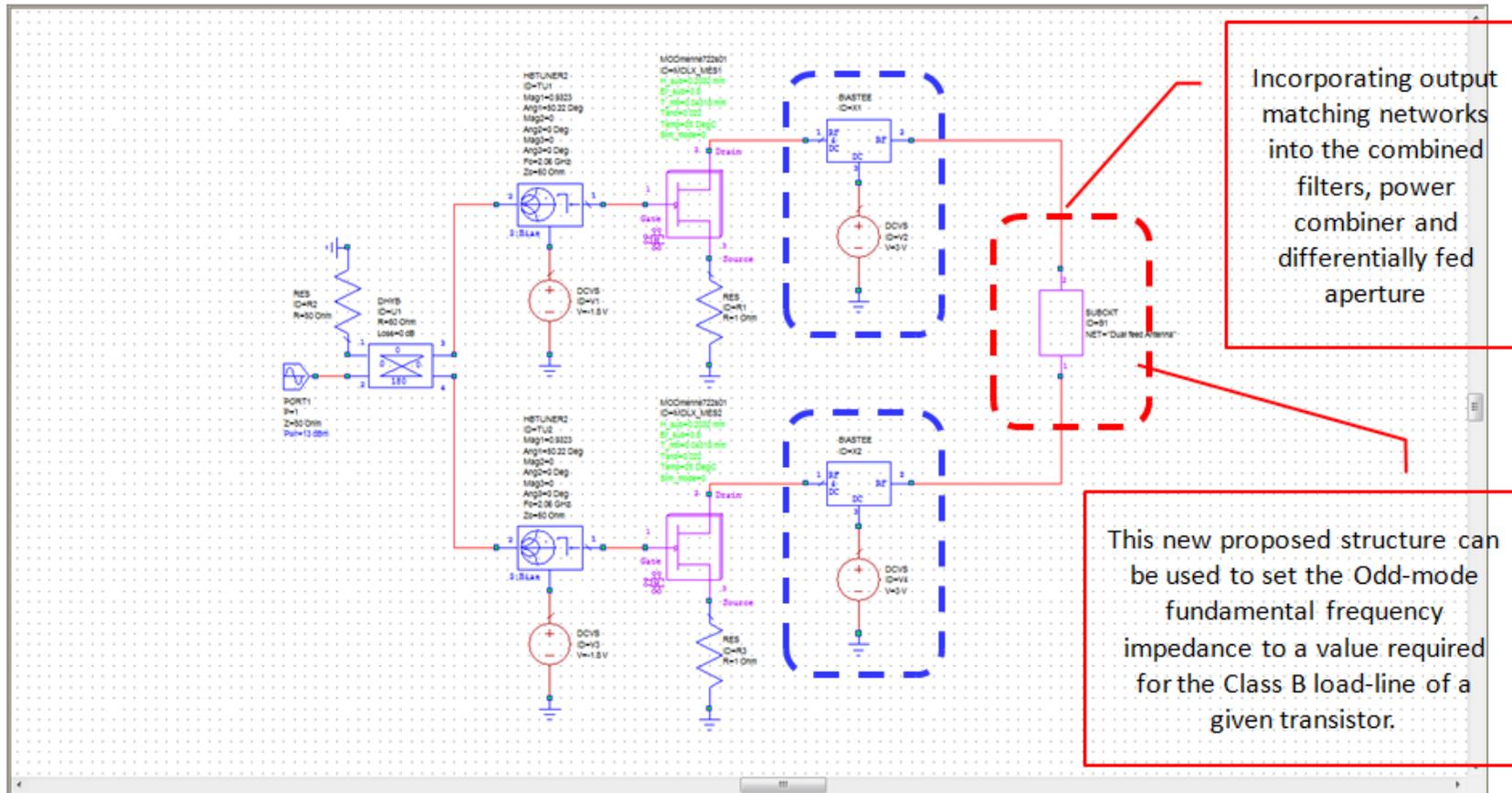


Fig. 4.14: Representation of new proposed push-pull transmitting power amplifier.

The comparison has been made through simulation between an ideal push-pull transmitting amplifier (Fig. 4.1) and this new representation of a push-pull amplifier as seen in Fig. 4.14. The current waveforms have been captured and compared at the node before entering a red dashed-line subcircuit block. Fig. 4.15 shows the comparison of those current waveforms, which have a good agreement. They differ slightly in the ripples due to the effects from higher order harmonics such as 5th and 7th. The reasonable agreement between the waveforms in Fig. 4.15 gives a verification of the proposed new structure. Noted that we are aware this is all observational and empirical as ideally, the current and voltage waveforms should be measured at the full package model to be able to properly use their intrinsic waveforms within the device package as a means of determining Class B mode of operation. Due to the limitation, this is not possible without a full package of an equivalent circuit model. At least, the current waveform at the device plane gives an indication of working in Class B.

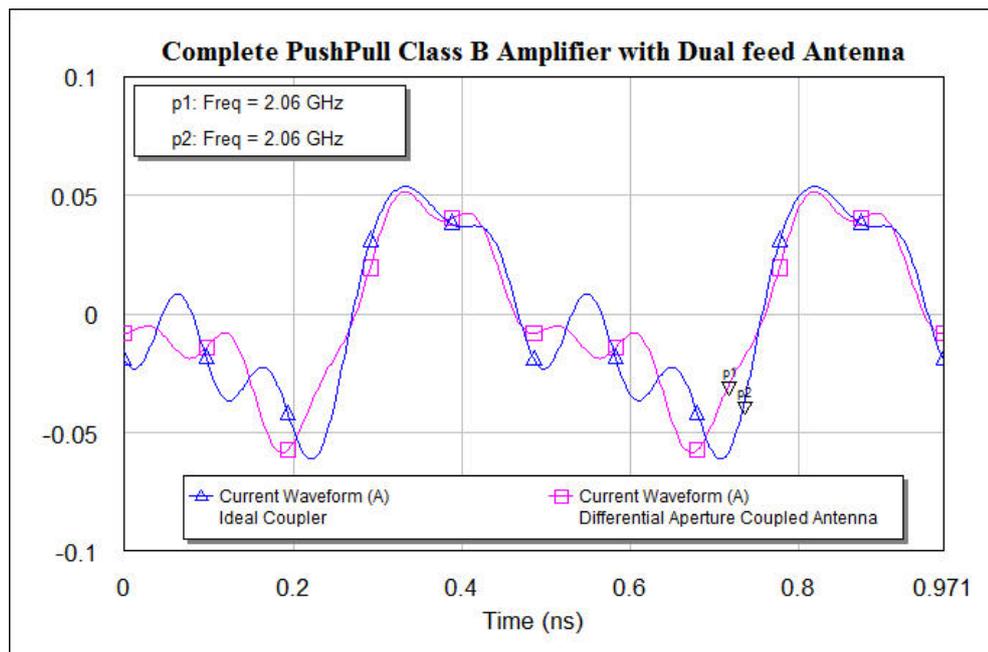


Fig. 4.15: Comparison of the current waveforms.

4.3 Parametric Study on Design Slot A

The purpose of this parametric study was to investigate and characterise the basic proposed design of a differentially fed aperture coupled microstrip antenna in order to find out the range of variation on the odd mode impedance or reflection coefficient at fundamental frequency. Besides, this is also to observe the effects on reflection coefficients at 2^{nd} (even) and 3^{rd} (odd) harmonics when one of the parameters is varied. The parameter variables involved in this study which is based on the primary design shown in Fig. 4.16 include the filter width (f_w), slot width (W_a) and slot length (L_a). Note that all dimensions for this primary design are similar to those of Structure B except for the slot's shape. The design of Slot A was inspired by the slot design from the Structure A.

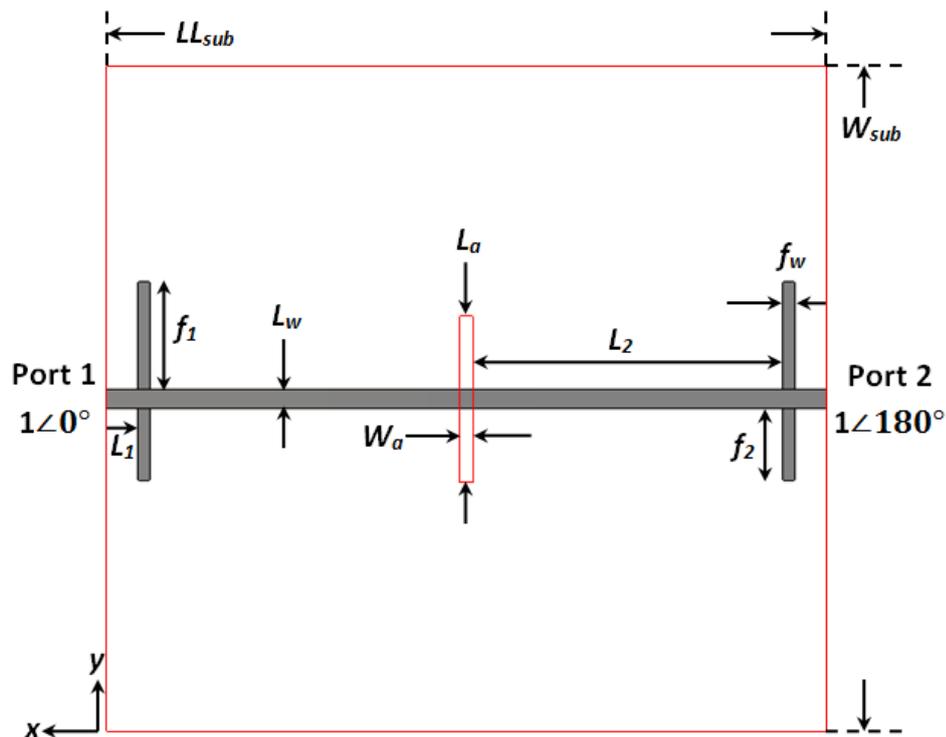


Fig. 4.16: Primary design for parametric study (bottom layer).

4.3.1 Effect of Filter Width Variation

There are seven different parameters with the primary filter width, $f_w = 1.4 \text{ mm}$ where the reflection coefficient on the Smith chart is $0.03688 \angle 28.94^\circ$. Fig. 4.17 shows there is a fine tuning of the odd mode reflection coefficient at the fundamental frequency due to small filter width (f_w) variation of 0.1 mm . The filter width variation which is started from $f_w = 1.1 \text{ mm}$ until 1.7 mm gives a slight effect on the odd mode reflection coefficient at the fundamental frequency. As the width varies, the residual susceptance of the stubs is varied, and hence the trajectory lies on a constant conductance circle.

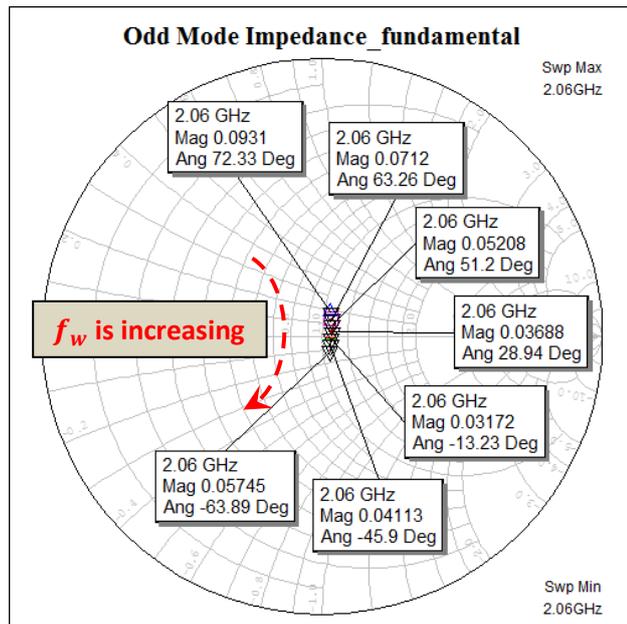


Fig. 4.17: Variation of the odd mode reflection coefficient at fundamental, f_o .

Furthermore, Fig. 4.18 and Fig. 4.19 respectively show the effects on 2nd and 3rd harmonic reflection coefficients when the filter width's variation takes place

simultaneously. Certainly, it does not affect much on harmonics as they still remain in a short circuit. This is because the stub length remains fixed at an appropriate length to generate harmonic short circuits, regardless of the line impedance.

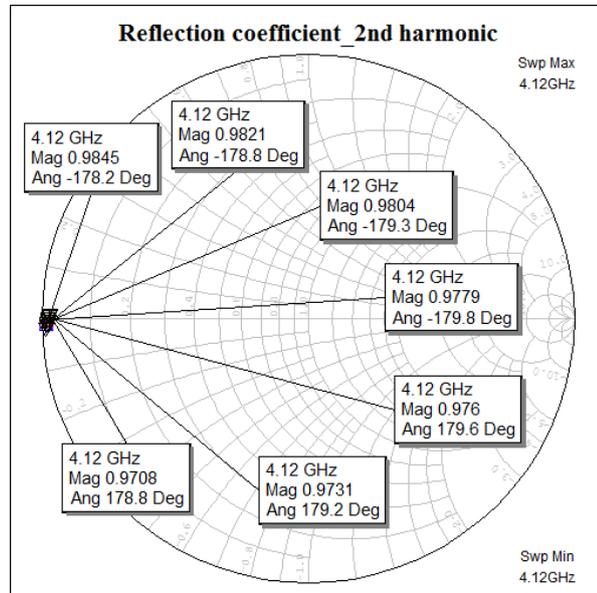


Fig. 4.18: Variation of the even mode reflection coefficient at 2nd harmonic.

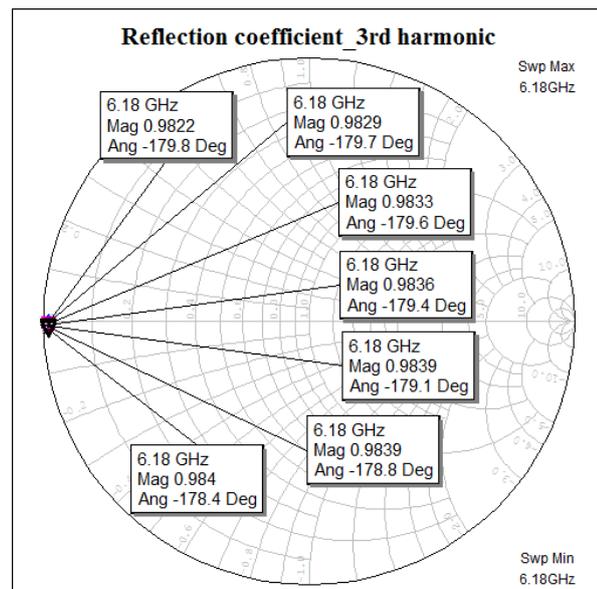


Fig. 4.19: Variation of the odd mode reflection coefficient at 3rd harmonic.

4.3.2 Effect of Slot Width Variation

In this parametric study, the slot width dimension has been varied from 0.5 mm to 1.5 mm in 0.1 mm steps. As seen in Fig. 4.20, there is a coarse variation of the odd mode reflection coefficient at fundamental frequency due to fine tuning of the slot width (W_a). This trajectory results from the changing radiation resistance and coupling capacitance which is transformed by the line length L_2 and the stub capacitance. This will allow good coverage of the Smith chart so that a wide range of impedance matching requirements could be met.

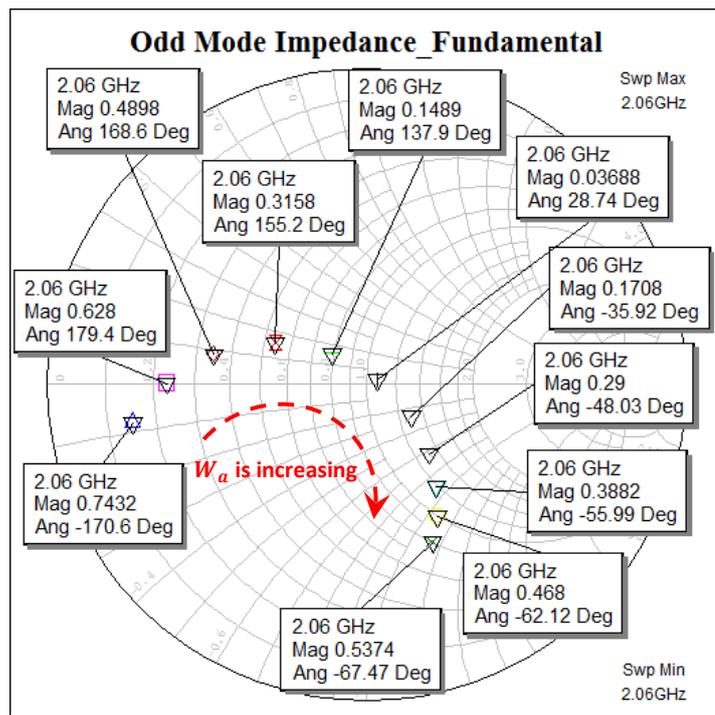


Fig. 4.20: Variation of the odd mode reflection coefficient at fundamental, f_o .

The slot width variations will not affect the harmonics. Fig. 4.21 and Fig. 4.22 respectively show that those harmonics still remain as short circuit.

4.3.3 Effect of Slot Length Variation

There are ten different parameters with the primary slot length, $L_a = 20$ mm. The variations between the shortest slot length (15 mm) and longest slot length (24 mm) with 1 mm steps are considered whose the reflection coefficient $0.9809\angle -139.2^\circ$ and $0.9339\angle -109.1^\circ$ respectively. As seen in Fig. 4.23, there is a variation of the odd mode reflection coefficient at the fundamental frequency which is distributed in a circular array. As can be seen the trajectory is very similar to that in Fig. 4.20, except that here the circular trajectory is more complete and reaches the outer edge of the chart, because of transmission line resonance associated with the slot. This also allows a very good coverage on the Smith chart so that a broad range of impedance matching requirement could be possibly met.

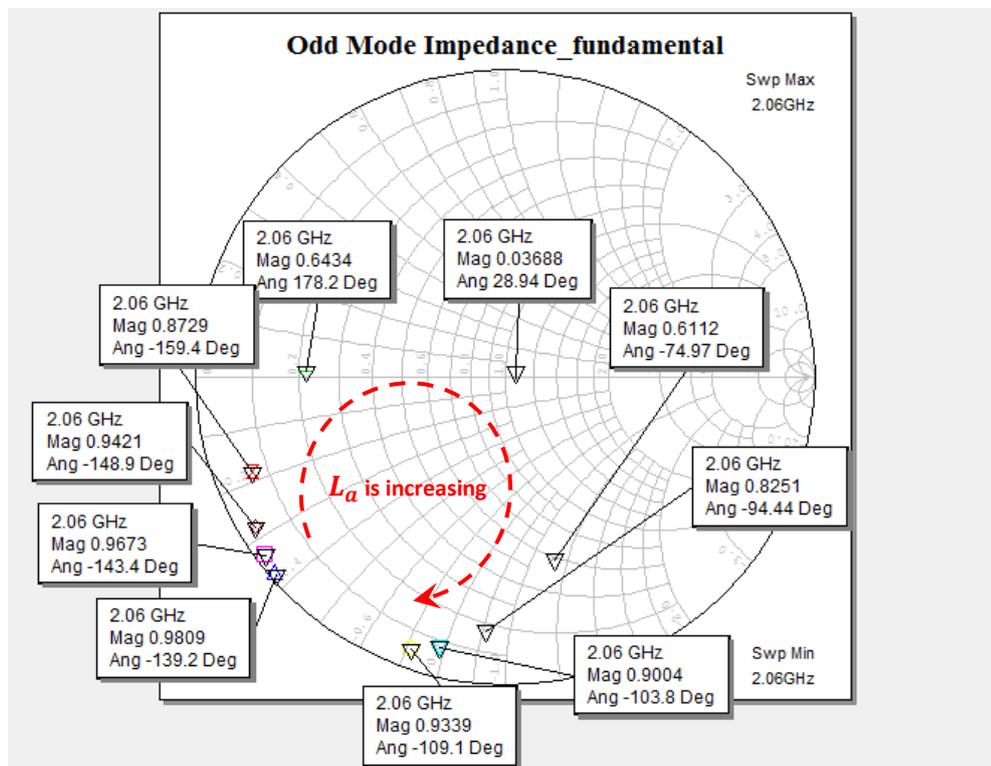


Fig. 4.23: Variation of the odd mode reflection coefficient at fundamental, f_o .

Similarly, the slot length variation does not indicate significant changes on the harmonics. Hence, Fig. 4.24 and Fig. 4.25 proved it all remain as short circuit.

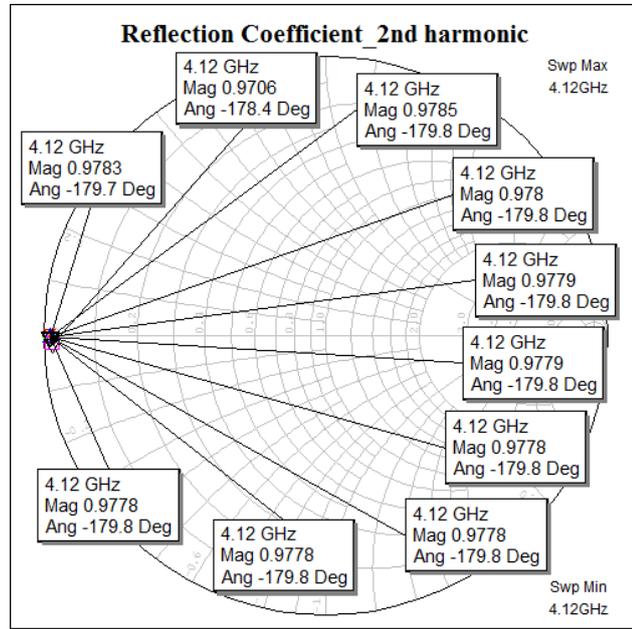


Fig. 4.24: Variation of the even mode reflection coefficient at 2nd harmonic.

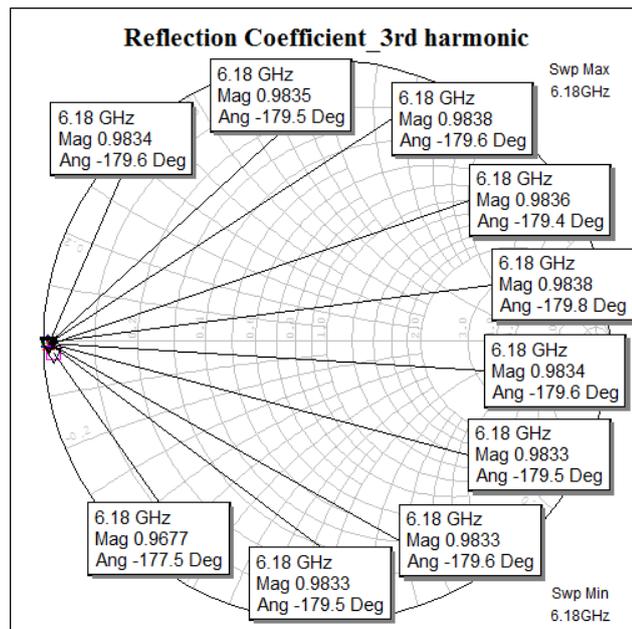


Fig. 4.25: Variation of the odd mode reflection coefficient at 3rd harmonic.

4.3.4 Effect of Moving Filter Point

For three different values of W_a (0.5 mm, 1 mm and 1.5 mm), variation of the odd mode reflection coefficient is determined by simulation for 35 different values of L_2 which is started from $L_2 = 38.45 \text{ mm}$ until $L_2 = 4.45 \text{ mm}$ in 1 mm step. From the figures shown in Fig. 4.26, Fig. 4.27 and Fig. 4.28, there are three different interesting trajectories of the odd mode reflection coefficient on the Smith chart which indicates every possible point of impedance matching requirement for any given devices and bias condition. This is precisely what we would expect when we vary the length of a transmission line which is terminated in a non 50Ω impedance.

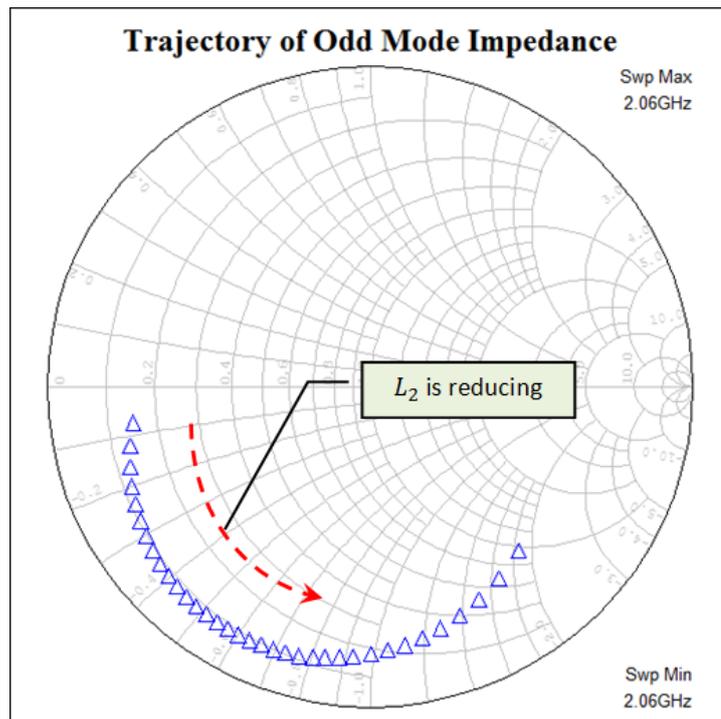


Fig. 4.26: Trajectory of the odd mode impedance when changing L_2 while maintaining the slot width, $W_a = 0.5 \text{ mm}$.

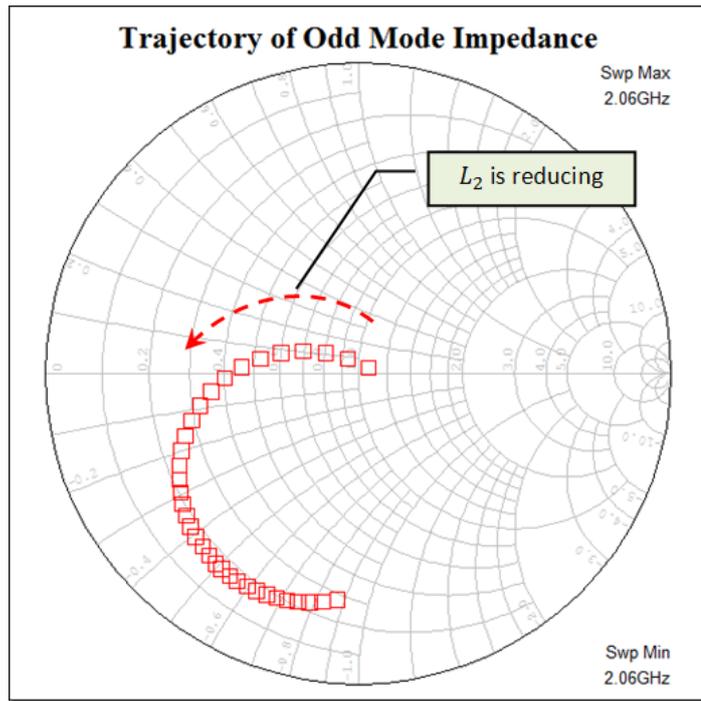


Fig. 4.27: Trajectory of the odd mode impedance when changing L_2 while maintaining the slot width, $W_a = 1$ mm.

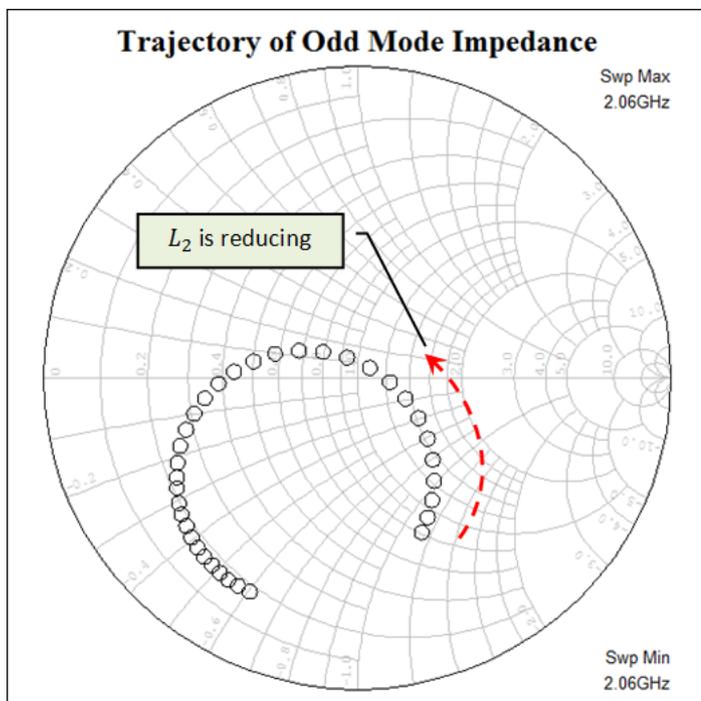


Fig. 4.28: Trajectory of the odd mode impedance when changing L_2 while maintaining the slot width, $W_a = 1.5$ mm.

4.4 Parametric Study on Design Slot B

In the previous parametric study, most of the odd mode impedances have covered the lower region on the Smith chart. In this section, another set of novel techniques will be investigated, aimed at covering the upper region of Smith chart with every possible point of the odd mode impedance matching requirement. The parameter variables involved in this study is based on the primary design of Structure B shown in Fig. 4.10. The effects of moving filter point towards designated slot are considered. There are three different design of slotted ground planes involved in this study. They are shown in Fig. 4.29.

Based on Fig. 4.29, for three different values of L_b ($L_{b_0} = 14$ mm, $L_{b_1} = 16$ mm and $L_{b_2} = 18$ mm), variation of the odd mode reflection coefficient has been determined by simulation for 16 different values of L_2 which is started from $L_2 = 38.45$ mm until $L_2 = 23.45$ mm in 1 mm step. Fig. 4.30 shows the effect on a trajectory of the odd mode impedance based on the moving filter points towards different designated slotted ground plane. It seems the trajectory of the odd mode reflection coefficient has good coverage on the Smith chart especially the upper region.

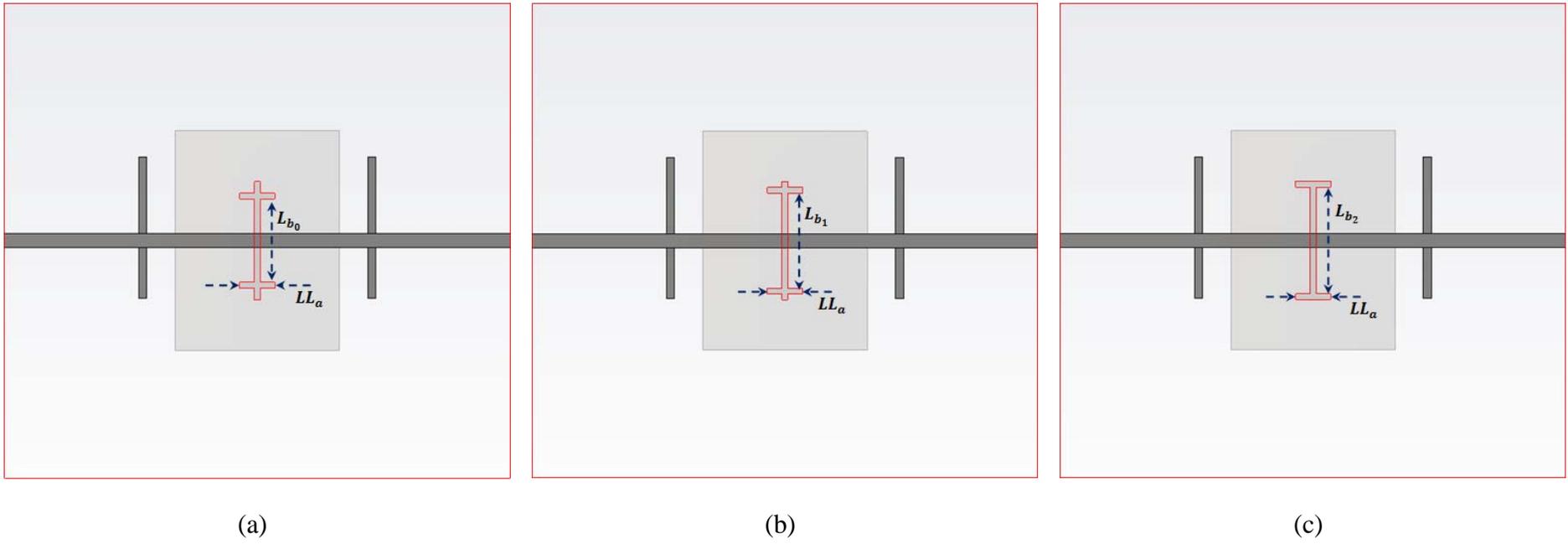


Fig. 4.29: Different design of slotted ground planes.

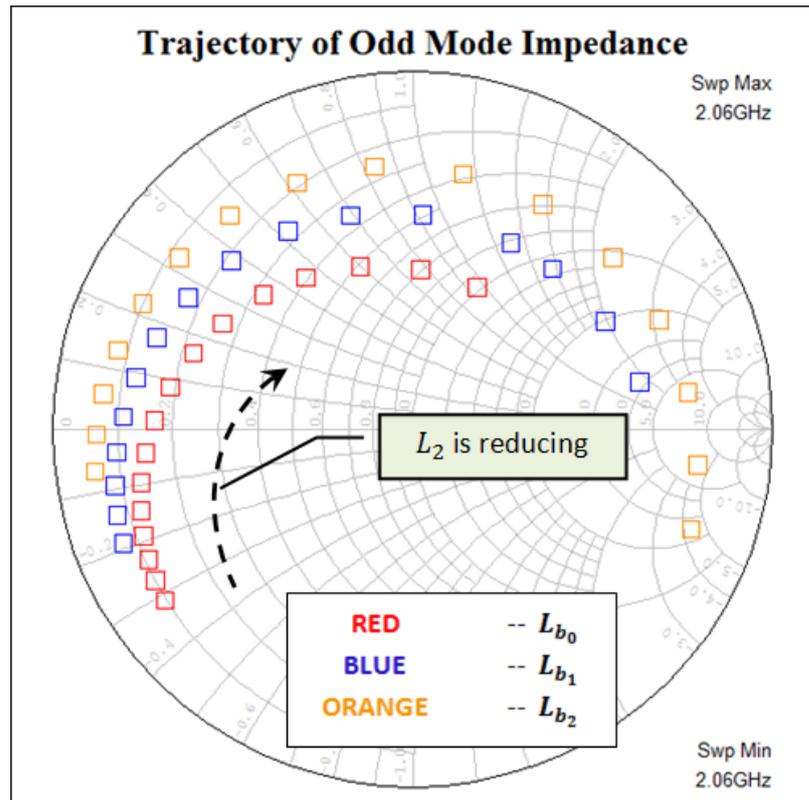


Fig. 4.30: Trajectories of the odd mode impedance at fundamental, f_o .

This novel technique allows the power combiner and matching network functions to be integrated into the two-port antenna structure. It has sufficient degree of freedom so that we can simply and systematically vary the available parameters to fit with the requirement of the design specification for any given devices and bias conditions. Therefore, it can offer advantages of neat and tight integration of a push-pull transmitting amplifier. Furthermore, controlling other higher harmonic impedances using open-circuit stubs will produce less-distorted output waveforms at a cost of rising in complexity.

4.5 Summary

A novel optimum power combiner for a push-pull transmitting power amplifier configuration is proposed. This structure was inspired by a technique of spatially coupling differential signals from a transmission line to an antenna structure via an aperture. The idea of combining differential signals from two active devices from push-pull is used to generate maximum current for the antenna whilst eliminating the associated losses and the necessity of a second hybrid or balun at the output. This concept of antenna feeding technique makes use of the open-short circuit transmission line theory [94] and it was first demonstrated by Pozar [71] on a single fed aperture coupled antenna in which it uses an extended microstrip line (terminated in an open-circuit) with approximate length of $\lambda/4$ beyond the edge of slot/aperture. This is actually creating an effective virtual short-circuit where the input impedance $Z_{in} = 0$ at the centre of the slot/aperture which indicates the current intensity at that particular point is maximum.

Two differentially fed multilayer passive antenna designs have been presented. The first antenna structure was purposely designed to be a power combiner and output matching network for differential signals from push-pull output using transistor NEC NE722S01 Low Noise / Low Power MESFET as amplifier. Secondly, the same concept was applied to another transistor, the NITRONEX NPTB00004 RF Power GaN HEMT in which a reduced size and compact version of push-pull amplifier-antenna module is obtained.

Furthermore, parametric studies on the available design variables for two different slot / aperture designs have been done. It was found that every design parameter has its limits. It shows the importance as well as advantages of available design variables owned by one structure. From both theory and simulation which show that the line length L_2 and the slot dimensions are the key parameters that we can use and manipulate in order to give such a good Smith chart coverage. This is actually reflects the technique of how to set the odd-mode fundamental frequency impedance to a value required for any classes of amplifier's load-line of a given transistor.

No major degradation in antenna performance such, radiation pattern and gain is expected when these key parameters (L_2 and the slot dimensions) are varied in order to achieve impedance matching. In this case, it was reasonable to assume that the presence of the ground plane between the layers would cause the positioning of the stubs relative to the aperture/slot not to affect the radiation pattern while improving the gain [93]. Generally, the bandwidth of the structure depends on the design variables that are available here including the size and shape of the aperture as well as the 50Ω line length, L_2 . This will allow very good coverage of the Smith Chart so that a wide range of impedance matching requirements could be met for any given devices, bias conditions and resonance frequency. Ultimately, the bandwidth of this type of system is expected to be dominated by the bandwidth of the antenna structure itself. It is possible to use matching networks on the outside, and, in the present case a complex feed network to optimise the bandwidth, subject to the Bode Fano limit. The couplet used to generate the odd mode signal would also influence the bandwidth when using the odd mode feed concept. Optimising the bandwidth

was not carried out as part of the current project. Note that what is required here is a matching concept that allows the optimum transistor input impedance to be tracked over the required frequency range.

CHAPTER 5

FULLY INTEGRATED AMPLIFIER–ANTENNA SIMULATIONS AND MEASUREMENTS

5.1 Introduction

The previous chapter has presented in detailed the theory and simulation of a differential aperture coupling technique for push-pull transmitting amplifiers. It started with the concept of a single fed aperture coupled antenna to show how maximum current is effectively being created to electromagnetically couple the energy to microstrip patch antenna through slot/aperture. This was followed by the two types of differentially fed aperture coupled passive antennas namely Structure A and Structure B respectively including some simulated and measured results to support the proposed design theory. Furthermore, the parametric studies on the available design variables for two different slot/aperture designs have been carried out to investigate the potential coverage of the Smith chart so that a wide range of matching requirements could be met for different devices and bias conditions.

This chapter presents the direct integration of a push-pull amplifier and an aperture coupled antenna. It starts with the simulation of push-pull transmitting amplifier followed by its transformation into a fully integrated version using realistic

lossy components such as optimised biasing decoupling circuits and a power divider with a phase shifter. Comparison between those two versions has been made through simulation. Some initial results from lab-based testing were taken before a proper measurement was carried out in the anechoic chamber. This is solely for ease of troubleshooting in order to ensure the prototype is credible to operate when real measurement takes place.

5.2 Push-pull Transmitting Amplifier

Previously in Fig. 4.1, an ideal configuration of push-pull transmitting amplifier is shown purposely to express the idea of replacing the output matching networks, 180° hybrid coupler and harmonic traps that reside within the red dashed-line block with a proposed design of Structure A or Structure B. One example design was shown in Fig. 4.14 where Structure B is incorporated within the ideal push-pull amplifier. In this section, it is only Structure B which will be discussed further for direct integration with other subcircuit blocks such as transistors, input and output bias decoupling circuits.

This is a challenging task to accommodate those mentioned three subcircuit blocks within the limited size of Structure B. As for this case, the Wilkinson power divider with 180° phase shifter will be a separate entity. Therefore, this push-pull transmitting amplifier is formed by two main blocks comprising a Wilkinson power divider with phase shifter and another block that effectively incorporates the output

matching network functions, power combiner, bias decoupling circuits, antenna and amplifiers. Fig. 5.1 shows the array of subcircuit blocks which is neatly transformed into a push-pull transmitting amplifier front-end.

The next section discusses the construction of input and output bias decoupling circuits along with the 180° phase shift Wilkinson power divider. The simulated results for those structures are shown accordingly as well.

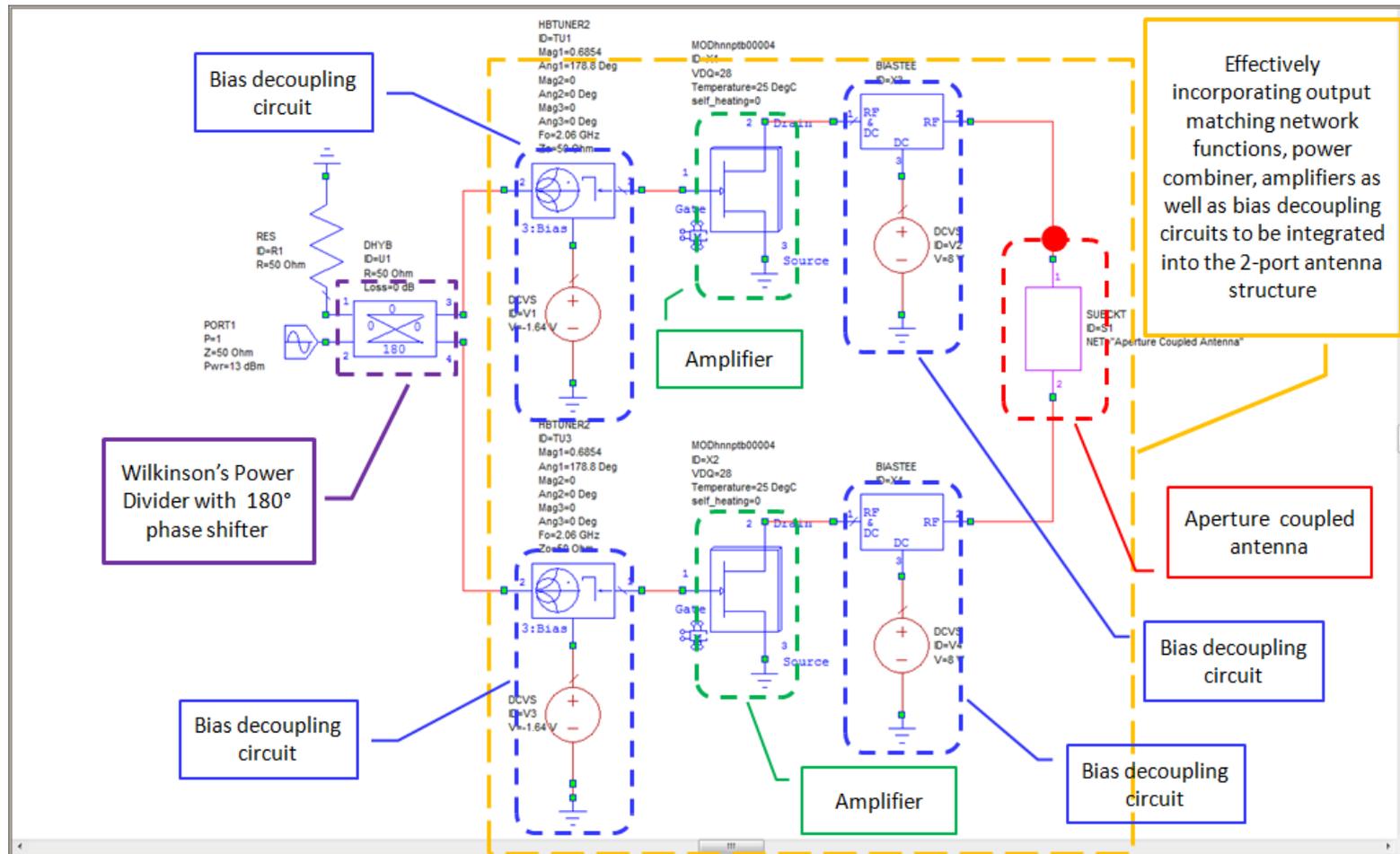


Fig. 5.1: Proposed push-pull transmitting amplifier front-end.

5.3 Wilkinson Power Splitter / Divider

The Wilkinson divider is an ideal form of power splitter / divider that is often used in many RF and microwave applications. It uses quarter-wave transformers which are easily fabricated on printed circuit boards and hence, it is a very cheap and simple power divider while still providing high levels of performance. The advantages of Wilkinson power divider include simplicity, reasonably low cost, considerably low loss and a high degree of isolation between the “output” ports.

Although the Wilkinson power divider concept can be used for an N-way system, it is easiest to see how it operates as a two way system. The Wilkinson power divider uses quarter-wave transformers to split the input signal in order to provide two output signals that are in-phase with each other. In this work, as the two legs of the splitter / divider are not identical in that they have different electrical length about 180° , the signals appearing at the outputs will have 180° phase difference with the same magnitude. Besides, theoretically the Wilkinson power divider can be considered as lossless since there is no current flow in the resistor which means the resistor does not dissipate any power. However, in practice there are some losses introduced but these are relatively low and can be neglected.

Fig. 5.2 shows a two way Wilkinson power splitter / divider with 180° phase difference at the outputs while Fig. 5.3 shows the simulated results, showing very good return loss at port 1, equally divided and transmitted power to the outputs at port 2 and port 3 as well as providing considerably good isolation between those two

ports. Meanwhile, Fig. 5.4 shows the outputs of Wilkinson power divider that have the same magnitude with 180° phase difference.

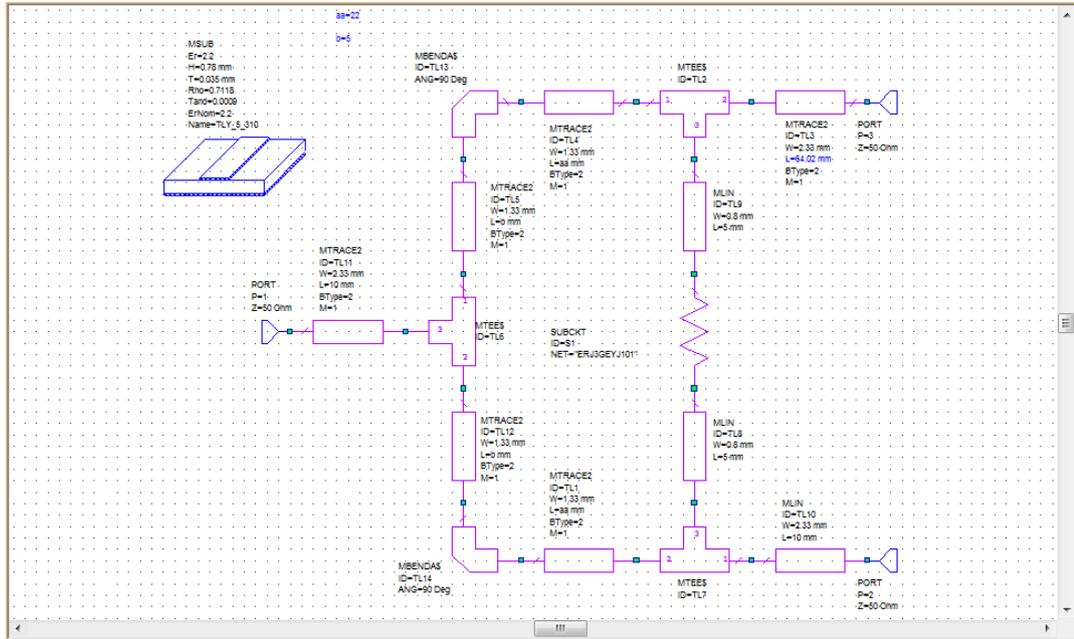


Fig. 5.2: Two way Wilkinson power splitter / divider.

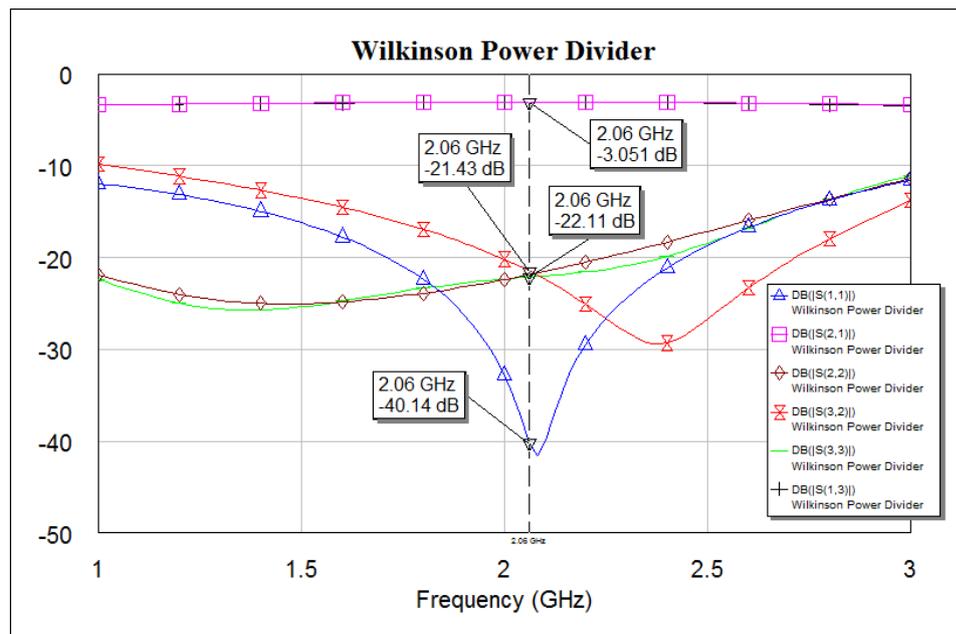


Fig. 5.3: S-parameter results of Wilkinson power divider.

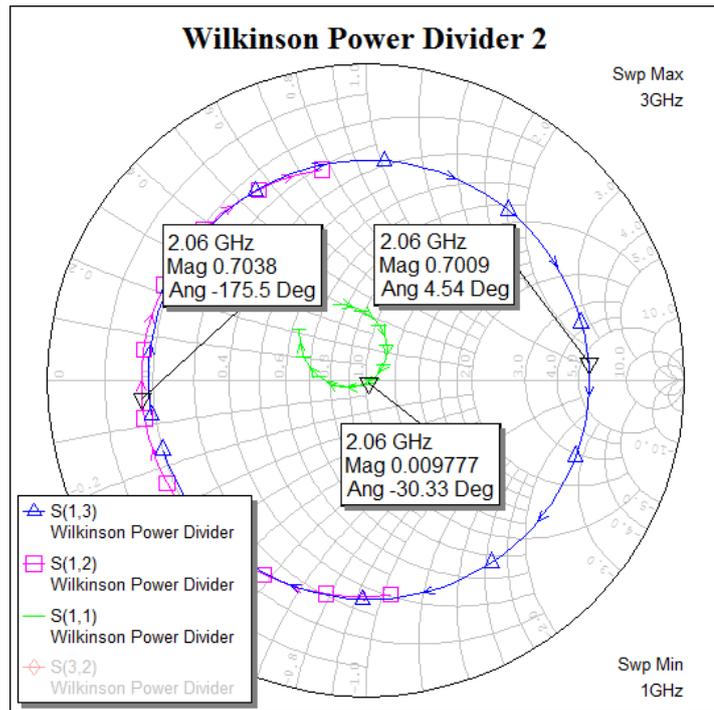


Fig. 5.4: Phase difference at the outputs of Wilkinson power divider.

5.4 Bias Decoupling Circuit

The design of bias decoupling circuit plays an important role in establishing stable operation and it is a fundamental and absolutely necessary in any RF power amplifiers design since at lower frequencies the impedance presented to the transistor is mainly determined by the bias circuitry. There are several versions which vary from other forms of bias decoupling circuit. Fig. 5.5 shows the complete push-pull transmitting amplifier prototype with standard configuration of input and output bias decoupling circuits where all elements are from real lossy material. As mentioned in the previous chapter, there is a series capacitor on both sides of the transistor to block the DC current from flowing into the source and the load. Also at the load side, there

is an EM Structure represented by a subcircuit block incorporating the output matching network functions, power combiner, antenna and harmonic traps that lies at the load side of the transistor which present an open circuit at design frequency 2.06 GHz, and a short circuit for up to 3rd order harmonics. Therefore, only the fundamental frequency power is transmitted through the patch antenna via aperture.

As seen in Fig. 5.5, there is a large capacitor at the edge end of the biasing line which is mainly to provide a short circuit at that connection point. With a quarter-wavelength ($\frac{\lambda}{4}$ at f_o) of the biasing line, the other end of that biasing line will be seen like an open circuit which will prevent fundamental frequency signal from flowing into the voltage source. Furthermore, an optimum inductor which is connected in series with the DC voltage source is purposely for backing up the imperfection of the capacitor. This precaution step is required and necessary to ensure the point where the connection of the biasing line with capacitor still remains as a perfect short circuit. So, the fundamental signal will see the impedance at the junction with that biasing line as an open circuit and thus, it can flow through the line length L_2 of the aperture coupled antenna. According to Tian He in [93], there should be inductors at the input side of the transistors which will be working as RF Choke. Besides, both voltage sources are connected to large capacitor in parallel to prevent a sudden change of the voltage supply while the 100 Ω and 100k Ω resistors to ground for safety precaution steps in case the parallel capacitors do not behave well, avoiding the transistors from burning out.

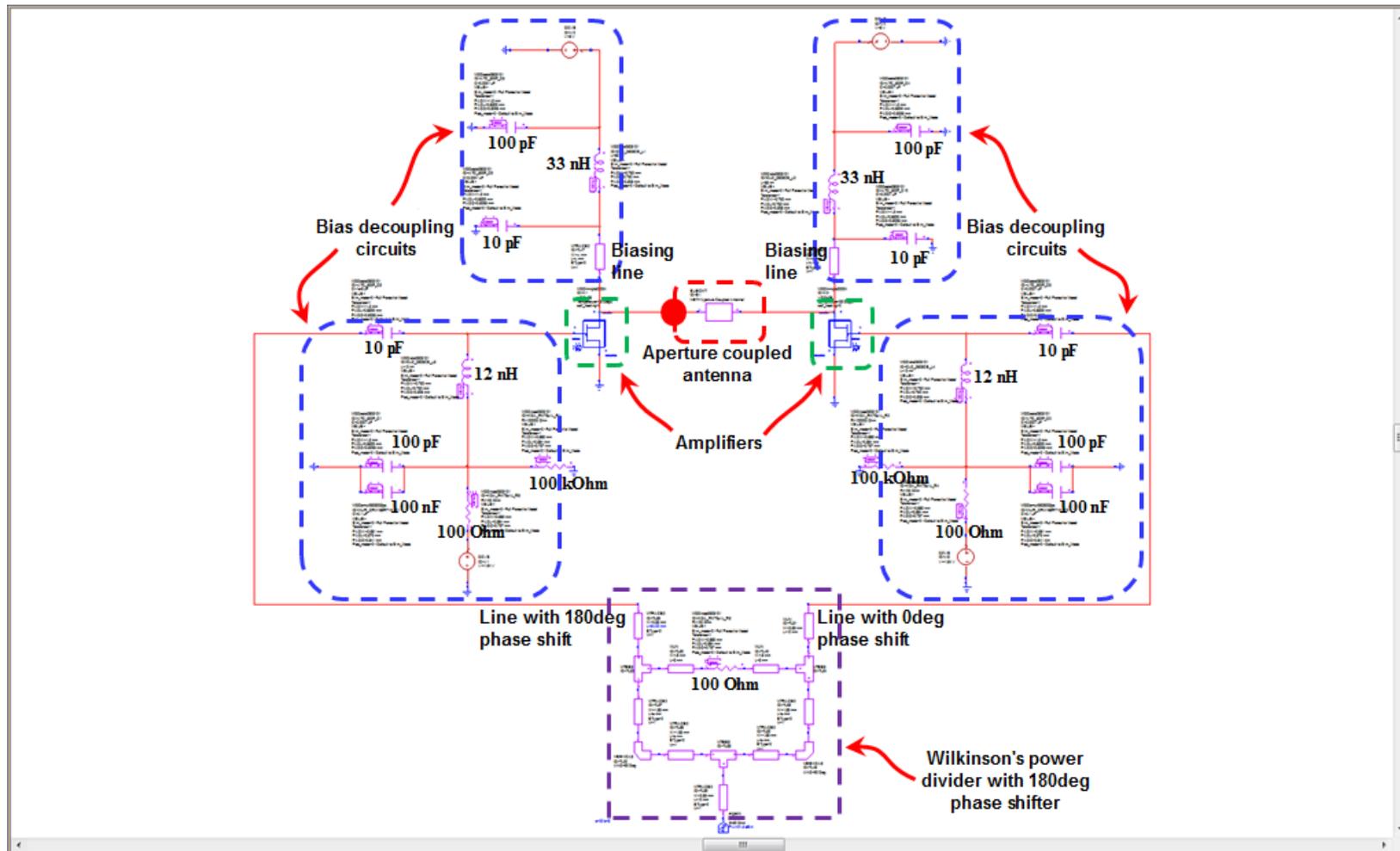


Fig. 5.5: New push-pull transmitting amplifier prototype.

5.5 Comparison of Push-pull Amplifier Topologies

Before any further characterisation of the embedded amplifiers in an aperture coupled antenna, it is necessary to verify the prototype. This confirmation is very important because it is not possible to measure the output power and PAE of the amplifiers directly since they are physically connected to the antenna with no detachable interface. Therefore, a comparison is made between two different push-pull amplifier topologies in terms of waveform at a selected node on the circuitry, by simulation. This could at least ensure the embedded amplifiers will work and behave in Class B mode and are not adversely affected by the proposed EM Structure B during a real in-house test.

The comparison made is based on Fig. 5.1 and Fig. 5.5. All components used in Fig. 5.5 are from real lossy materials including substrate, capacitors, inductors, resistors and transistors. In other words, all components that reside within the subcircuit blocks shown in Fig. 5.1 are replaced by the realisable structures. There is one selected node on ideal circuitry as seen in Fig. 5.1 to observe the current waveform flowing into the Structure B. The same nodes applied to the prototype shown in Fig. 5.5 so that the consistency for both ideal push-pull amplifier and the new prototype could be assessed. The simulations have been carried out for both circuits and the results are shown in Fig. 5.6. Comparing those two waveforms, it is obvious that the prototype has retained a similar trend of waveform characteristic to that of its ideal form. It is then confirmed that the prototype worked well in Class B mode.

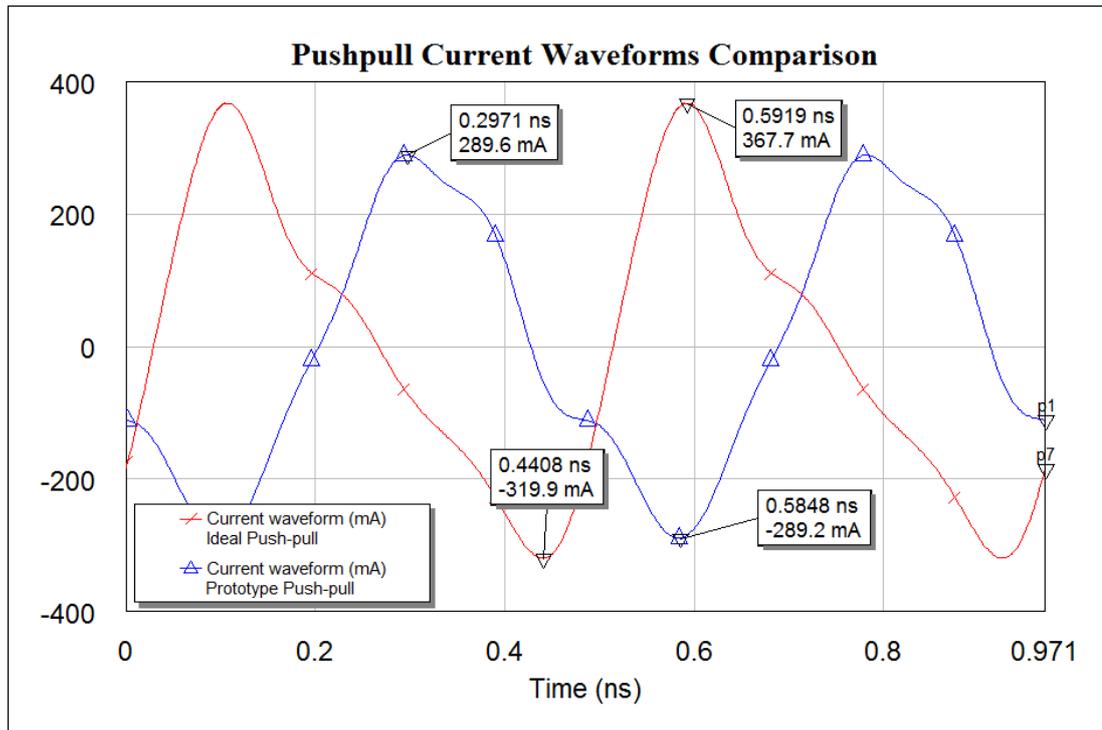


Fig. 5.6: Comparison of the current waveforms between ideal push-pull and new prototype.

5.6 Fully Integrated Push-pull Transmitting Amplifier

Apart from establishing a novel technique for direct integration of power amplifiers and antennas, it is of interest to demonstrate the feasibility of applying it to a fully integrated antenna–amplifier front-end. This also has a potential to realise a fully integrated push-pull amplifier for microwave transmitters.

In this work, a passive version of the antenna is adapted from aperture coupled microstrip antenna. As for the active version of this novel antenna, it is constructed by mounting an opposed pair of Class B amplifiers into the line with the

harmonic traps, 50Ω line length, aperture and radiating patch forming the output load and matching networks as seen in Fig. 5.7. Two transistors from Nitronex NPTB00004 are used with Class B operation in a push-pull amplifier configuration. They are placed in such a way that the amplifiers' outputs are facing each other as shown in Fig. 5.7.

Meanwhile, Fig. 5.8 shows a real fabricated prototype of embedded push-pull amplifier based on antenna Structure B shown in Chapter 4. During odd mode excitation, the amplifiers will be in a differential configuration and create maximum current at the centre point where two signals meet and interact between the circuits and patch antenna.

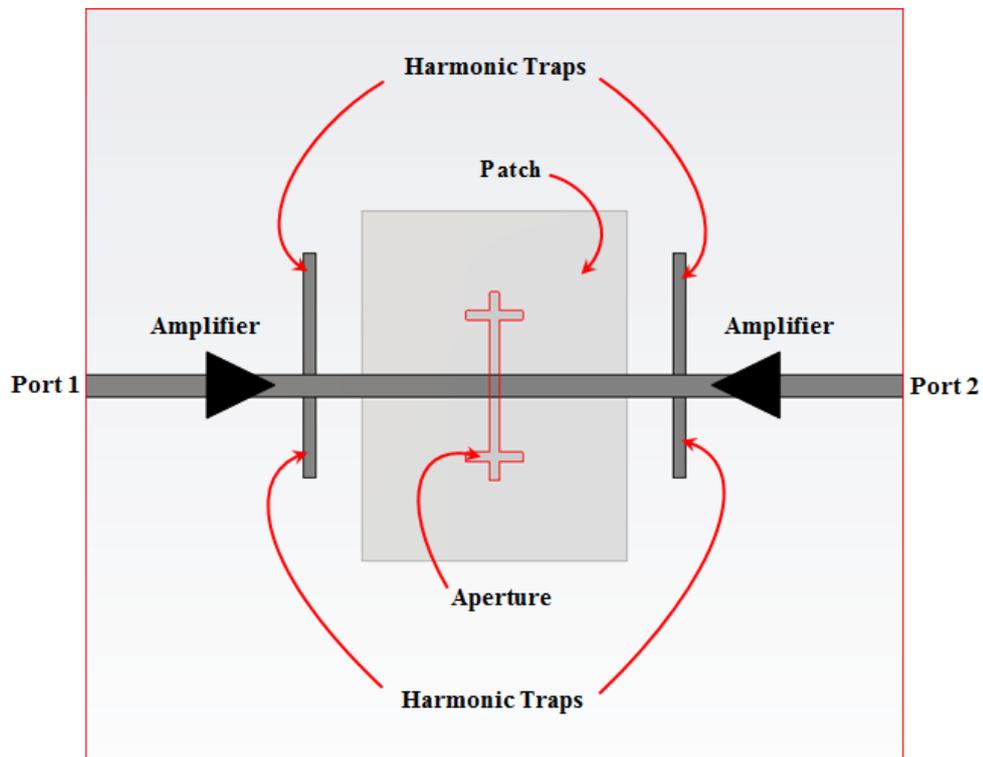


Fig. 5.7: Layout of amplifiers embedded on antenna Structure B.

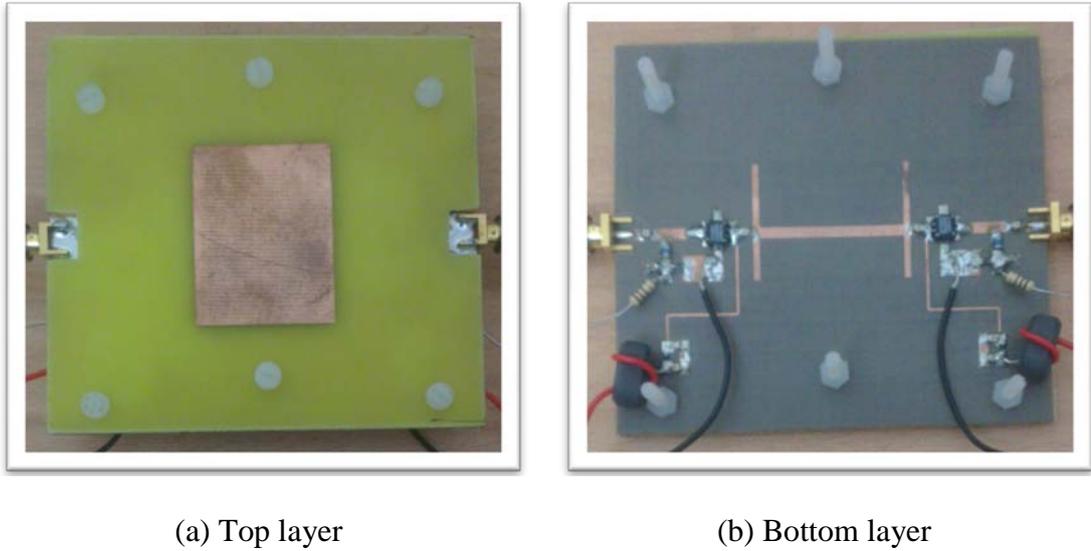


Fig. 5.8: Fabricated push-pull transmitting amplifier.

5.7 Measurement

In order to validate this fully integrated push-pull transmitting amplifier, a systematic measurement procedure is required. A block diagram which is illustrating the measurement setup can be seen in Fig. 5.9. Firstly, the structure under test (SUT) should be in transmitting mode. There are two types of SUT involved in this measurement, the passive antenna and an active integrated antenna as known as push-pull transmitting amplifier. Note that the passive antenna structure has no embedded amplifiers and hence, no harmonic traps are required.

In this case, a single rectangular patch antenna which is printed on FR-4 board is used at the receiving side. This receiving antenna has been specifically designed to have resonance at 2.06 GHz. Secondly, the measurement starts with

measuring the received power from both SUTs over a range of frequencies. Finally, the difference in received power between both measurements is the power gain of the integrated push-pull amplifier. Generally, the experimental works are divided into two parts which are stated as follows:

- i. Measurement of received power between Rectangular Patch Antenna (receiving mode) and Differential Fed Aperture Coupled Antenna (transmitting mode).
- ii. Measurement of received power between Rectangular Patch Antenna (receiving mode) and Push-pull Transmitting Amplifier (transmitting mode).

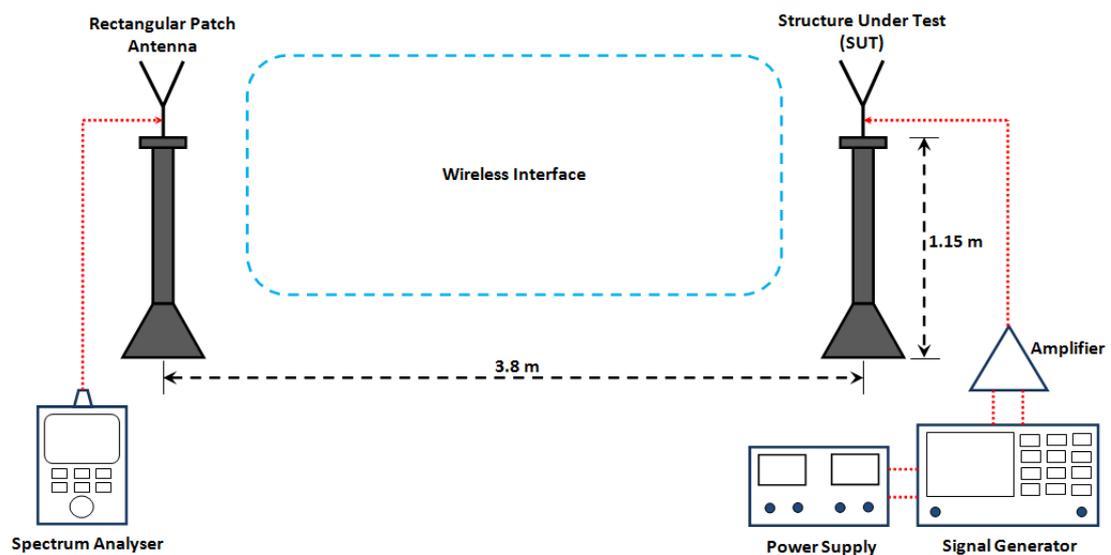


Fig. 5.9: Measurement setup for small signal power gain.

The received power measurement was successfully carried out in an open lab environment using available equipments and facilities. As seen in Fig. 5.9, the transmitting and receiving antenna are separated by a distance which is sufficient to

be in the farfield zone. This is to ensure a rectangular patch antenna is illuminated by a plane wave from the transmitting SUTs during measurement. With step frequency 10 MHz which is started from 1.9 GHz to 2.2 GHz, the received power was measured. Fig. 5.10 shows a comparison of received power from two different structures which are passive and active respectively. As seen in Fig. 5.10, the push-pull transmitting amplifier is capable of providing an additional power gain about 6 dB at designed frequency 2.06 GHz.

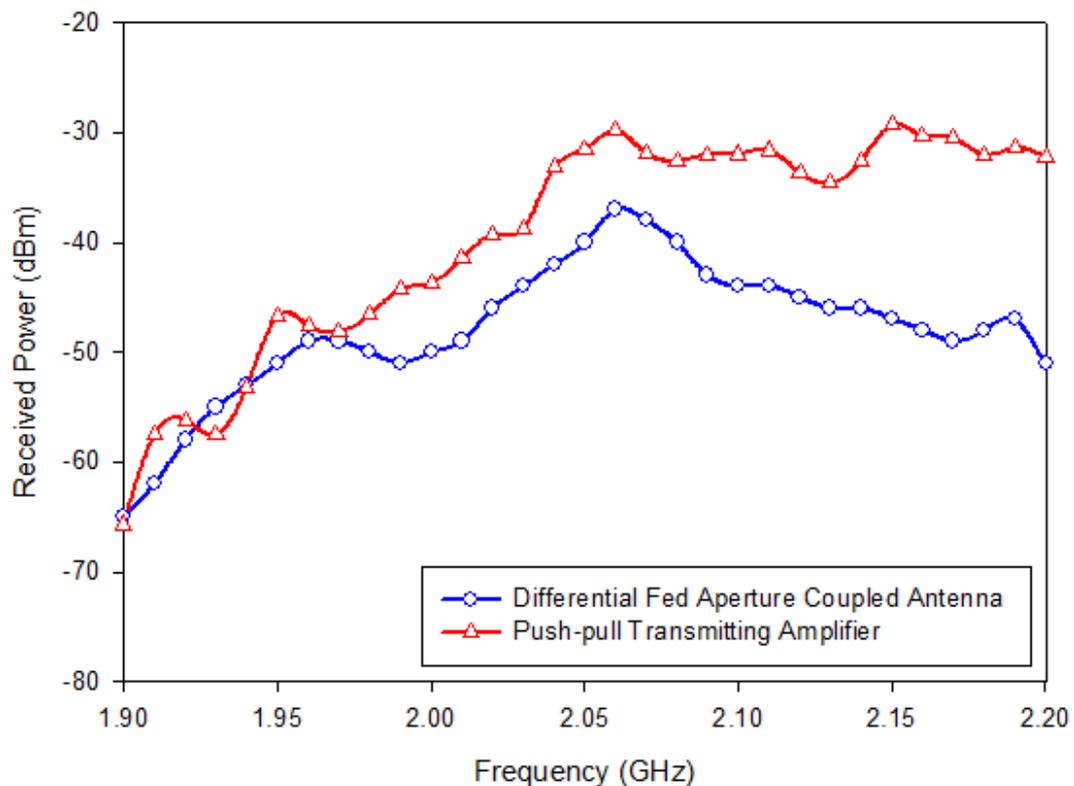


Fig. 5.10: Received power from the passive and active integrated antenna.

Since the harmonic terminations are incorporated with Structure B, it is one of our concerns to observe the response of the received power due to 2nd and 3rd harmonics. The same measurement setup and procedure is used to measure the

received power and their differences compared to the fundamentals were observed. The measured results have been plotted in separate graphs shown in Fig. 5.11 and Fig. 5.12 respectively. Those two figures show that the harmonics have been well suppressed.

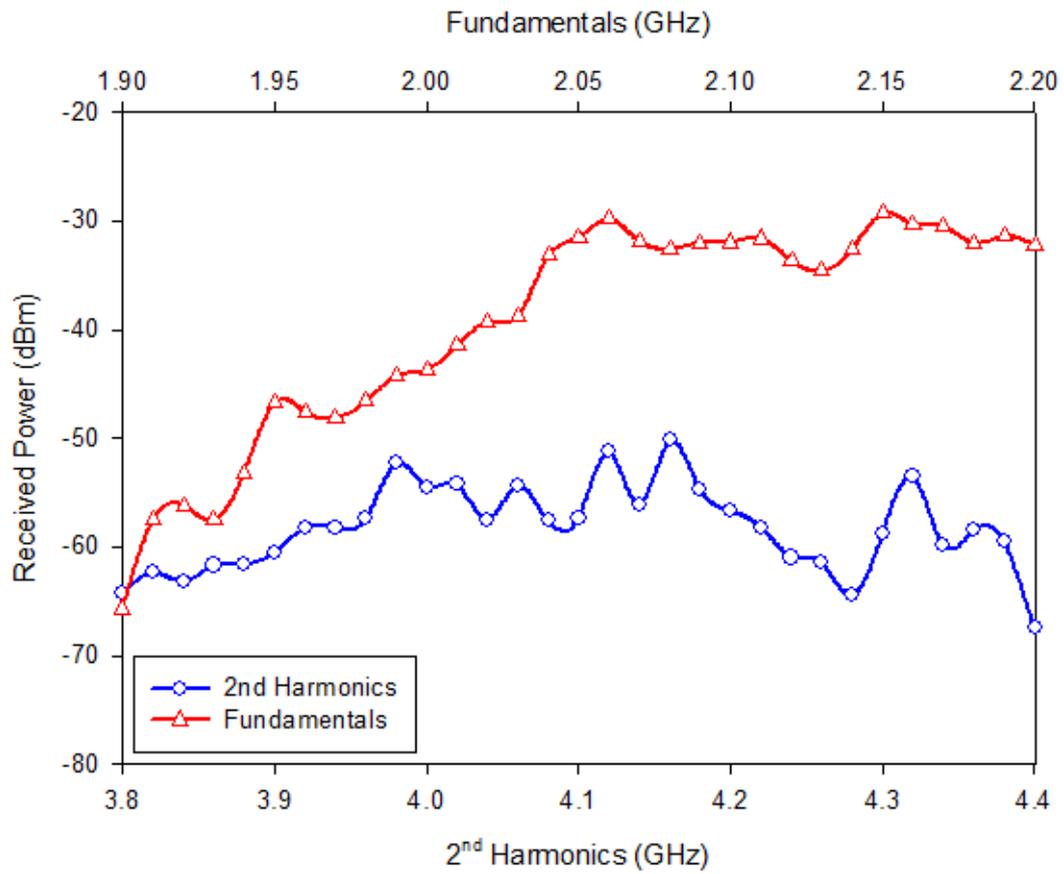


Fig. 5.11: Radiated power from the fundamentals and 2nd harmonics.

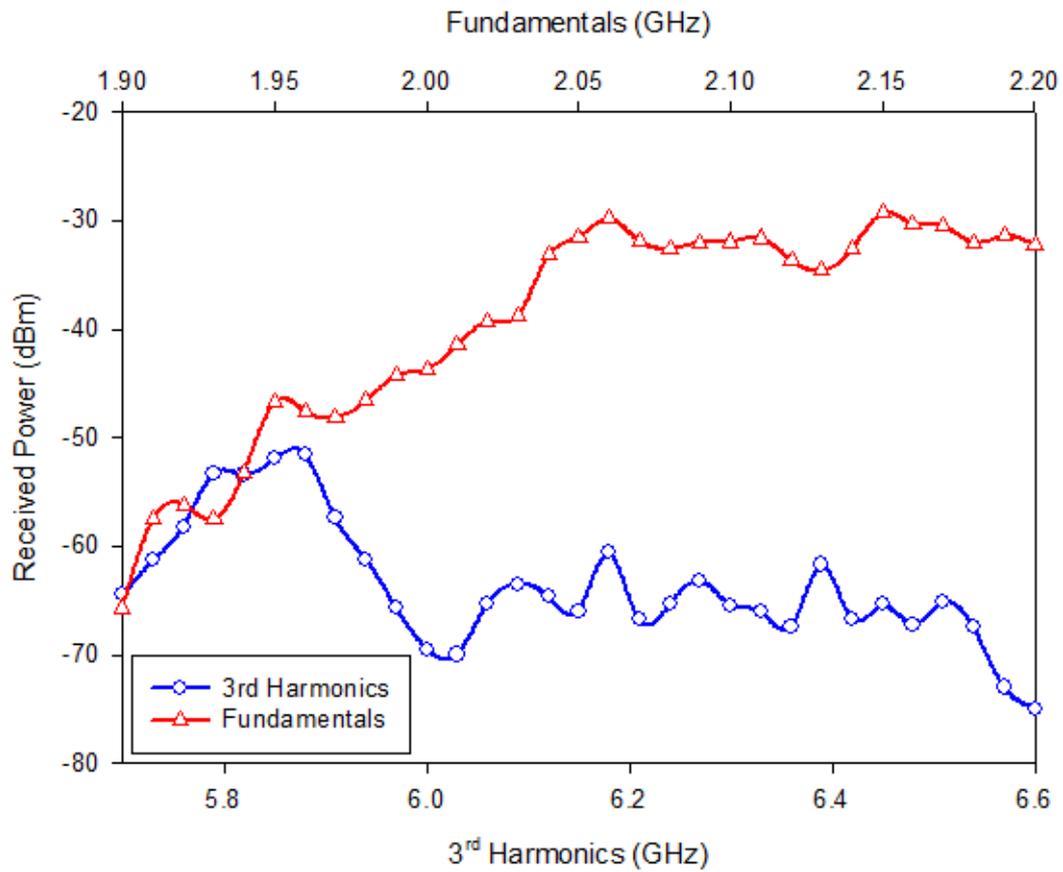


Fig. 5.12: Radiated power from the fundamentals and 3rd harmonics.

5.8 Summary

One of the two passive EM structures which have been presented in the previous chapter was chosen to be realised as a fully integrated amplifier-antenna prototype. The transformation of an ideal push-pull amplifier into a version of fully integrated push-pull transmitting amplifier is presented. Comparison between an ideal and the prototype was made by simulation before any further characterisation was carried out. This is to ensure the prototype will behave similarly to its ideal version and it can only be done by comparing the waveforms at the selected node in

circuitry. However, the on-bench testing is still necessary before a proper measurement being carried out in the anechoic chamber. This is solely for ease of troubleshooting in order to ensure the prototype is credible to operate when real measurement takes place.

Measured results have validated a proposed technique for direct integration of power amplifiers and antennas. The measured received power from a prototype is generally higher than that of its passive version while the harmonics are also have been quite well suppressed. This actually demonstrates an efficient power combining from a differential output active circuit to an antenna without any bond wires which are physically connected is achieved. This prototype can be used in many applications where differential signals are used such as in transceivers. This novel technique allows freedom to adjust and optimize the EM structure based on the amplifier outputs.

Even though there is only a relative measurement between two approaches, it is considered to be convincing that our new prototype is working in class-B mode since their waveforms characteristic consistency at the same nodes for both ideal push-pull amplifier (Fig. 5.1) and the new prototype (Fig. 5.5) have been assessed by simulation earlier in the previous section. Therefore, it can be assumed that the new prototype will be having and share the same characteristic of class-B power amplifier.

CHAPTER 6

SUMMARY, CONCLUSION AND FUTURE WORKS

6.1 Summary

In this thesis, a novel technique for direct integration of power amplifiers and antennas has been established by demonstrating its feasibility through simulation and experiment. This novel technique suggests that the design variables of the EM structure can be systematically manipulated in order to discover every possible point of impedance matching on the Smith chart so that a wide range of impedance matching requirements could be met for any given devices and bias conditions with no issue on degradation in antenna performance such as bandwidth, radiation pattern and gain when these key parameters have been varied in order to achieve impedance matching. In this case, it was assumed that the presence of the ground plane between the layers caused the positioning of the stubs relative to the aperture/slot not to affect the radiation pattern and simultaneously improving the gain whilst maintaining other antenna performances such as bandwidth and beamwidth [93]. Therefore, this technique has been applied to develop a fully integrated antenna-amplifier front-end.

Initially, the idea was to take advantage of the fruitful use of differential feeding technique. Since the push-pull amplifier configuration uses this kind of

feeding technique, the EM structure which is adapted from the differentially fed aperture coupled antenna is incorporated at the output stage within push-pull amplifier architecture. This not only eliminates the losses due to 180° hybrid coupler which is typically around $1.2 - 1.5$ dB within frequency range of 30 MHz – 3 GHz [97], it also enhances the immunity from common mode interference and improves the overall system efficiency. In term of space saving benefits, it is estimated that one 180° hybrid coupler occupies about 25% of the overall prototype's size. The conventional push-pull amplifiers used two 180° hybrid couplers in which it adds another 25% to the overall size. Therefore, the idea is to replace the output hybrid coupler with the one which allows the power combiner and output matching network functions to be integrated into the two-port antenna structure.

Besides, this novel technique has also been applied to the other type of transistor with different biasing conditions as well. The same type of two-port EM structure and power amplifier architecture which are aperture coupled antenna and push-pull amplifier respectively have been used in the integration process with no problem encountered. This concept explained that two-port antenna structure allows good coverage of the Smith chart, hence a good impedance matching requirement could be met. In a nutshell, the concept and theory applied in this work can offer advantages of neat and tight integration of push-pull transmitting amplifier. Furthermore, controlling other higher harmonic impedances using open-circuit stubs has been shown to produce appropriate-shaped output waveforms for Class B operation.

6.2 Conclusion

At microwave frequencies, a complex value of impedance matching requirement is vital in the design of active components and this is absolutely crucial to the overall front-end system performance. All resistance and reactance components respectively are required to be taken into consideration especially for direct integration of power amplifiers and antennas within the front-end systems. This is a very important consideration in order to avoid and remove the need for lossy networks such as transformer, balun and hybrid coupler in between the two subcircuit blocks. This could be a promising solution to realise a fully integrated push-pull transmitting amplifier in microwave transmitters, for instance.

In conventional push-pull architecture, there are baluns or hybrid couplers at the input and output stage as a power splitter and combiner respectively. Since the push-pull amplifier outputs used the concept of odd mode theory in a two-port network, this theory and concept has been extended to be applied for feeding a two-port antenna structure. An optimum impedance matching requirement should be met to integrate the push-pull outputs directly with a two-port antenna structure. A novel structure of differentially fed aperture coupled antenna has been specifically designed according to the matching requirement and biasing conditions imposed by the push-pull outputs. The prototype was then fabricated and successfully demonstrated the theory and concept through experiment.

In conclusion, this technique has removed the need for lossy matching elements and the output baluns by effectively incorporating the output matching

functions and power combiner into the two-port antenna structure. Besides, it is obviously very useful for direct integration of amplifiers and antennas since it can reduce the total loss and thereby improve the overall system performance efficiency for a wide range of wireless communication. Furthermore, the entire circuit configuration could be potentially integrated on a MMIC without having direct electrical connection using bond wires.

6.3 Future Works

There are good prospects on the works related to direct integration of active devices and EM structures. The methods developed in this thesis could be applied to structures in many different forms and architectures. This indicates that there are many possible works could be done to refill the research gaps in order to improve the existing constituent parts for better performance. For example, an investigation can be carried out to design EM structure which is effectively incorporating the output matching functions and power combiner for Doherty power amplifiers. This is quite challenging and complicated as there are two amplifiers that are working in different operation modes. The carrier amplifier should be in Class AB mode while the peaking amplifier is in Class C and their outputs have a phase difference of about 90° . This kind of power amplifier architecture has the potential of providing very high efficiency without losing its linearity.

On the other hand, although the benefits of microstrip as radiators in narrowband systems have been well established, it is rare to see dielectric resonators as the common choice of antennas in mobile communication systems. The attractive properties of dielectric resonator antennas (DRA) include wideband, low loss and great potential to be integrated with MMIC as the DRA could be a chip encapsulation. Further investigation can be carried out to apply this concept in ultra wideband (UWB) technology. The increasing demands for bandwidth in most communication applications make this UWB technology a promising solution. However, the works to establish fully integrated UWB front-end systems into MMIC would be a very challenging task to look into the integration issues.

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