Modular Multilevel Converter with Full-bridge Submodules for Flexible Medium Voltage DC Electric Railway Systems

by

Sina Sharifi

A thesis submitted to the University of Birmingham
for the degree of
DOCTOR OF PHILOSOPHY

Department of Electronic, Electrical
and Systems Engineering
School of Engineering
University of Birmingham
December 2022

UNIVERSITY OF
BIRMINGHAM

University of Birmingham Research Archive

e-theses repository

This unpublished thesis/dissertation is copyright of the author and/or third parties. The intellectual property rights of the author or third parties in respect of this work are as defined by The Copyright Designs and Patents Act 1988 or as modified by any successor legislation.

Any use made of information contained in this thesis/dissertation must be in accordance with that legislation and must be properly acknowledged. Further distribution or reproduction in any format is prohibited without the permission of the copyright holder.

Abstract

The idea of using DC railway electrification systems operating at medium voltage levels has been proposed in the literature. The Medium-voltage DC (MVDC) railway electrification systems are suitable options for the mainline and high-speed electric railways and have a wide range of advantages over the traditional AC and DC electrification systems. The benefits include but are not limited to less voltage drop, less impact on the public AC networks and possibility of connection to the low-voltage AC distribution networks, simple power supply diagram, and possibility of forming DC microgrids with the MVDC railway feeder as the main part.

Despite the advantages and due to practical challenges, MVDC railways have not been implemented in the railway industry. In particular, designing AC-DC power converters for the MVDC TPSs is one of the challenges towards developing the MVDC railways.

In this research, a 25 kV DC railway electrification system for the high-speed lines has been proposed. For the MVDC TPSs, a modular multilevel converter with full bridge submodules (MMC-FB) has been designed and a suitable control and modulation scheme for the MMC-FB has been developed. In the next step, the performance of the proposed MMC-FB and its controller has been evaluated by the MVDC railway simulation models in various operating scenarios.

Finally, the technical feasibility of the proposed control and modulation scheme has been investigated using a small-scale lab demonstrator of an MVDC TPS. Similar to the simulation results, the experimental results show the appropriateness of the MMC-FBs for the MVDC TPSs.

Acknowledgements

First, I would like to thank my parents and brothers for all their love, understanding and patience. Special thanks to Dr Soroosh Sharifi, Dr Narges Mahpeykar and Dr Delaram Sharifi for their great support from the beginning of my PhD studies and specifically during the dark days of the COVID-19 lockdowns.

My sincere thanks go to Dr Pietro Tricoli and Professor Clive Roberts for supervising my PhD project and their valuable helps, and Dr Stuart Hillmansen for assessing the annual progress reports.

I would also like to thank the friendly people at Birmingham Centre for Railway Research and Education (BCRRE), particularly Dr Tamer Kamel, Dr Tabish Mir, Dr Edward Stewart, Dr Paul Weston, Dr Mani Entezami and Mr Adnan Zentani. I would like to also thank Dr Ivan Krastev for his helps with the lab prototype.

This project has received funding from the Shift2Rail Joint Undertaking (JU) under grant agreement No 826238. The JU receives support from the European Union's Horizon 2020 research and innovation programme and the Shift2Rail JU members other than the Union.

Table of Contents

List of Figures

List of Tables

List of Abbreviations

Term	Explanation/Meaning/Definition
AI	Analogue input
AO	Analogue output
BCRRE	Birmingham centre for railway research and education
CSV	Comma-separated values
DCCB	DC circuit breaker
DG	Distributed generation
DO	Digital output
EMI	Electromagnetic interference
dq	direct-quadrature
FFT	Fast Fourier transform
FPGA	Field-programmable gate array
IGBT	Insulated gate bipolar transistor
IGCT	Integrated gate commutated thyristors
MMC-FB	Modular multilevel converter with full-bridge submodules
MVDC	Medium voltage DC
NI cRIO	National Instruments Compact RIO
PETT	Power electronic traction transformer
PI	Proportional - Integral
PV	Photovoltaic

Term	Explanation/Meaning/Definition
PLL	Phase-locked-loop
RMS	Root mean square
RT	Real-time
SFC	Static frequency converter
STATCOM	Static synchronous compensator
SVC	Static volt-ampere reactive compensator
SWOT	Strengths, Weaknesses, Opportunities, and Threats
TDD	Total demand distortion
THD	Total harmonic distortion
TPS	Traction power substation

1 INTRODUCTION

The mainline and high-speed electric railways are usually supplied by AC railway electrification systems at medium voltage level, which are single-phase supplies and cause imbalance on the three-phase public AC networks [1]. Therefore, the AC railways are typically connected to a high-voltage AC transmission line to mitigate the unbalanced loading issue [2]. This usually involves expensive equipment and connection works. In addition, high-voltage AC transmission lines are not always located near the railway traction power substations (TPSs), causing more cost for the railway electrification projects.

DC railway electrification systems draw balanced currents from the public AC networks using AC-DC power converters and they are usually used to supply urban railways and metros. This is because protecting DC lines needs complicated and costly DC circuit breakers [3], and thus, the voltage level of the DC electrification systems is limited to 4 kV [4]. This low voltage level, in turn, increases the voltage drop and transmission losses when the power consumption becomes higher.

Mitigating technical challenges of the traditional DC electrification systems can lead to development of a new electrification system for the high-speed lines with higher DC voltage levels such as 25 kV DC. Having low impact on the AC networks, power electronic converters make it possible to provide medium-voltage DC (MVDC) supply from widely available AC distribution networks. Moreover, it is possible to limit DC short-circuit currents by the power converters [5] and reduce the current ratings of the DC circuit breakers. Thanks to fully controlled bidirectional converters, the MVDC railway electrification system can be well integrated with the AC distribution networks, supporting the networks by consuming/producing reactive power [1]. Moreover, the

MVDC railways can have enough power capacity to integrate renewable power sources and create an MVDC microgrid. For instance, Figure 1.1 shows an MVDC microgrid where the distribution network, renewable energy sources, distributed generation units (DGs), and energy storages can flexibly interact with the railways [1], [3].

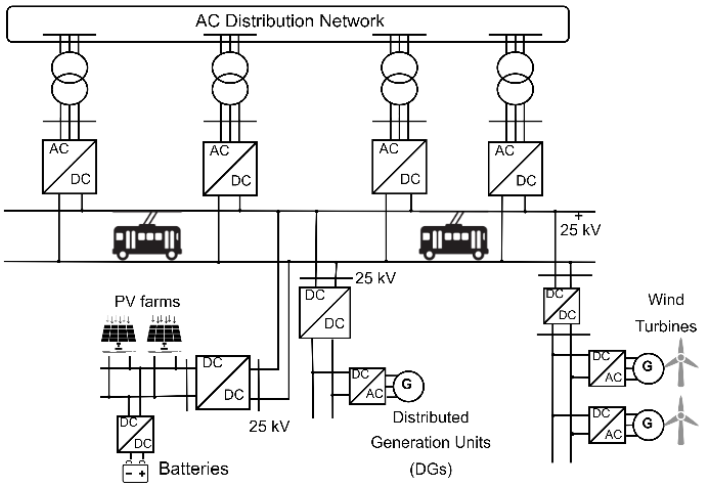


Figure 1.1 - MVDC railways as a part of a microgrid

In addition, the reactance of the overhead lines is theoretically zero in steady state, and thus, the voltage drop and reactive power consumption would be less than the AC railways [6]. Having no skin effect, the MVDC overhead lines can be realised with smaller cross-sectional area and lower cost [1]. In contrast to the AC railways, there is no need to implement neutral sections in the MVDC railways and the MVDC TPSs can be easily paralleled, which leads to reduction of the TPS power ratings [1], [7]. Inexistence of the neutral sections also simplifies the power diagram of the supply system and avoids power interruption and speed loss [7].

1.1 Research objectives

Despite the advantages and due to practical challenges, MVDC railways have not been implemented in the railway industry. In particular, designing AC-DC power converters for the MVDC TPSs is one of the challenges towards developing the MVDC railways.

This is because the MVDC railway networks have unique characteristics which make them different from other MVDC networks. For instance, the electric trains are located between the network nodes and their power profile is dramatically changed during traction cycles (acceleration, coasting and braking). The power converter of the MVDC TPSs should be able to control the active and reactive power transfer between the MVDC railways and public AC networks while complying with power quality standards. Moreover, the MVDC TPS converter must have DC short-circuit current controller to tackle MVDC overhead line protection issue.

The aim of this research is to propose an MVDC railway electrification system for high-speed lines. As one of the main elements of the system, this research focuses on power converter of the MVDC TPSs. Based on the literature review and among the high-power AC-DC converter topologies suitable for the medium-voltage applications, modular multilevel converter with full bridge submodules (MMC-FB) has been found to be a promising topology for the MVDC TPSs. Hence, an MMC-FB is designed for the proposed MVDC electrification system and its performance is evaluated under various operating conditions. This overarching aim is achieved through the following objectives:

- To review the feeding arrangements proposed for the MVDC railway electrification systems in the technical literature.
- To define the specifications of the proposed MVDC electric railway system.
- To design an MMC-FB for the MVDC TPSs and propose a control and modulation scheme for the MMC-FB.
- To validate the MMC-FB design and the proposed control and modulation scheme by simulating an individual MVDC TPS equipped with the MMC-FB.

- To estimate the MMC-FB losses and its efficiency curve under various load conditions using the developed simulation model.
- To assess performance of the MMC-FBs in a double-end fed MVDC railway in the presence of renewable power sources by extending the simulation model.
- To analyse performance of the MMC-FBs in a MVDC railway network with multiple TPSs by an expanded simulation model.
- To build a small-scale lab demonstrator of an individual MVDC TPS and assess the control and modulation scheme proposed for the MMC-FB using the hardware setup.

1.2 Publications

Several parts of this PhD research project have been published in a peer-reviewed journal and two international conferences:

- **S. Sharifi**, I. Ferencz, T. Kamel, D. Petreuș, P. Tricoli, "Medium-Voltage DC Electric Railway Systems: a review on feeding arrangements and power converter topologies", IET Electrical Systems in Transportation, vol. 12, no. 4, pp. 223–237, September 2022.
- **S. Sharifi** and P. Tricoli, "Medium voltage DC (MVDC) railway electrification systems: Assessment of performance," in World Congress on Railway Research 2022, June 2022.
- **S. Sharifi**, T. Kamel, P. Tricoli, "Investigating the best topology for Traction Power Substations (TPSs) in a Medium Voltage DC (MVDC) railway electrification system", in 23rd European Conference on Power Electronics and Applications (EPE'21 ECCE Europe), September 2021.

The research has been also presented in Centre for Power Electronics (CPE) Annual Conference 2021:

- **S. Sharifi**, P. Tricoli, C. Roberts, "Flexible Medium Voltage DC Electric Railway System," in Centre for Power Electronics (CPE) Annual Conference, July 2021, poster presentation.

The work presented in this thesis has been undertaken as part of Flexible medium voltage DC electric railway systems (MVDC-ERS) project funded by Shift2Rail Joint Undertaking (JU) under grant agreement No 826238.

1.3 Thesis outline

The rest of this PhD thesis is organised as follows:

Chapter 2, 'Literature review', reviews the commonly used railway electrification systems and the feeding arrangements proposed for the MVDC railways in the literature. Moreover, it presents the high-power AC-DC converter topologies suitable for the MVDC TPSs.

Chapter 3, 'modelling the proposed MVDC electric railway system and modular multilevel converter', introduces the proposed MVDC railway electrification system and presents the methodology used for modelling the MVDC railway system, MMC-FB, proposed control and modulation scheme for the MMC-FB, and DC short-circuit current controller. Finally, this chapter discusses the MMC loss modelling.

Chapter 4, 'Simulation analysis of MVDC railways', describes the performance of the MVDC railway system in various simulation cases. It also presents the results for the loss estimation using the simulation model.

Chapter 5, ‘Experimental setup of an MVDC TPS, introduces the hardware and software design of the small-scale lab demonstrator devolved for an individual MVDC TPS.

Chapter 6, ‘Experimental results’, discusses the performance of the small-scale lab demonstrator tested under constant DC loads, DC load change, and DC-side short-circuit.

Chapter 7, ‘Conclusion and future work’, draws conclusions of this research project and presents the possible areas of research related to the MVDC railways.

2 LITERATURE REVIEW

2.1 Conventional railway electrification systems

Currently, there are various kinds of electric traction systems around the world. The first electric traction systems were based on DC power supplies. The most notable events in early stages of development of traction systems have been presented in Table 2.1.

Table 2.1 - Notable events in development of traction systems [4], [8]–[10]

Notes	Date	Location
Experiments on battery propulsion	1837	Massachusetts, USA
Experiments on battery propulsion	1838	Scotland
Power supply along with traction line – The use of small DC locomotive	1879	Berlin, Germany
Electric tram line	1881	Berlin-Lichterfelde, Germany
Electric railway	1883	Brighton, UK
Electric streetcar line	1884	Cleveland, Ohio, USA
Tramway network with simple overhead wire	1886	Montgomery, Alabama, USA
Electric tramway network with sprung DC motors - speed control using rheostat and field control	1888	Richmond, Virginia, USA
Underground electric traction in urban areas	1890	London and Liverpool, UK
Underground electric traction in urban areas	1895	Baltimore, Maryland, USA

Initially, the electric traction systems were mainly realised by DC or single-phase AC (universal) motors [4]. Based on the requirements of these traction motors and other technical and regional matters, the electric traction systems have been developed in various paths. Expansion of low-voltage DC systems, and emerging medium-voltage AC systems were two major technical solutions. While in Central Europe, the frequency for the AC electrification systems was selected to be $16\frac{2}{3}$ Hz, it was chosen to be 25 Hz in the United States of America. The medium-voltage AC electrification system with 50 and 60 Hz was also implemented in 1950s and introduced as a replacement for some of the old low-voltage DC railways [11].

The commonly used railway electrification systems are classified in Figure 2.1 and are discussed in the following sections.

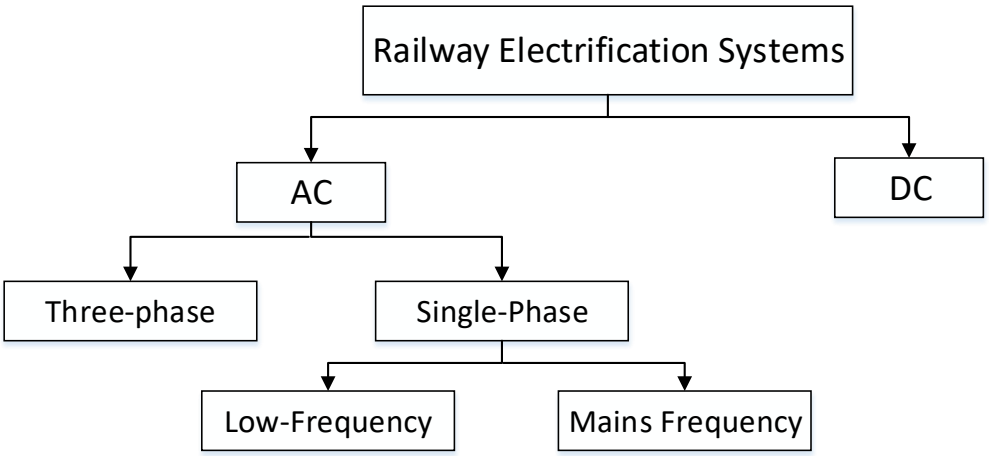


Figure 2.1 - Commonly used railway electrification systems

2.1.1 Low-voltage DC systems

Having torque-speed characteristics compatible with the traction cycles, separately excited and series DC motors were suitable for the trains [11] and hence, the DC supplies were appropriate solutions in the earliest stages of the railway systems development. First, DC electrification systems with nominal voltages around 0.5 kV were developed to supply trams and metros. Having high voltage drops and power

losses, these systems were not able to supply the lines with high traffic volume. Therefore, the DC systems with higher nominal voltages, e.g. 0.75, 1.5, and 3 kV were introduced [4]. Moreover, 3 kV DC systems were developed in the United States of America between 1914 to 1916 [12]. Following this, 4 kV DC railways were used for Torino-Ceres railway in Italy in 1920 [4]. The DC systems with nominal voltages higher than 3 kV were also implemented in Belgium, Poland and Spain [1].

To use DC electrification systems for the mainlines and high-speed railways, it was needed to further increase the voltage level to decrease the power losses and voltage drops. However, the voltage level of DC systems was limited to 4 kV, mainly because of protection matters. In fact, DC circuit breaker suitable for higher voltage and current ratings were expensive and complicated due to lack of zero-crossing in DC voltages and currents. As a result, medium-voltage AC systems were chosen as suitable systems for the high-speed railways.

2.1.2 Single-phase AC systems with low frequency

The single-phase AC railway electrification systems with low frequency have been used in the United States of America and European countries such as Switzerland, Germany, Sweden, Austria and Norway. In these systems, on-board transformers are used to step down overhead line voltage (10 – 15 kV) to the voltage levels appropriate for the motor drives. As two examples, the New York – New Haven line was electrified by 11 kV, 25 Hz system in 1906 and the Dessau-Bitterfeld line was realised by 10 kV, 15 Hz supply system in 1911 [4].

The series commutator motors were mainly used as traction motors in the AC railways. These motors had high maintenance costs due to sparks during commutation process. As the number of sparks is proportional to the frequency of the supply system, the

system designers decided to reduce the supply frequency to $16\frac{2}{3}$ (where the mains frequency is 50 Hz) or 20 – 25 (where the mains frequency is 60 Hz). In addition, choosing lower frequencies has led to other technical advantages over the AC railways operating at mains frequency, such as less reactance and voltage drops and less skin effect in the overhead line conductors. The benefits in terms of voltage stability, electromagnetic compatibility and transmission losses have been also investigated in [13]. On the other hand, the on-board transformers in the low-frequency supply systems are bulkier and have negative impact on the system efficiency.

This electrification system can be developed in two forms [4]:

1) Centralised system, in which a dedicated power system consisted of generators and transmission and distribution lines is constructed for the railway network. Before 1900, this was the preferred form as the public grid was not widely available.

2) Distributed system, in which the railway lines are connected to three-phase public grids via frequency converters. This form, shown in Figure 2.2 , became more economical when the public grid and the railway loads were more expanded. In this configuration, the TPSs should be isolated by neutral sections when they are connected to different public grids with different phase and frequency.

Initially, rotating converters (electric machines with different number of pole pairs) were used for the frequency conversion. In 1980s and 1990s, the rotating converters were replaced by static cyclo-converters [14]. In cyclo-converters, thyristors are used to perform direct AC/AC conversion. The output waveform, however, is not purely sinusoidal and contains harmonic contents. Back-to-back converters were then proposed and implemented to tackle this issue. In these converters, insulated gate

bipolar transistors (IGBTs) or integrated gate commutated thyristors (IGCTs) are used to realise a rectifier and an inverter stage to indirectly convert the frequency.

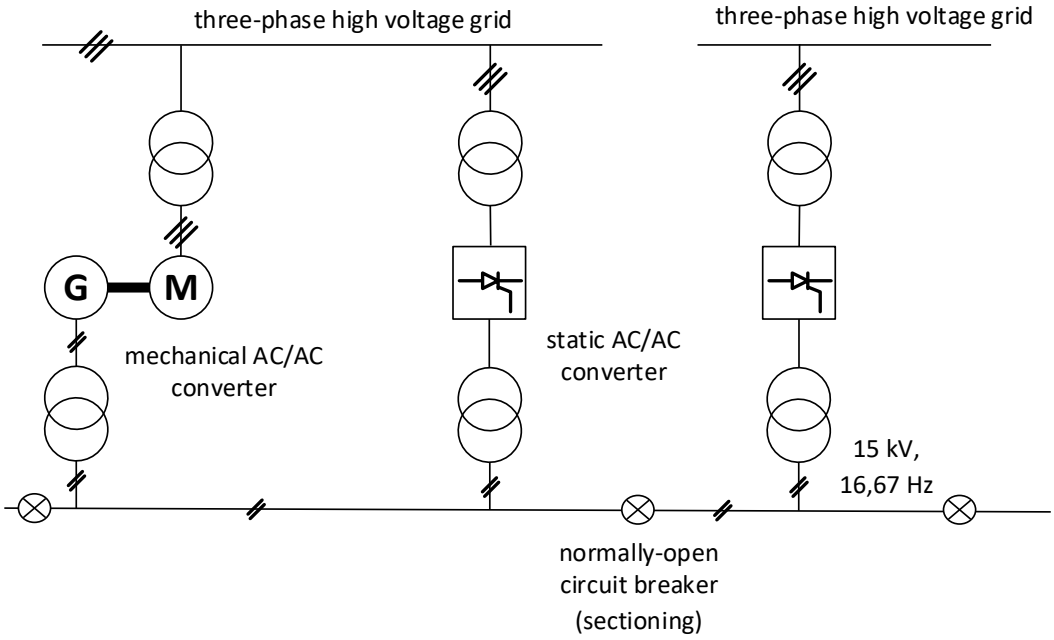


Figure 2.2 - low-frequency AC railways - Distributed form [4]

2.1.3 Single-phase AC systems operating at mains frequency

Development of static rectifiers after the World War II made it possible to feed the DC traction motors by an AC supply system. Therefore, the AC supply systems could be directly connected to the public AC networks without frequency conversion. In addition, motor drives were developed enough to drive three-phase induction motors [4], providing more options for selecting traction motors.

The 25 kV, 50 (60) Hz electrification system is widely used for mainlines and high-speed railways. Figure 2.3 illustrates a typical 25 kV AC railway electrification system [15], where the traction transformers of the substations feed the trains. Supplying single-phase AC railways from the three-phase mains grid causes unbalanced loading issue. Hence, the adjacent substations are fed by different phases of the mains grid to

reduce this negative effect. As a result, the substations should be isolated by neutral sections.

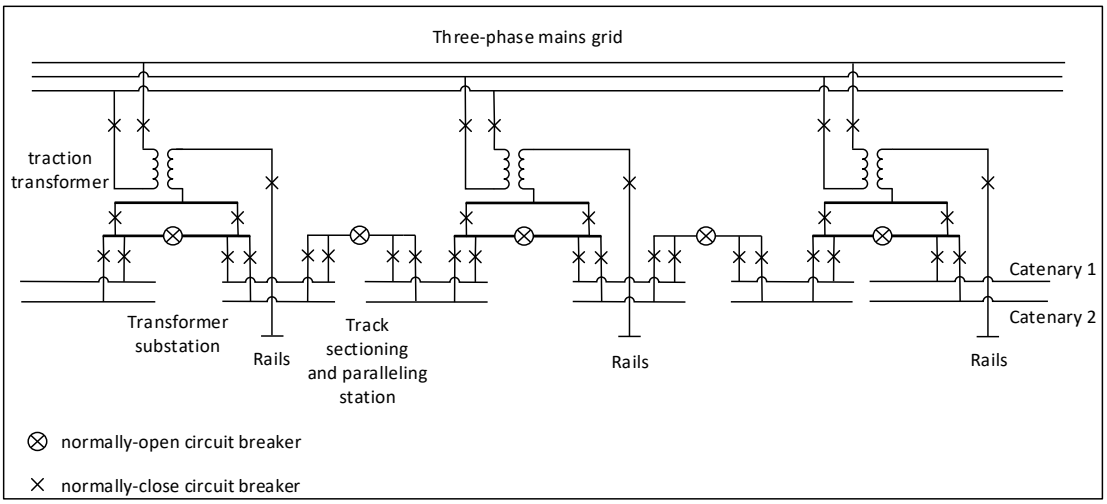


Figure 2.3 - A typical 25 kV, 50 (60) Hz supply system [15]

There are various configurations for realising 25 kV, 50 (60) Hz systems. The simplest arrangement, shown in Figure 2.4 (a), consists of a transformer directly connected to the railway supply system. This arrangement, however, suffers from high line impedance and voltage drops, considerable rail-to-earth potential difference and safety issues, and high ground currents which might cause interference with the adjacent communication devices [15].

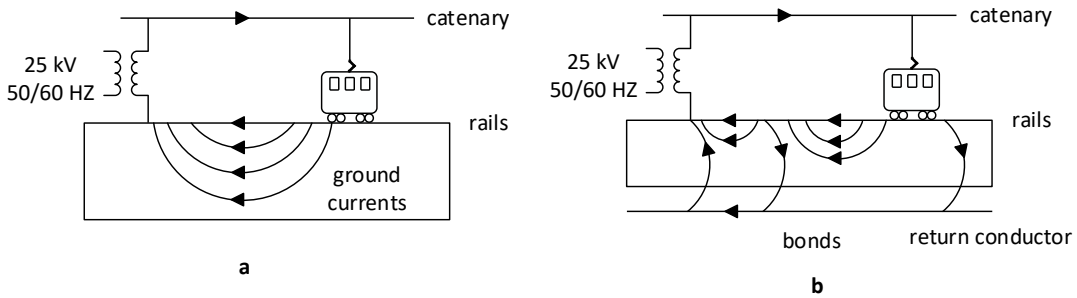


Figure 2.4 - Various configurations for 25 kV, 50 (60) Hz railways [15]*: a) Direct connection via a transformer b) Direct connection via a transformer and a return conductor*

As depicted in Figure 2.4 (b), a return conductor bonded to the rails can reduce the return path impedance. Another solution is to use booster transformers, installed in every 3 – 4 kilometres. According to Figure 2.5 (a), the booster transformers with unity turns ratio are installed between the overhead lines and rails. In this way, almost all the return current flows through the secondary of the booster transformer. Figure 2.5 (b) presents an alternative for this arrangement, where a return conductor is installed together with the booster transformers to absorb the return current.

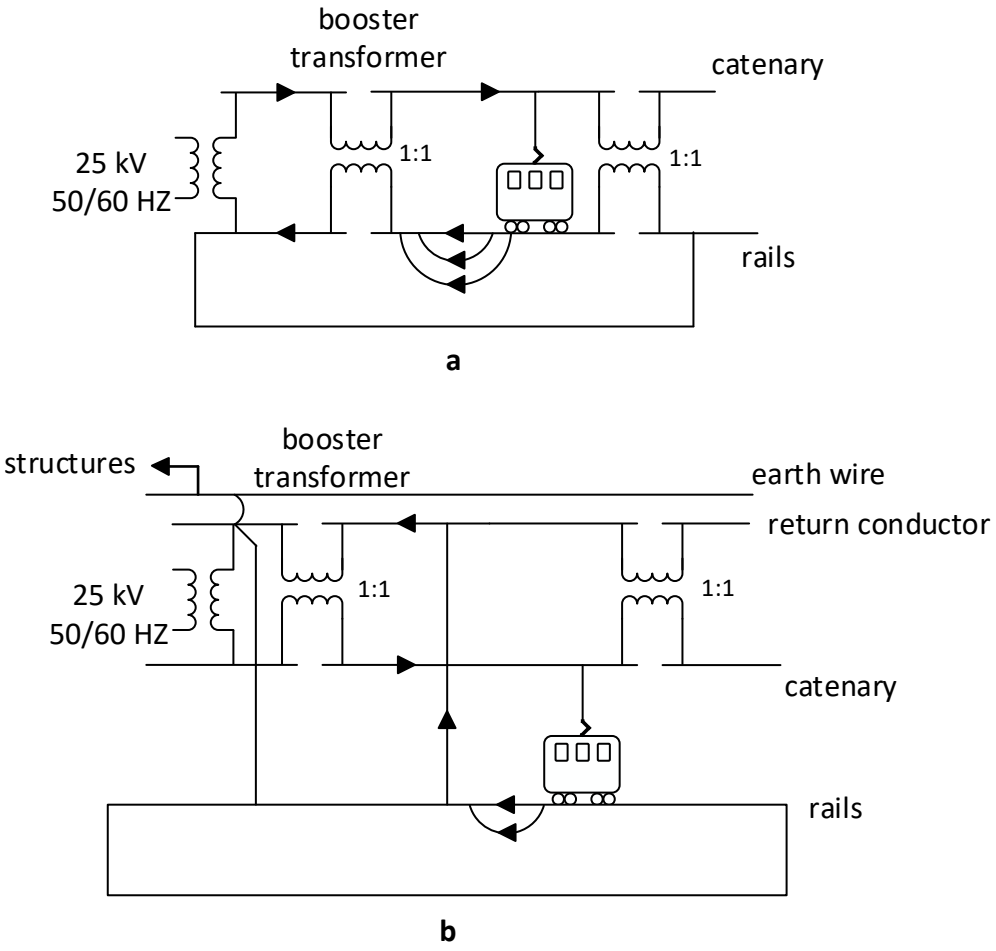


Figure 2.5 - 25 kV, 50 (60) Hz railways with (a) Booster transformer (b) Booster transformer and a return conductor [15]

Figure 2.6 demonstrates another established arrangement for the 25 kV, 50 (60) Hz railways, which consists of autotransformers with unity turns ratio connected to the

overhead lines and an auxiliary feeder. The centre tap of the autotransformer is connected to the rails, and the voltage on the primary side is 50 kV. Therefore, the trains are supplied at 25 kV but the input voltage is higher (50 kV). This makes it possible to increase the distance between the traction substations. In addition, the return current is forced to flow through the autotransformers.

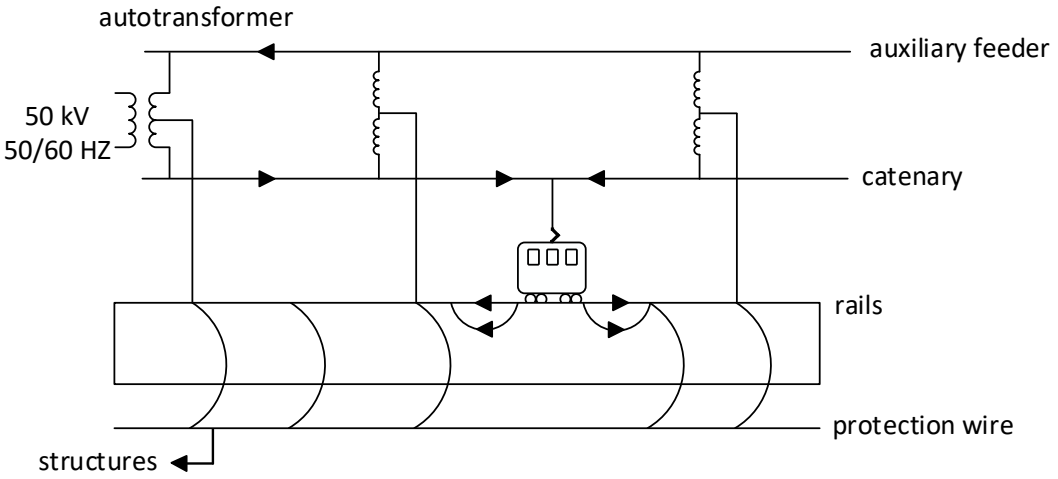


Figure 2.6 - Implementation of autotransformers in 25 kV, 50 (60) Hz railways [15]

As mentioned, the single-phase 25 kV railways cause imbalance on the three-phase public AC networks. Hence, these electrification systems are typically supplied by a high-voltage AC transmission line [2]. Balanced transformers have been proposed and used to alleviate the unbalanced loading problem by creating a balanced two-phase system. Impedance matching, Le-Blanc, Scott, and Woodbridge transformers are the most notable designs. In addition, the use of balanced transformers can attenuate harmonic distortions in some cases. Nevertheless, these transformers cannot entirely solve the unbalanced loading issue, since they operate as a balanced three-phase transformer only when the output phases are equally loaded [2], and this is not usually the case.

The imbalanced loading and voltage drops can also be reduced by Static volt-ampere reactive compensators (SVCs). The SVCs uses thyristors to switch reactors and/or capacitors. The switching of the thyristors, however, produces unwanted harmonic contents which should be filtered by bulky passive filters. The Static synchronous compensators (STATCOMs) are also a solution for improve the power quality on the public AC networks. Operating based on switch-mode converters, STATCOMs are able to act as active filters and eliminate the unwanted harmonic contents produced by the railway network with smaller filters than those implemented in SVCs [14].

The 25 kV 50 (60) Hz railways are also realised by Static frequency converters (SFCs). In these converters, the three-phase AC voltage is rectified to DC voltage in the first stage, and it is converted to single-phase 50 (60) Hz voltage for the railway network in the second stage. Therefore, the railway TPSs draw balanced and high-quality currents from the three-phase AC network, and thus, the railway network can be connected to the AC networks with lower voltage levels and the neutral sections can be removed from the railway system. In addition, the power factor and short circuit currents can be fully controlled by the converters. It is also possible to share the load among the TPSs in the railway network [14]. On the other hand, SFCs are more complex and generally less energy-efficient in comparison to the transformers.

2.1.4 Three-phase AC systems with low frequency

The three-phase asynchronous motors became an option for the traction applications in the early of the twentieth century. Feeding these motors via feeders with voltage level of a few kV was technically viable, and this led to development of a three-phase AC railway electrification system. As there were no reliable adapter gear units available at that time, the motors were connected to the train wheels by means of a crank. Hence,

the motor speed was limited to the speed of the wheels and the trains speed was controlled by changing the number of poles of the motors. To operate the trains at 50-60 km/h speed and less, the supply frequency had to be reduced.

A three-phase 16.7 Hz electrification system was developed in Switzerland in 1985 [4]. The three-phase railway supplies were also implemented in Italy, Hungry and United States of America. The voltage level of the overhead lines was chosen up to 3 kV, and the motors were supplied by two parallel overhead lines [4].

Due to insulation considerations, the structure of the overhead lines was complicated at junctions. In addition, the trains speed was limited to 100 km/h because of two-wire contact lines and mechanical constrains linked to them. In addition, because of the strong coupling between motor speed and synchronous speed, speed control was difficult. Furthermore, there were ripples in the power consumed by the motors as a result of the rigid connection between the motors and wheels, causing interference with the nearby communication lines [4].

After a few years of operation and because of the technical issues, the three-phase railway supplies were abandoned in almost all countries and were replaced by low-frequency single-phase AC or DC railways.

2.2 Proposed feeding arrangements for MVDC railways

The idea of increasing voltage level of the DC railway electrification systems has been proposed since 1989 [16]. However, this system has not been implemented in the railway industry due to technical challenges. The feeding arrangements proposed for the MVDC railways can be classified into two groups: 1) Systems with MVDC intermediate feeders; and 2) Systems with MVDC overhead lines. Appendix A presents

the review paper published by the author of this PhD thesis in which these proposals are thoroughly reviewed (section 2).

Table 2.1 presents a Strengths, Weaknesses, Opportunities and Threats (SWOT) analysis for the MVDC railway electrification system to demonstrate its advantages over the traditional solutions and elaborate the challenges. Some of the strengths and opportunities are demonstrated in this thesis. This thesis also deals with the weakness related to the design and development of the power converters for the MVDC TPSs.

Table 2.2 - SWOT analysis for MVDC railway electrification systems

Strengths	**Weaknesses**
- Low impact on the main three-phase AC networks (no imbalanced loading) - Ability of limiting DC short circuit currents by power converters - Facilitating the integration of renewable power sources and creating microgrids - Negligible voltage drop and reactive power consumption due to negligible reactance in steady state - Simple power diagram without neutral sections - No skin effect in the overhead lines and smaller and lighter overhead lines - Having less conversion stages in the power converters and possibly higher power efficiencies (in comparison to 25 kV AC railways realised by static frequency converters)	- The need for DC circuit breakers and more expensive protection equipment - Lack of experience in topology selection, design and development of the power converters for the MVDC TPSs - Power losses in the power electronic converters (both in TPSs and in PETTs) - Complex central control unit and the need for bidirectional data transfer (in the case of implementing power sharing schemes) - Possibility of corrosion on installations
Opportunities	**Threats**
- Possibility of using the same infrastructure as 25 kV AC railways - Integrating MVDC railways to widely available AC distribution networks rather than high-voltage AC transmission networks - Bidirectional active power transfer with the main three-phase AC networks (absorbing regenerated energy from the brakes, injecting generated power by the renewable resources to the main grid) - Providing reactive power support for the main three-phase AC networks - Possibility of power sharing between the MVDC TPSs and reducing the power capacity of the TPSs. - Possibility of increasing the speed of the trains (as there are no neutral sections, and thus, there are no power interruptions)	- The reliability of the TPSs and PETTs needs to be evaluated - There are research areas which need to be further investigated (as will be discussed in section 7.1 and section 4 of Appendix A) - There are no approved standards for the MVDC railways at the moment - The need for power electronic traction transformers (PETT) on the trains, which implies that all the rolling stocks need to be redesigned/modified

2.3 Converter topologies suitable for the MVDC TPSs

Considering the requirements of an MVDC railway electrification system with 25 kV overhead lines, the high-power AC-DC converter topologies have been analysed in the published review paper (Appendix A, section 3.1). Based on this study, MMC-FB has been identified as a feasible and promising solution for the power converters of the MVDC TPSs.

3 MODELLING THE PROPOSED MVDC ELECTRIC RAILWAY SYSTEM AND MODULAR MULTILEVEL CONVERTER

In this chapter, specifications of the proposed MVDC electric railway electrification system are defined. Then, an individual MVDC TPS is modelled, and the assumptions made in the modelling are discussed. The TPS converter, realised by MMC-FB topology, is the main part of the TPS. The MMC-FB designed for the MVDC TPSs and the proposed control and modulation units are described in detail. Finally, the method used for evaluating MMC-FB losses and efficiency is presented. The TPS modelling is done in Matlab/Simulink environment, and the simulation results are presented in the next chapter.

3.1 Specifications of the proposed MVDC railway electrification system

The arrangement for the proposed MVDC railway electrification system is illustrated in Figure 3.1. The AC-DC power converters of the MVDC TPSs provide DC voltage from AC distribution networks. In addition, a PETT is installed on each rolling stock to convert the MVDC overhead line voltage to the voltage levels suitable for the motor drives. The nominal voltage chosen for the proposed MVDC electrification system is 25 kV DC. In this way, the existing infrastructure for 25 kV AC railways can be used for MVDC railways in the future. In addition, MVDC railways with 25 kV feeders will have enough capacity to transfer energy between the renewable power sources, distribution network and railway TPSs.

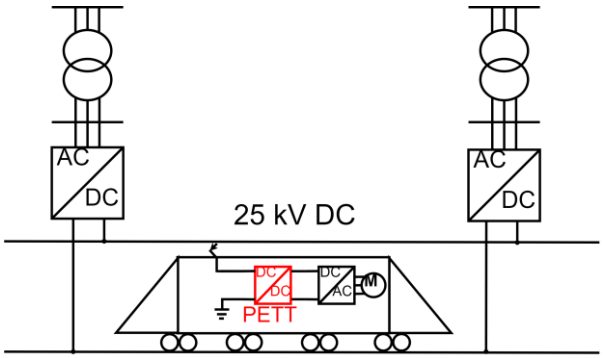


Figure 3.1 - The proposed MVDC railway electrification system

So far, MVDC railways have not been implemented in the industry. Therefore, there are no defined standards for their operation. As the operation conditions in MVAC and MVDC railways can be similar, the parameters defined in the standards for MVAC railways [17] are chosen for the proposed MVDC electrification system. Table 3.1 shows the assumed operational conditions.

Table 3.1 - Assumed operational conditions for the proposed MVDC railway electrification system

Parameter	Symbol	Value (kV)
Lowest non-permanent voltage	U_{min2}	17.5
Lowest permanent voltage	U_{min1}	19
Nominal voltage	$V_{DC,nom}$	25
Highest permanent voltage	U_{max1}	27.5
Highest non-permanent voltage	U_{max2}	29

The long-term overvoltages can last between 20 milliseconds and 1 second. The catenary voltage can drop to $U_{min2} < V < U_{min1}$ for no more than 2 minutes. In addition, the catenary voltage can increase to $U_{max1} < V < U_{max2}$ for a maximum duration of 5 minutes. In the no-load condition, the output voltage of a TPS should be equal to or less than U_{max1}. In this research, the no-load and nominal voltage selected is 25 kV DC.

For 25 kV AC railways, the highest long-term overvoltage (U_{max3}) is 38.75 kV. Considering that in AC systems, the Root Mean Square (RMS) of the nominal voltage is 25 kV while in DC systems the nominal voltage has a DC value of 25 kV, the highest long-term overvoltage for the MVDC electrification system can be smaller than that in AC railways. In this study, the value for U_{max3} is defined as U_{max2} + 10% = 31.9 kV.

The proposed MVDC electrification system is designed for high-speed lines. As a typical value, the maximum load for each TPS is considered to be 16 MW. To increase the reliability of the system, it is desired to have at least two AC-DC power converters in each MVDC TPS. In this case, one converter is used as a reserve converter. In this study and for simplicity, each TPS is designed with one power converter. As the semiconductors of the power converters cannot be overloaded, the TPS converters should be designed for the peak load. In addition, the TPSs should be able to handle low-duration overloads. Hence, a margin of 4 MW (25%) is considered, and the power rating for each TPS (and its converter) is assumed to be 20 MW. Table 3.2 shows the parameters selected for the MVDC TPSs and their power converters.

Table 3.2 - Parameters of MVDC TPSs

Parameter	Symbol	Value
Maximum consumption (for each TPS)	$P_{max,load}$	16 MW
Power rating of each TPS	$P_{rated,TPS}$	20 MW
Number of AC-DC converters in each TPS	N_c	1
Power rating of the power converter	$P_{rated,c}$	20 MW
Nominal DC voltage of the power converter	$V_{DC,nom,c}$	25 kV
DC current of the power converter at full load of 16 MW	$I_{DC,full,c}$	640 A
Maximum DC current of the power converter	$I_{DC,max,c}$	800 A

3.2 Model of the MVDC railway

Figure 3.2 depicts the power diagram for an MVDC TPS. Each MVDC TPS is connected to an AC distribution network and is equipped with a Y-Y transformer to provide a suitable voltage level for the TPS converter. In this study, the distribution voltage level chosen is 33 kV, and the TPS transformer provides 11 kV on the converter side. The distance between the TPS and distribution network is 0.5 km, and the AC cable parameters are selected based on [18].

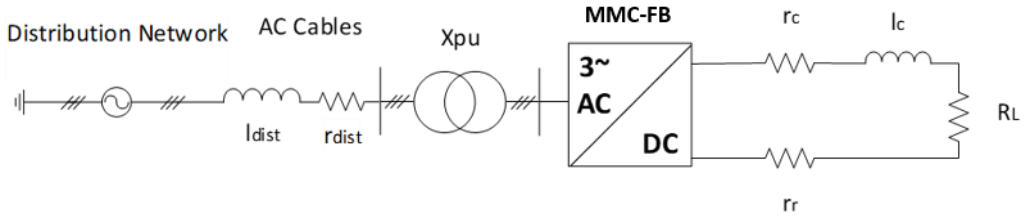


Figure 3.2 - The MVDC TPS model

The MVDC electrification system feeds the trains' load R_L through overhead lines, which are modelled by r_c and l_c. The running rails provide a path for return current. In the model, they are represented by r_r.

In this study, the simulation models are used to investigate the TPS converter's performance. Considering the converter's dynamic behaviour, the time span of the simulations is less than 1 second. During this time span, the trains' movement can be neglected. Therefore, the parameters for the overhead lines and running rails are constant during a simulation.

The MVDC system is a double-track railway system, i.e., the inbound and outbound trains are fed by two parallel feeding paths. Choosing contact wire conductors with a 150 mm^2 cross-sectional area for each feeding path, the equivalent inductance and

resistance of the overhead line equipment are assumed to be 1.55 mH/km and 0.16 Ω/km, respectively. The running rails in each path have 15 mΩ/km resistance [19].

Similar to the conventional railway electrification systems, the potential difference between running rails and ground (as a result of current leakage) causes safety issues. In addition, the return path should be a low-impedance path to avoid voltage drops and facilitating short-circuit current detection. Hence, earthing and bonding should be considered during the MVDC system design.

Due to the same voltage level in MVAC and MVDC railways, the methods used for earthing and boning can be similar, concentrating on electromagnetic interference (EMI) issues. It should be noted that at a same power level, the current level in a 25 kV DC railway is less than a 25 kV AC railway as the there is less reactive power consumption in the MVDC system. This implies smaller potential differences between the running rails and ground. The detailed design of earthing and bonding system for the MVDC railway system is out of scope of this thesis.

As the parallel overhead lines (and the running rails) are bonded together in a double-track MVDC system, they can be assumed as parallel impedances. Hence, the double-track system is modelled and simulated by only one path, and the overhead line equipment (and running rail) impedances are halved. Table 3.3 summarises the parameters used in the simulation models.

Table 3.3 - Parameters of MVDC TPS

Parameter	Symbol	Value
Distribution network frequency	f_g	50 Hz
Distribution network voltage level	V_{prim}	33 kV
Voltage on secondary side of TPS transformer (converter side)	V_{second}	11 kV
Apparent power of TPS transformer	S_t	20 MVA
Per unit resistance of TPS transformer	R_{pu}	1.1%
Per unit reactance of TPS transformer	X_{pu}	10%
Resistance of AC cables	r_{dist}	60.1 mΩ/km
Inductance of AC cables	l_{dist}	0.37 mH/km
Distance between TPS and distribution network	D_{dist}	0.5 km
Resistance of the overhead line equipment (double-track system)	r_c	80.0 mΩ/km
Inductance of the overhead line equipment (double-track system)	l_c	0.78 mH/km
Resistance of the running rails (double-track system)	r_r	7.5 mΩ/km

The developed model for an individual MVDC TPS is then extended to double-end fed and meshed MVDC railway system by connecting MVDC TPS models in Matlab/Simulink.

3.3 MMC-FB model

3.3.1 Power circuit

As shown in Figure 3.3, the MMC-FB power circuit consists of three legs, and each leg is formed by two arms. In each arm, there are N_{sub} full-bridge submodules and one arm inductor. Table 3.4 presents the parameters of the simulated MMC-FB.

The MMC-FB is designed for $U_{max3} = U_{max2}$ + 10% = 31.9 kV on the DC side. Therefore, it is realised by eight submodules per arm. In the worst-case scenario, the capacitors in each submodule should be charged up to $\frac{U_{max3}}{N_{sub}} = \frac{31.9\ kV}{8}$ = 4 kV. This means that each IGBT in the full-bridge submodules should be able to block 4 kV and the submodules can be realised by 6.5 kV IGBTs, considering enough safety margin

for their operation [20]. The MMC-FB design can be easily extended to operate at higher DC voltages by increasing the number of submodules in each arm. In other words, even if a U_{max3} higher than 31.9 kV is selected, the design of the MMC-FB does not change dramatically.

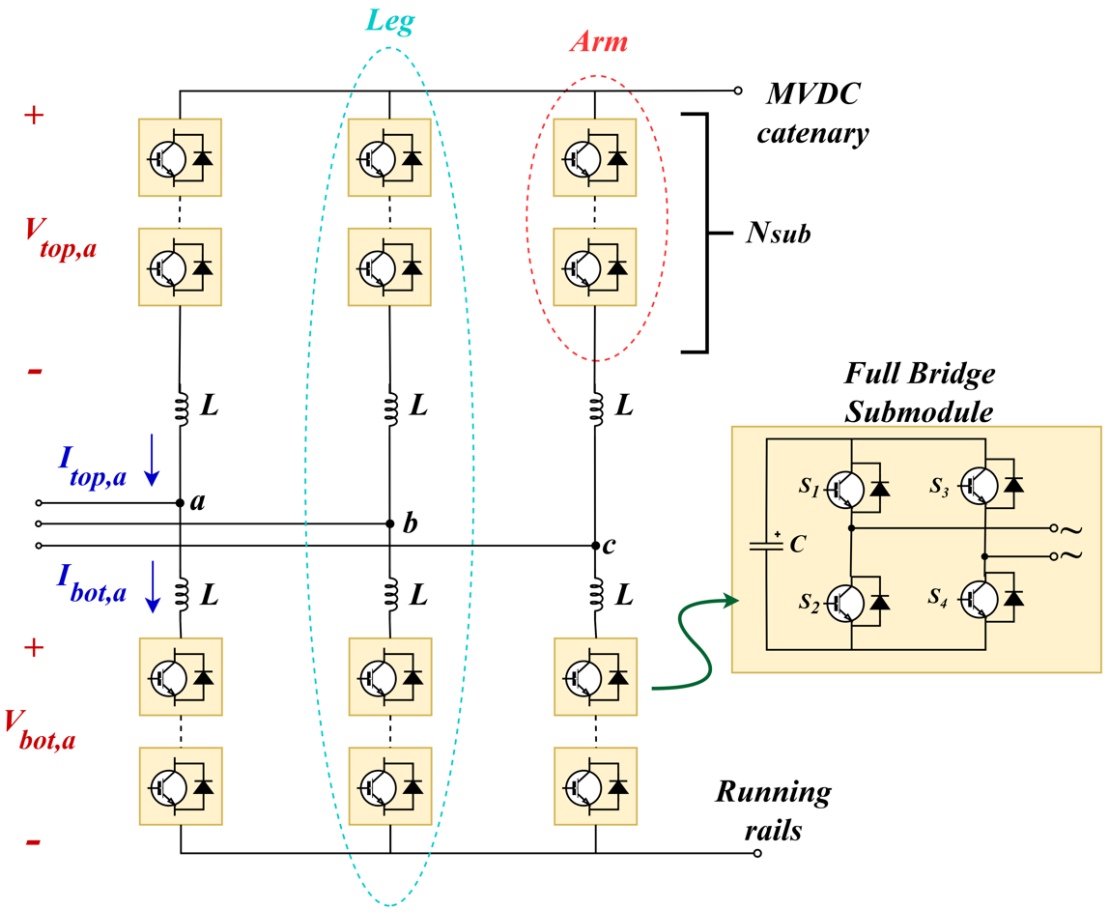


Figure 3.3 - Power circuit of the MMC-FB

Table 3.4 - Parameters of MMC-FB

Parameter	Symbol	Value
Number of submodules (per arm)	N_{sub}	8
Nominal voltage of the capacitor in each submodule	$V_{C,nom}$	3.13 kV
Capacitance (per submodule)	C_{sub}	10 mF
Arm inductance	L_{arm}	8 mH
Resistance of the arm inductor windings	R_{arm}	0.01 Ω
Carrier frequency	f_c	3 kHz

To select a proper IGBT for the MMC-FB, the maximum arm current needs to be evaluated. Assuming a lossless converter, displacement factor of 1 ((cos (φ_1) = 1) and modulation index of 0.7 (m = 0.7), the equations below estimate the maximum arm current. First, the maximum phase voltage on the AC side is calculated:

$$V_{AC,phase,peak} = \frac{1}{2} m\, V_{DC} \;\rightarrow\; V_{AC,phase,peak} = 8.75\ kV \tag{3-1}$$

After evaluating the maximum phase current on the AC side by (3-2), the arm current can be represented as in (3-3) [21]:

$$\frac{3}{2}\, V_{AC,phase,peak} I_{AC,phase,peak} = V_{DC}\, I_{DC} \tag{3-2}$$

$$I_{arm}(t) = \frac{I_{DC}}{3} \pm \frac{I_{AC,phase,peak}}{2} \cos(\omega t) \tag{3-3}$$

Considering the DC current of $I_{DC,max,c}$, the maximum value for the peak arm current is evaluated as follows:

$$\begin{aligned} I_{(AC,phase,peak)max} &= 1.52\ kA \\ I_{(arm,peak)max} &= \frac{I_{DC,max,c}}{3} + \frac{I_{(AC,phase,peak)max}}{2} = 1.03\ kA \end{aligned} \tag{3-4}$$

To consider the transients and the effect of the displacement factor, it is recommended to select an IGBT−diode module with a collector current rating of at least 1.3 kA. Alternatively, the submodules can be realised by four groups of parallel IGBT−diode modules with lower current ratings.

Figure 3.4 represents the TPS model developed in Matlab/Simulink using the Simscape library. To rectify some issues with the transformer block, the transformer impedance is modelled by setting the impedance parameters of the transformer block (0.002 pu), together with external resistance and inductances on the secondary side (R_s and X_s, 0.998 pu).

In some simulation cases, the trains' load is modelled by a controlled current source, where the current profile corresponds to a power profile at a fixed DC voltage of 25 kV. In the rest of simulations, the load is applied by a constant resistor corresponding to a specific power level at 25 kV DC. In the next chapter and for each simulation case, the load type is indicated.

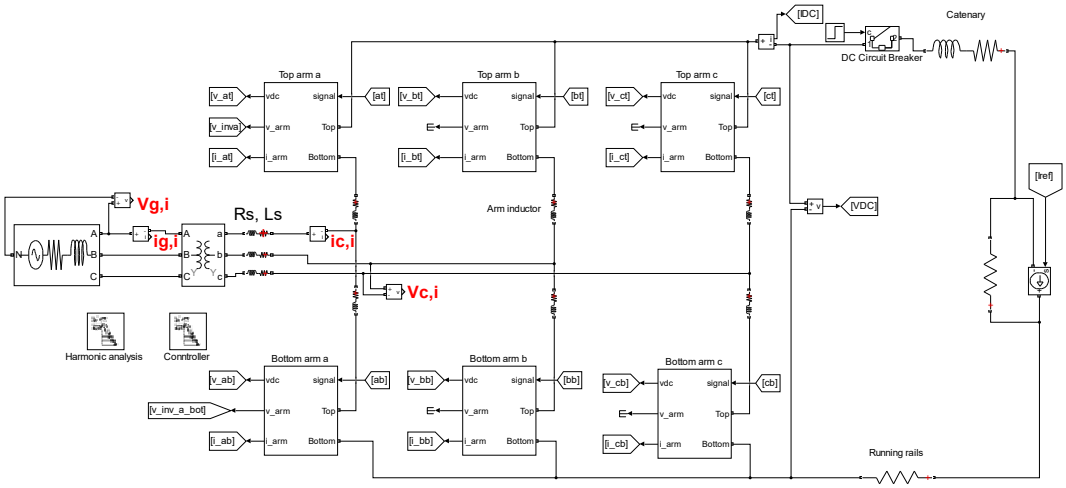


Figure 3.4 - The MVDC TPS modelled in Matlab/Simulink

3.3.2 Control scheme

The proposed control scheme for the MMC-FB is designed in a direct-quadrature (dq) frame. The principle of the control scheme is similar to that of grid-connected two-level converters in the dq frame [22]. However, the outer control loop in the d axis is designed differently. Figure 3.5 shows the implemented MMC-FB controller, which mainly consists of outer and inner control loops. The overall schematic of the control system and the Proportional−Integral (PI) controller gains used in the MVDC TPS simulations are presented in Appendix B.

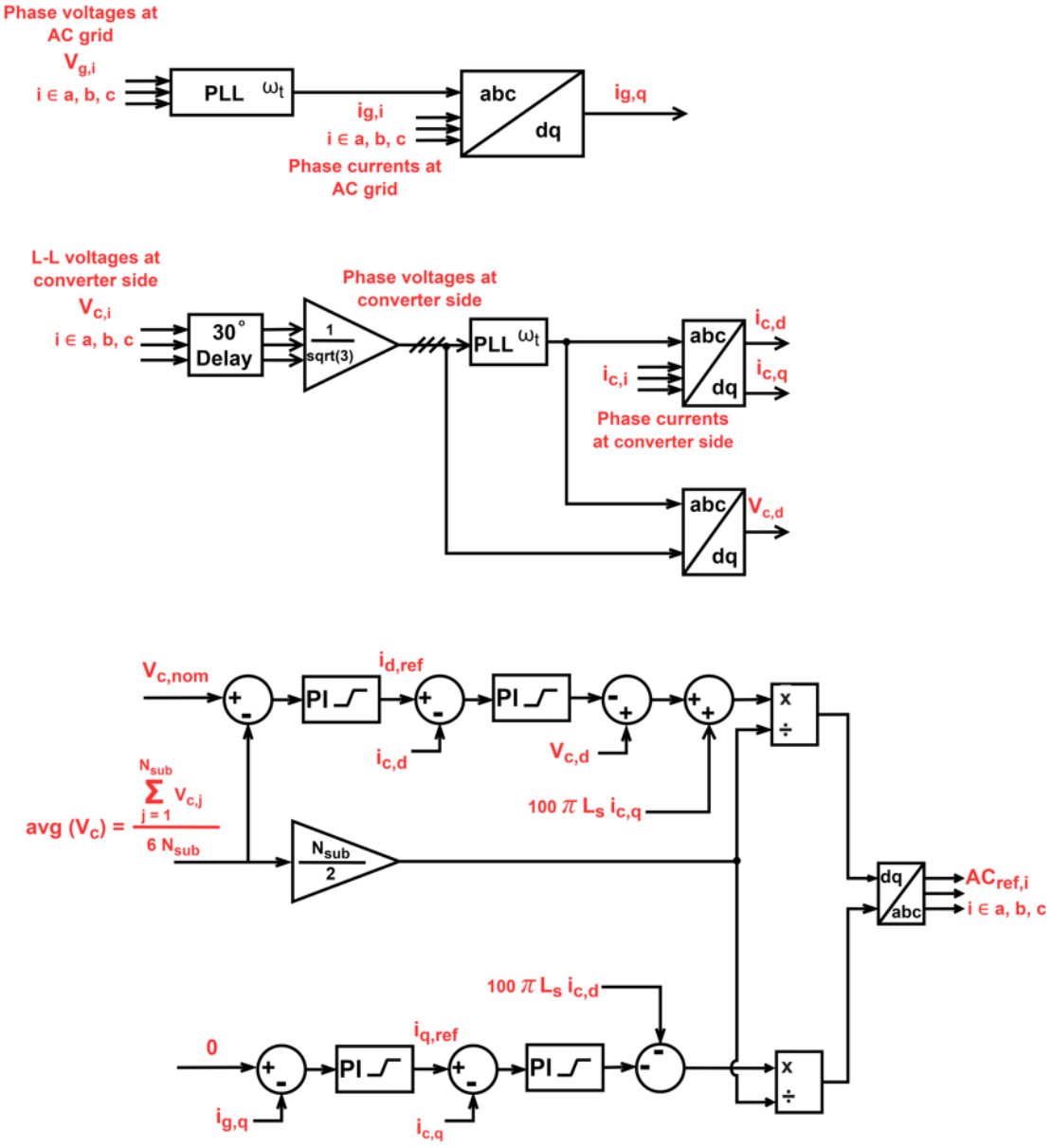


Figure 3.5 - The proposed controller for the MMC-FB

On the AC grid side, the measured phase voltages are passed to a Phase-Locked-Loop (PLL) block to determine the phase angle ω_t. This phase angle is then used to calculate the quadrature component of the AC grid currents ($i_{g,q}$). Similarly, line-to-line voltages on the transformer's secondary (converter) side are measured to evaluate direct and quadrature components of the converter currents ($i_{c,d}$ and $i_{c,q}$) and direct component of the converter-side voltage ($v_{c,d}$).

The outer control loop in the d axis is responsible for maintaining the average of the capacitor voltages to the reference value ($\frac{V_{DC,nom,c}}{N_{sub}} = \frac{25\ kV}{8}$ = 3.13 kV). In fact, this control loop provides the reference for $i_{c,d}$ to control the active power transfer to/from the converter capacitors. The outer control loop in the q axis regulates the reactive power consumption on the primary side of the transformer (grid side) to a setpoint, by producing a reference for $i_{c,q}$. Based on the AC network requirements, the setpoint for the reactive power can be changed during the TPS operation. In this study, the setpoint is zero in all the simulation cases.

The aim of inner control loops is to keep the measured $i_{d,c}$ and $i_{q,c}$ to their reference values. After applying cross-coupling terms between d and q axes, the control signals are divided by $\frac{N_{sub}}{2} \times avg\ (V_c)$, where $avg\ (V_c)$ refers to the average of the capacitor voltages. This operation is necessary to form the amplitude of the control signals and make them appropriate for the modulation stage. In other words, after transforming the control signals from the dq to abc frame, the resultant control signals for the phases 'a', 'b' and 'c' are sinusoidal-like waveforms ($AC_{ref,i}\ , i \in a, b, c$). For modulation indices less than 1, the $AC_{ref,i}$ signals should lie between −1 and 1.

3.3.3 Modulation and sorting scheme

In [23], a level-shifted carrier modulation scheme has been described for the MMCs with half-bridge submodules. In this PhD thesis, the mentioned scheme is extended for the MMC with full-bridge submodules. In this way, the proposed modulation unit can be used for the MMC-FBs in the MVDC TPSs. This aim is achieved by designing proper logic for driving four IGBTs (instead of two) and inserting submodules with

both positive and negative output voltages. In addition, the output of the modulation scheme is reformulated, so that the DC-side voltage is controlled by a DC reference.

Figure 3.6 illustrates the block diagram of the designed modulation and sorting scheme. In the DC index generator block and as shown in Figure 3.7, a reference for the DC voltage is compared with N_{sub} level-shifted carriers and a DC index (DC_{index}) is produced. Using negative carriers, and thus, negative DC indices, this arrangement can also be used for producing negative DC voltages. Nevertheless, the voltage polarity does not change in the MVDC railway electrification system and only positive carriers are implemented in this study.

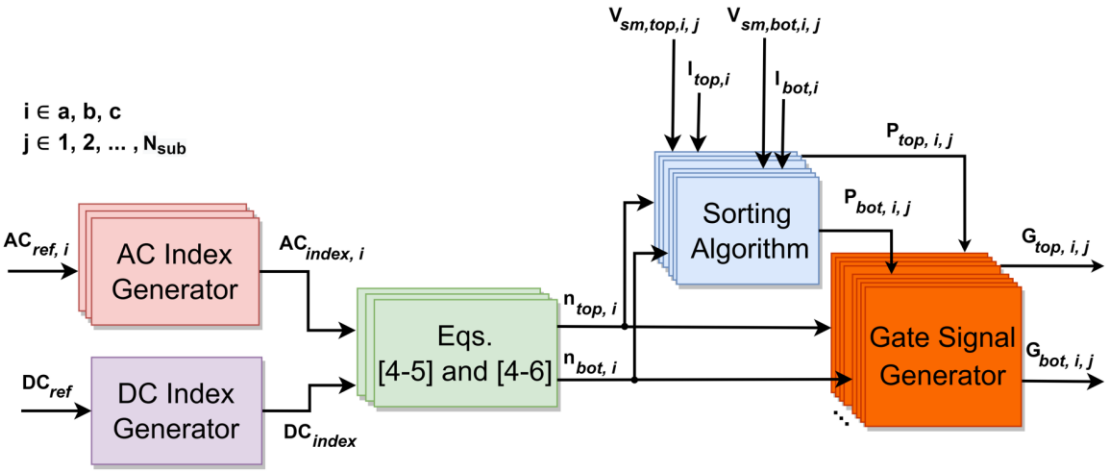


Figure 3.6 - Block diagram of the modulation and sorting scheme used for the MMC-FB

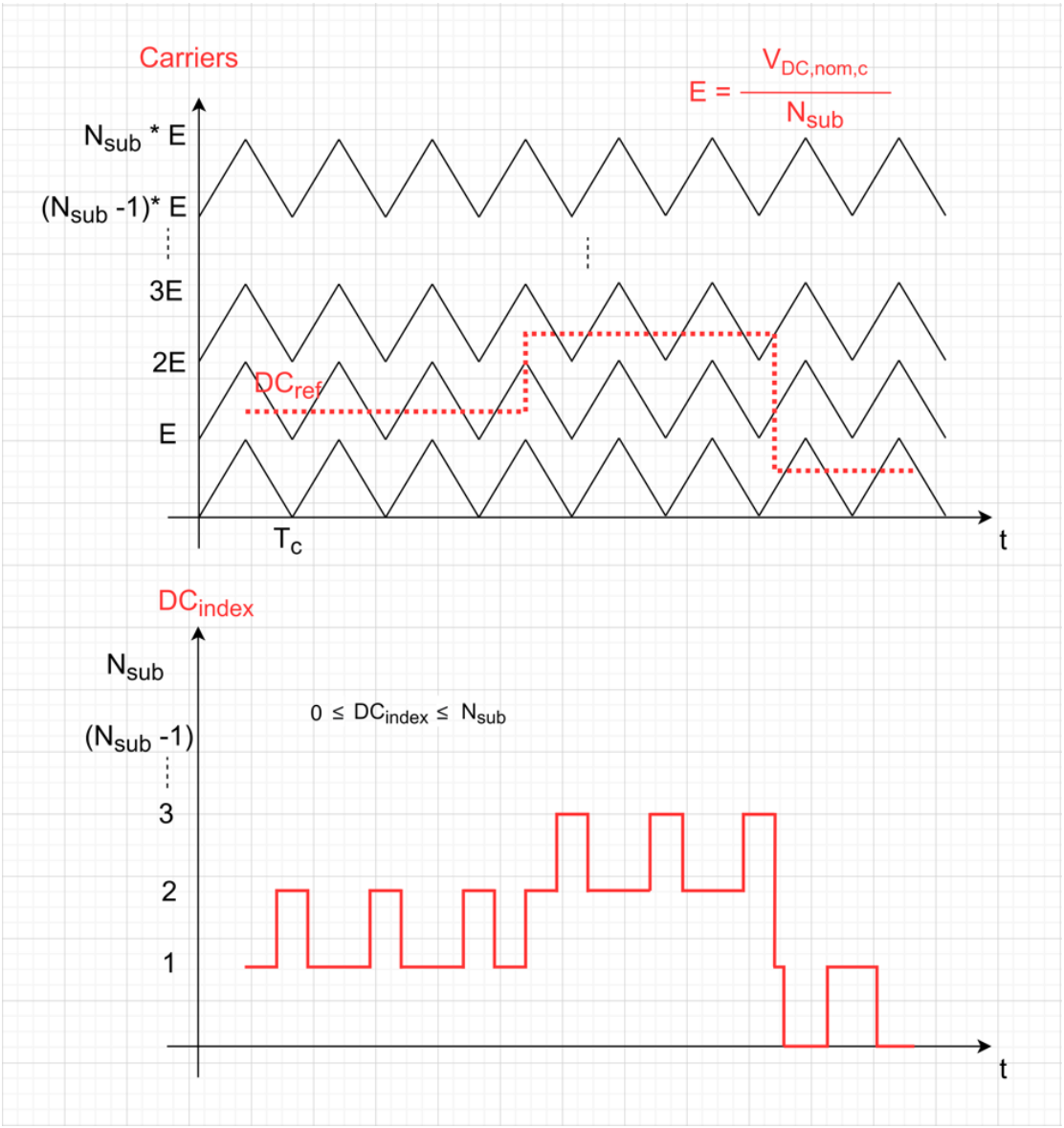


Figure 3.7 - The DC index generator block

In all the simulation cases, the carrier frequency (f_c) is 3 kHz. Except for the simulation cases related to the DC short-circuit current controller, the reference for the DC voltage is $V_{DC,nom,c}$ = 25 kV DC, which corresponds to a DC_{index} of 8.

Similarly, the output of the controller for each phase ($AC_{ref,i}$, $i \in a, b, c$) is compared with N_{sub} level-shifted carriers in the AC index generator blocks. Figure 3.8 shows the logic implemented in these blocks.

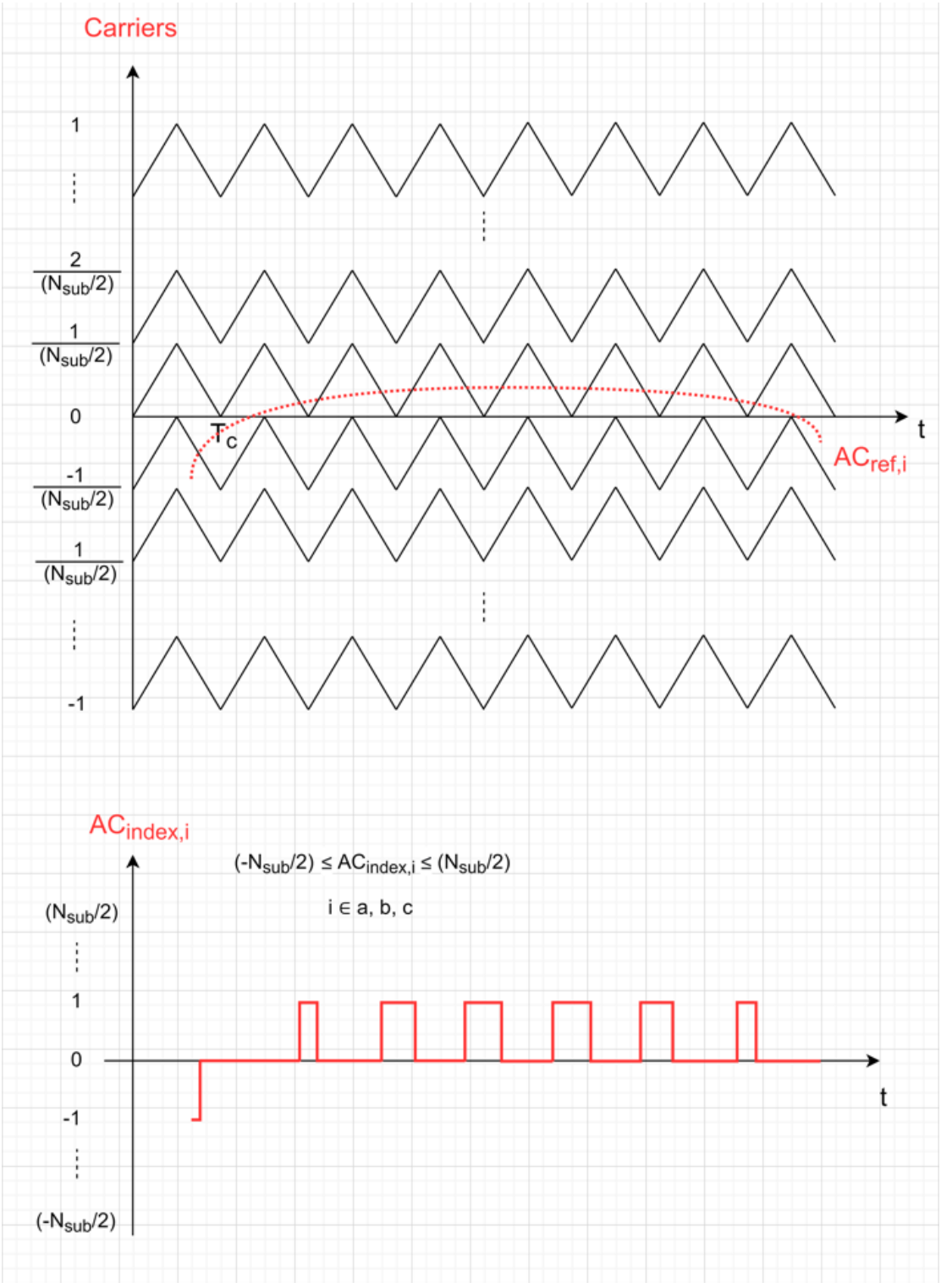


Figure 3.8 - The AC index generator block

The resultant AC index for each phase ($AC_{index,i}$, $i \in a, b, c$) is then utilised to evaluate the number of submodules which should be inserted in each arm circuit ($n_{top,i}$ and $n_{bot,i}$, $i \in a, b, c$):

$$n_{bot,i} = floor\left(0.5\left(DC_{index} + 2AC_{index,i} + 1\right)\right) \qquad -N_{sub} \le n_{bot,i} \le N_{sub} \qquad (3\text{-}5)$$

$$n_{top,i} = DC_{index} - n_{bot,i} \qquad -N_{sub} \le n_{top,i} \le N_{sub} \qquad (3\text{-}6)$$

The negative values for $n_{top,i}$ and $n_{bot,i}$ indicate that the submodules need to be inserted with a negative voltage. The derivation of the above formula is presented in Appendix C.

In the sorting blocks and considering the arm current direction and the sign of n_t and n_{bot}, the capacitor voltages are sorted. In addition, a priority index is assigned to each capacitor within an arm ($P_{top,i,j}$ for the top arms and $P_{bot,i,j}$ for the bottom arms, $i \in a, b, c$ and $j \in 1, 2, \dots, N_{sub}$). In the simulation models, the sorting is done every 1 ms. Figure 3.9 shows the sorting algorithm for the top arm of phase 'a'. All the sorting blocks implement the same logic.

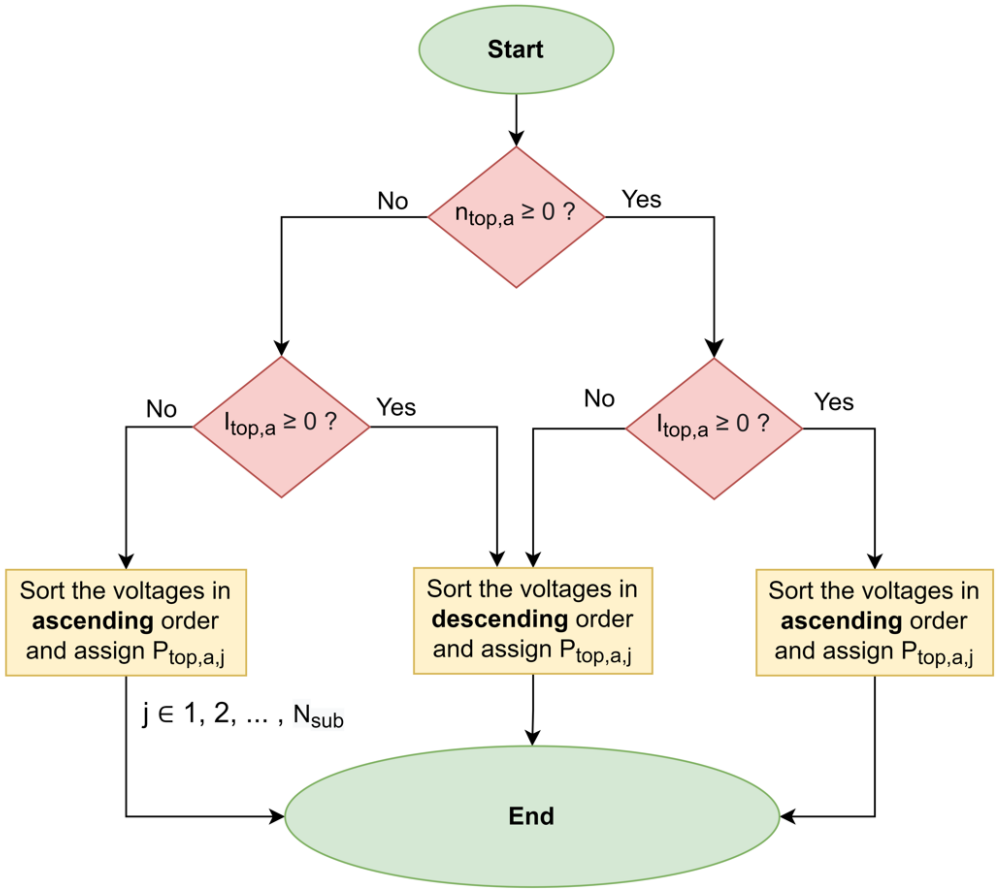


Figure 3.9 - Logic implemented in the sorting blocks

The priority indices lead to insertion of the capacitors with the highest priority within an arm. For example, if $n_{top,a} = 1$, and the arm current in the top arm of phase 'a' ($I_{top,a}$) is positive, the capacitor with the least voltage is inserted into the circuit. This is because when the module is inserted with a positive output voltage, the positive arm current charges the inserted capacitor. Table 3.5 presents various possible states for a full-bridge submodule and the effect of the arm current on charging/discharging its capacitor.

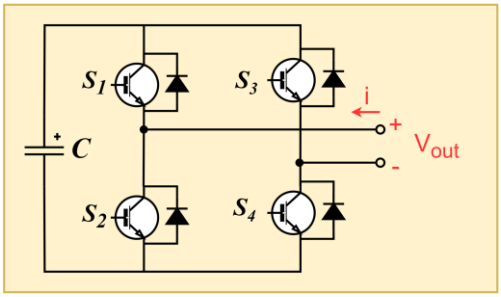


Table 3.5 - Possible states for full-bridge submodule

State	S1 (= $\overline{S_2}$)	S4 (= $\overline{S_3}$)	V_{out}	i ≥ 0	i < 0
1	1	1	+ V_c	V_c ↑	V_c ↓
2	1	0	0	Fixed	Fixed
3	0	1	0	Fixed	Fixed
4	0	0	− V_c	V_c ↓	V_c ↑

The gate signal generator blocks interpret the priority indices and, based on the values for $n_{top,i}$ and $n_{bot,i}$, provide proper gate signals for the switches in each submodule. Figure 3.10 depicts the logic implemented, which is designed based on the states presented in Table 3.5. In this figure, $G_{top,a,j,3}$ denotes the gate signal for switch number 3 (S_3) in module number *j* in the top arm of phase 'a'. For the rest of the arms and phases, the logic is the same.

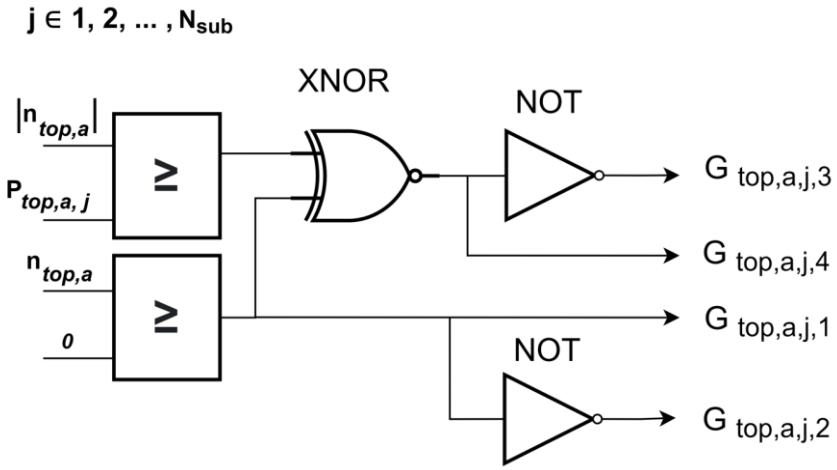


Figure 3.10 - The logic of gate signal generator blocks

3.3.4 DC short-circuit current controller

The MVDC TPSs are protected by AC circuit breakers on the AC side. Concerning the DC side, installing DC Circuit Breakers (DCCBs) is necessary. This is because short-circuit currents on the DC side can increase rapidly and damage the TPS converter before the AC circuit breakers trip. On the other hand, DCCBs with 25 kV DC and high current ratings are costly [3], complicated and hard to realise. In fact, this is one of the obstacles towards realising MVDC railways in the industry.

As a solution, the MMC-FBs can limit the short-circuit currents to a maximum value ($I_{DC,max,fault}$), e.g., 1.2 pu. Although the DCCBs are still required to isolate capacitors and inductors of the converters from the faulty MVDC network, their current ratings can be much smaller. In other words, the MVDC network can be protected by cheaper protection equipment.

The MMC-FBs limit the short-circuit currents by decreasing the DC-side voltage while the amplitude of the AC-side voltages remains constant. As shown in Figure 3.11, a PI controller regulates the reference for the DC voltage by sensing the DC-side current. The controller gains are presented in Appendix D.

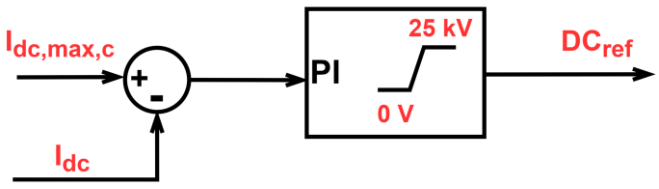


Figure 3.11 - DC short-circuit current controller

In the normal situation, the output of the PI controller is saturated to 25 kV DC. In the case of a short-circuit, i.e., DC currents higher than $I_{DC,max,c}$, the PI controller decreases the DC voltage reference, and thus, the DC_{index}. Based on equations (3-5)

and (3-6), this leads to a decrease in the number of inserted submodules. For smaller values of DC_{index}, the number of inserted submodules becomes negative in some time intervals. Therefore, the average of arm voltages, and thus, the DC voltage decreases.

If the short-circuit is non-permanent and the fault is cleared before the DCCBs act, the PI controller increases the DC voltage reference to restore the voltage to 25 kV DC. In the designed protection strategy, all the MMC-FBs in the MVDC network are equipped with a short-circuit controller. Therefore, an MVDC network with multiple TPSs can be protected against the DC short-circuits.

The short-circuit situation is modelled by connecting the fault resistor (R_{sc}) in parallel to the load, as illustrated in Figure 3.12.

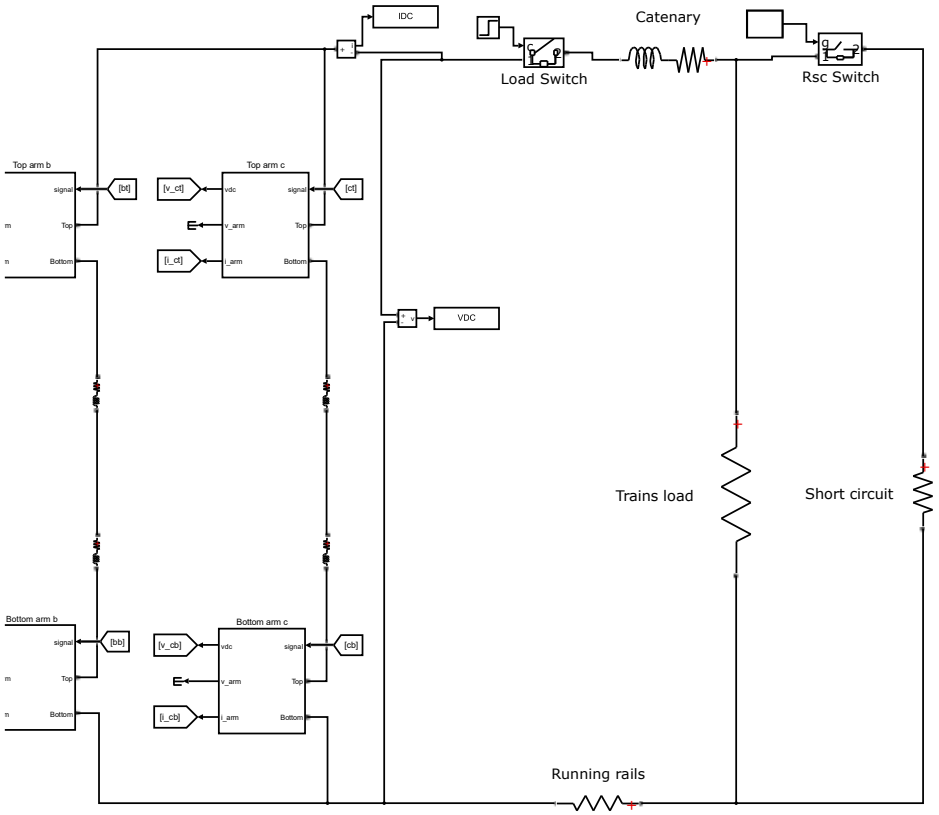


Figure 3.12 - DC fault modelling in the Matlab/Simulink simulations

3.4 MMC loss modelling

The power losses and efficiency of an MMC-FB are evaluated in Matlab/Simulink based on switching and conduction losses (P_{sw} and P_{cond}) of the IGBTs and diodes. It is assumed that the MMC-FB is realised by IGBT−diode modules 'ABB 5SNA 1000G650300 HiPak IGBT' (6.5 kV, 1 kA) [24].

In each arm, and for each IGBT and diode, the current samples at time instants 't' and 't – 1' are used to identify turn-on and turn-off moments. The curves for E_{on} and E_{off} versus collector current I_C in the module datasheet show typical switching energies per pulse for the IGBTs. Using curve-fitting techniques, the curves at a junction temperature of 125 °C are transformed to quadratic equations. Hence, knowing the collector current at the switching moments, the IGBT energy losses during the switching periods can be determined. The same procedure is carried out for the diodes, using typical reverse recovery energy E_{rec} versus forward current I_F curve from the module datasheet. For the diodes, the energy losses during the turning-on process are neglected.

The curves in the datasheet are valid when the test voltage applied to the modules is V_{cc} = 3.6 kV. Therefore, to consider the actual DC voltage applied to the modules [25] in the MMC-FB, the curves are multiplied by $\frac{(V_{C,nom})}{(V_{cc})} = \frac{3.13\ kV}{3.6\ kV} = 0.87$.

In the next step, power losses for each switching instant are calculated, assuming that each instant lasts for one step of the simulation (T_s = 10 μs), i.e.:

$$P_{sw}(t) = \frac{E_{sw}(t)}{T_s} \tag{3-7}$$

To evaluate the conduction power losses, typical on-state characteristics curve (collector current I_C versus collector emitter voltage V_{CE}) for the IGBTs and typical

diode forward characteristics (forward current I_F versus forward voltage V_F) for the diodes are transformed to fifth-degree polynomial functions by curve fitting ($V_{CE} = f(I_C)$ and $V_F = f(I_F)$). Hence, V_{CE} and V_F are evaluated based on instantaneous I_c and I_F, respectively. The conduction power losses are then determined by multiplying instantaneous I_C to V_{CE} for the IGBTs, and I_F to V_F for the diodes.

The MMC-FB efficiency is estimated based on the average power and according to equation (3-8):

$$\eta = \frac{\bar{P}_{out}}{\bar{P}_{out} + \bar{P}_{loss,MMC}} \times 100 = \frac{\bar{P}_{Load} + \bar{P}_{OHL} + \bar{P}_{rails}}{\bar{P}_{Load} + \bar{P}_{OHL} + \bar{P}_{rails} + \bar{P}_{loss,MMC}} \times 100 \qquad (3\text{-}8)$$

where $\bar{P}_{loss,MMC}$ is the average power losses of the MMC-FB over a time interval. In the simulations and to evaluate a typical value for the average power losses and the MMC-FB efficiency, the load is applied from t_1 = 0.3. The average power losses between t_1 = 0.3 and t_2 = 0.8 are then computed as follows:

$$\bar{P}_{loss,MMC} = \frac{\int_{t_1}^{t_2} \big(P_{sw}(t) + P_{cond}(t)\big) dt}{t_2 - t_1} \qquad (3\text{-}9)$$

In (3-8), $\bar{P}_{Load}$, $\bar{P}_{OHL}$ and $\bar{P}_{rail}$ are the average power consumed by the train's load, overhead lines and the running rails, respectively. Similar to $\bar{P}_{OHL}$ and $\bar{P}_{rail}$, $\bar{P}_{Load}$ is determined as follows:

$$\bar{P}_{Load} = \frac{\int_{t_1}^{t_2} (V_{Load}(t) \times I_{Load}(t)) dt}{t_2 - t_1} \qquad (3\text{-}10)$$

where $V_{Load}(t)$ and $I_{Load}(t)$ are the instantaneous voltage and current of the load.

3.5 Summary

The aim of this chapter was to discuss the methodology used to model and simulate the proposed MVDC railways. First, specifications of the proposed MVDC railway

electrification system were defined. Assuming typical values, a model for an individual MVDC TPS as the building blocks of the MVDC railway model was then introduced. Moreover, an MMC-FB was designed for the MVDC TPS, considering the required voltage and current ratings of the IGBT–diode modules. Concerning the MMC-FB controller, a control scheme in direct-quadrature (dq) frame was proposed. The controller's aim is to regulate the average voltage of the submodules and reactive power consumed by the converter. The controller outputs are then passed to the modulation stage, which is designed based on level-shifted carrier modulation and is able to control the DC-side voltage. This chapter also presented a DC short-circuit current controller, which limits DC fault currents by decreasing the DC-side voltage. Finally, the methodology used for estimating MMC-FB losses and efficiency was described. The MMC-FB was simulated in Matlab/Simulink using the Simscape library and the simulation results are presented in the next chapter.

4 SIMULATION ANALYSIS OF MVDC RAILWAYS

This chapter presents the performance analysis of the MVDC railways using the simulation models. The models are developed based on the methodology presented in the previous chapter, and the parameters assumed in each simulation case are explained.

4.1 Case 1: An individual MVDC TPS in normal operation

In simulation case 1, the simulation model of an individual MVDC TPS is run to assess the TPS performance. The developed Matlab/Simulink model was presented in the previous chapter. The simulation time is from t_1 = 0 s to t_{stop} = 0.8 s, and the initial voltage for the converter capacitors is $V_{C,nom}$ = 3.13 kV. The DCCB is closed at t_{DCCB} = 0.2 s to ensure that the DC-side voltage is stable before applying the load.

A typical power consumption profile of the high-speed trains consists of accelerating, coasting and braking, each taking several seconds/minutes. The goal of the simulations in this section is to investigate the TPS performance in extreme loading conditions. In addition, the MMC-FB should ideally respond to the load changes in several tens of milliseconds or less. Therefore, instead of a typical power consumption profile, an extreme load profile (shown in Figure 4.1) is implemented by a controlled current source to mimic the trains' power consumption.

At t_{DCCB} = 0.2 s, the load starts to rise from 0 A and at t_1 = 0.3 s, it reaches the full load of 640 A (equivalent to 16 MW at 25 kV DC). It is assumed that the trains are located close to the TPS and start to accelerate at the TPS location. Therefore, the parameter for distance between the load and the TPS is selected as 10 m.

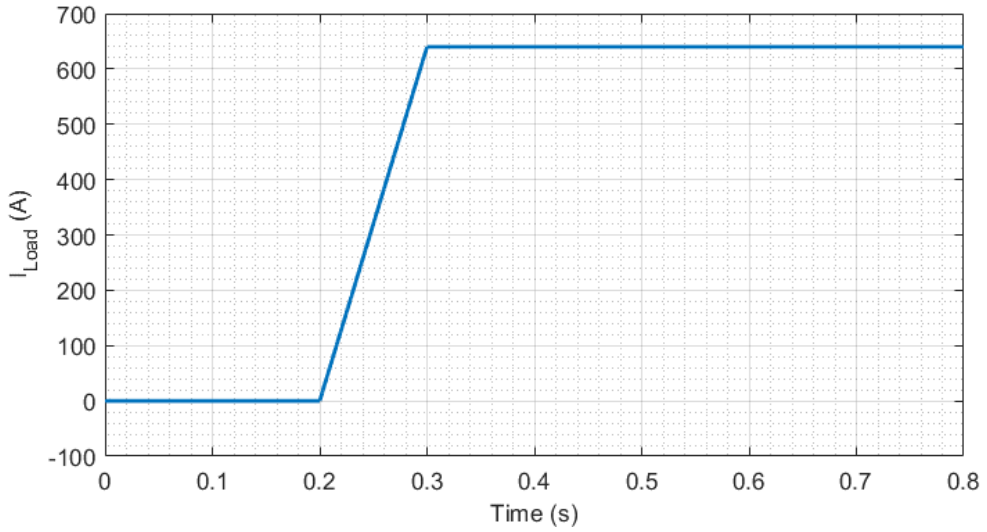


Figure 4.1 - DC load current profile - case 1

Figure 4.2 depicts the voltage on the DC terminals of the MMC-FB. In all the simulations, it is assumed that the capacitors are pre-charged to 3.13 kV and then the simulations start. Therefore, immediately after starting the simulations, a transient DC voltage with a peak of 50 kV is observed. The objective of the simulations is to assess the MVDC TPS behaviour after this transient and in particular, after connection of the load. Hence, this transient can be neglected in analysis. In the real-world implementation of the MMC-FB and as will be discussed in section 5.3, the converter capacitors are charged gradually to avoid overshoot/undershoot in DC voltage.

Following the initial transient, the DC voltage is regulated at 25 kV. After applying the load at t_{DCCB} = 0.2 s and during acceleration of the trains, the DC voltage drops to 24.35 kV. From t_1 = 0.3 s, the controller restores the voltage to the nominal value of 25 kV.

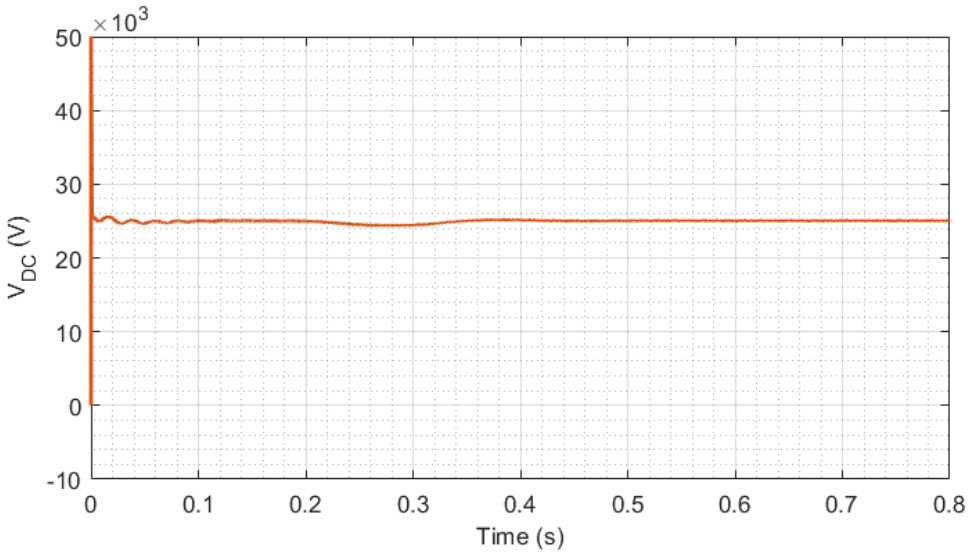


Figure 4.2 - DC-side voltage - case 1

The magnified DC voltage between t_2 = 0.5 s and t_{stop} = 0.8 s is presented in Figure 4.3. The maximum and minimum voltages in this time frame are 25.12 kV and 24.96 kV, respectively. In other words, the peak-to-peak voltage ripple is 0.64%, showing that the implemented control and modulation algorithm are able to regulate the DC-side voltage with low voltage ripples.

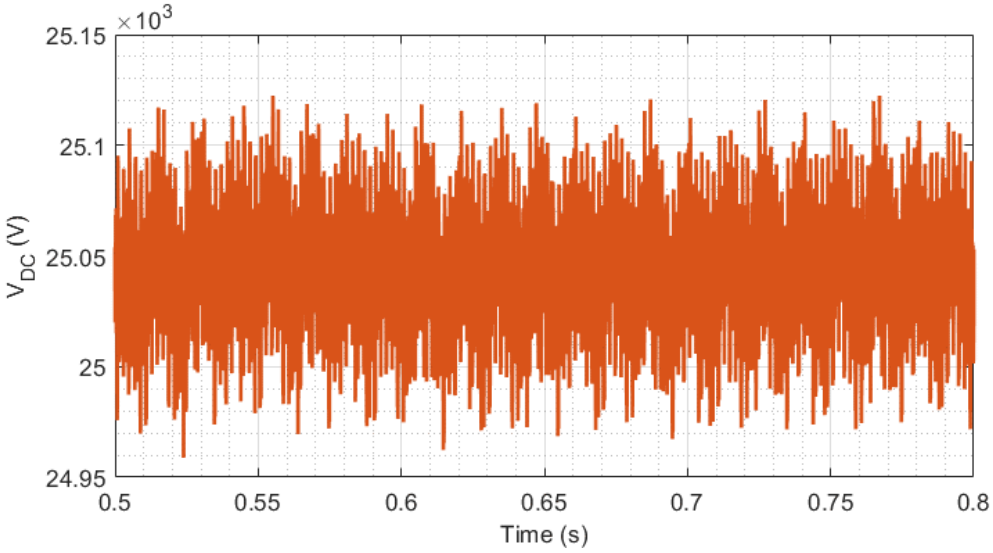


Figure 4.3 - DC-side voltage between t = 0.5 s and t = 0.8 s - case 1

The capacitor voltages in the six arms of the MMC-FB are presented in Figure 4.4. Similar to the DC voltage and after the transient related to the trains' acceleration, the capacitor voltages are kept around $V_{C,nom}$ = 3.13 kV. The voltages are magnified in Figure 4.5, showing that the peak-to-peak ripple of the capacitor voltages is less than 7.5%. Moreover, the sorting algorithm operates properly as the capacitor voltages are balanced within an arm.

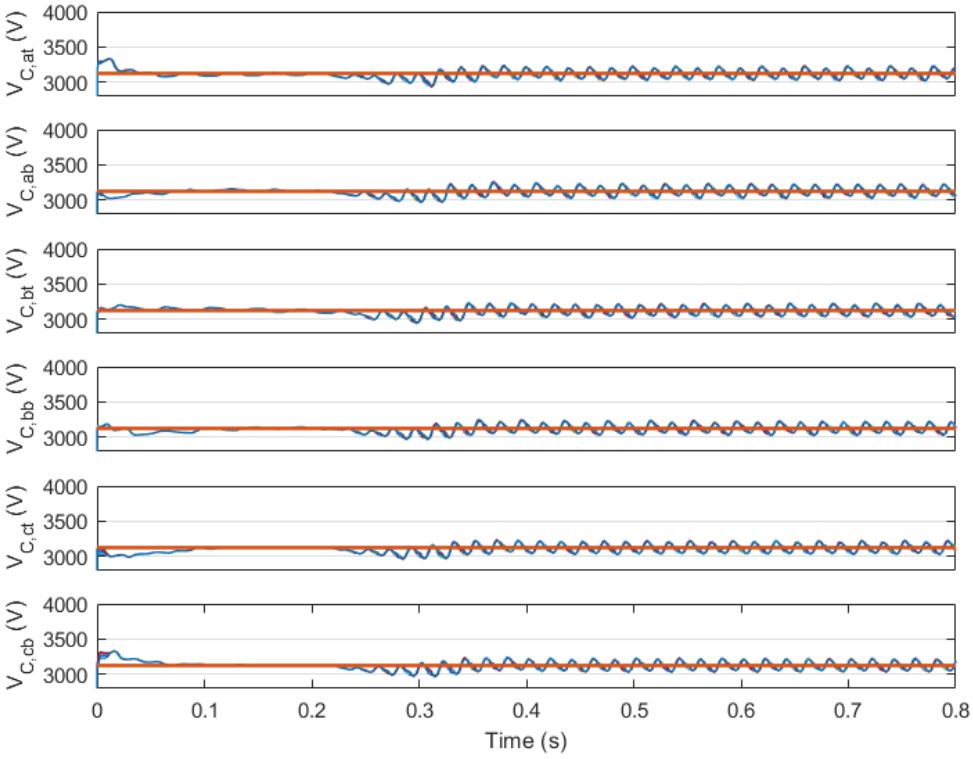


Figure 4.4 - MMC-FB capacitor voltages - case 1

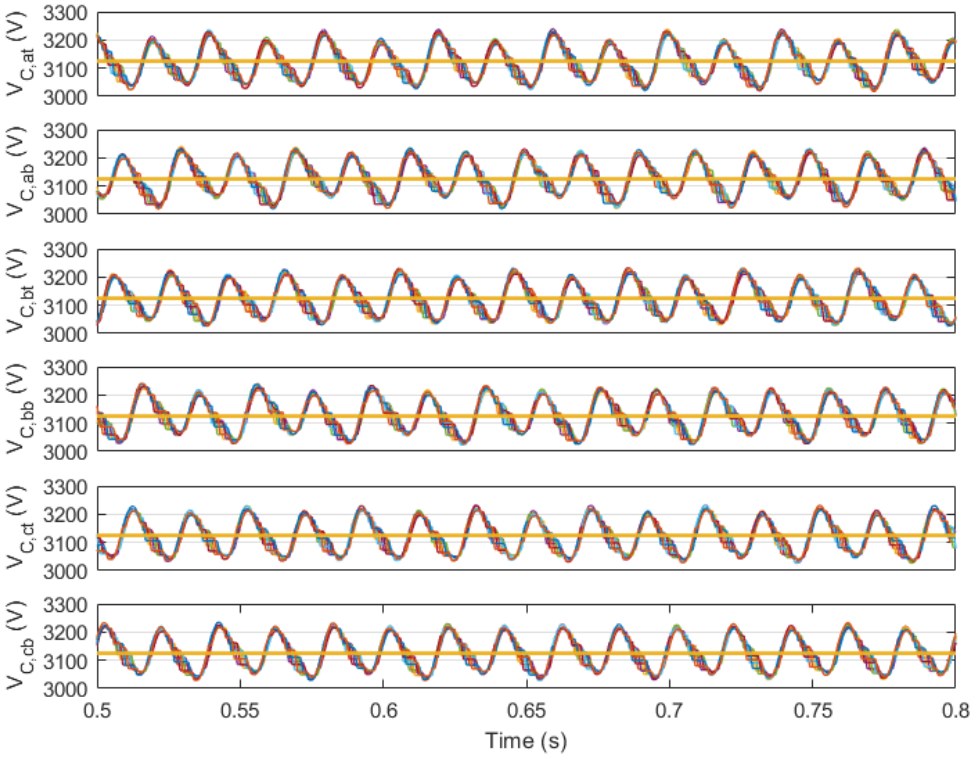


Figure 4.5 - Magnified capacitor voltages - case 1

Figure 4.6 demonstrates the MMC-FB arm voltages in phase 'a', which consist of N_{sub} = 8 levels. The arm voltages are 180° out of phase to properly form the DC- and AC-side voltages. Figure 4.7 shows the voltage drops on the arm inductors in phase 'a'. The arm inductor voltages are periodic waveforms with a frequency of 50 Hz and amplitude of 2.7 kV. Moreover, the MMC-FB arm currents, demonstrated in Figure 4.8, have a negative DC offset of around 210 A in steady state which is approximately equivalent to $\frac{I_{DC}}{3}$.

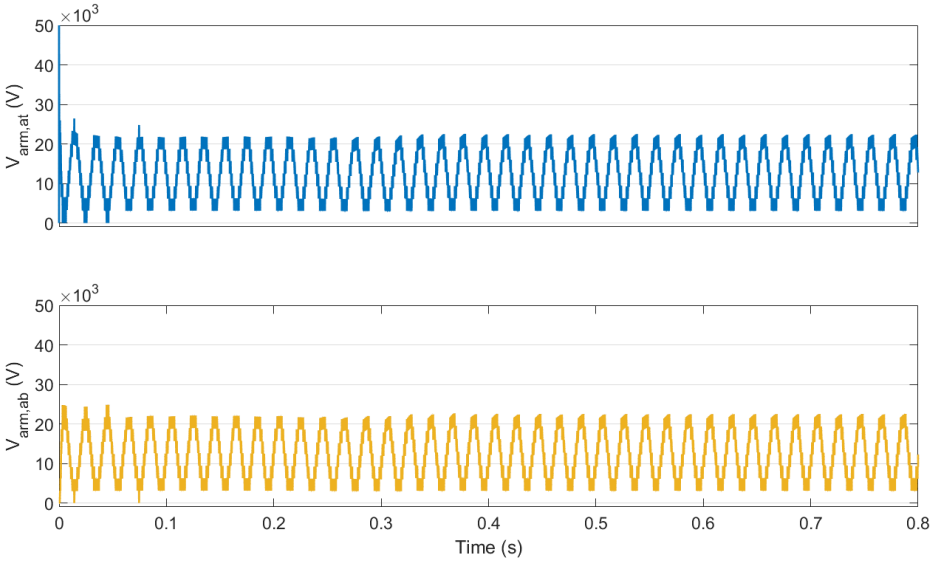


Figure 4.6 - Arm voltages in phase 'a' of MMC-FB - case 1

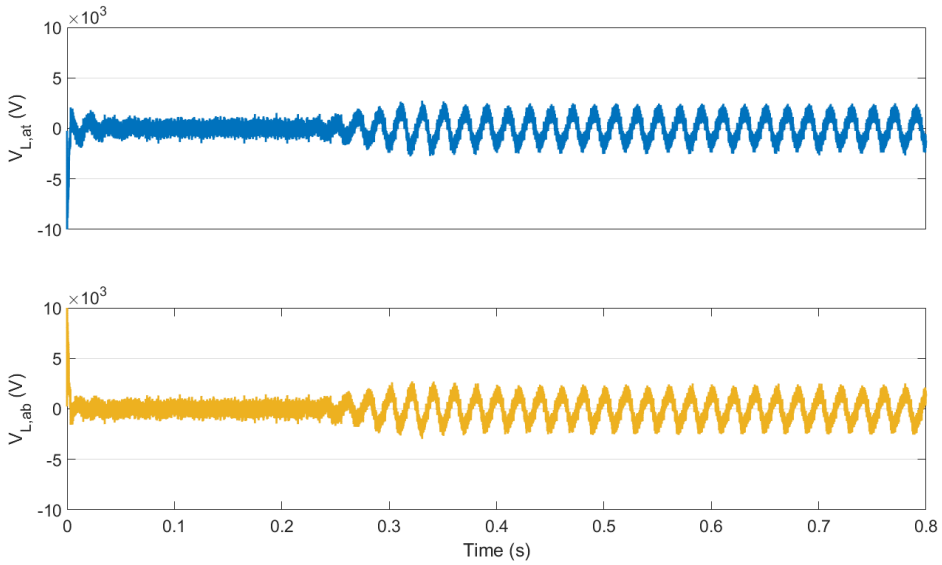


Figure 4.7 - Voltage drops on the arm inductors of phase 'a' - case 1

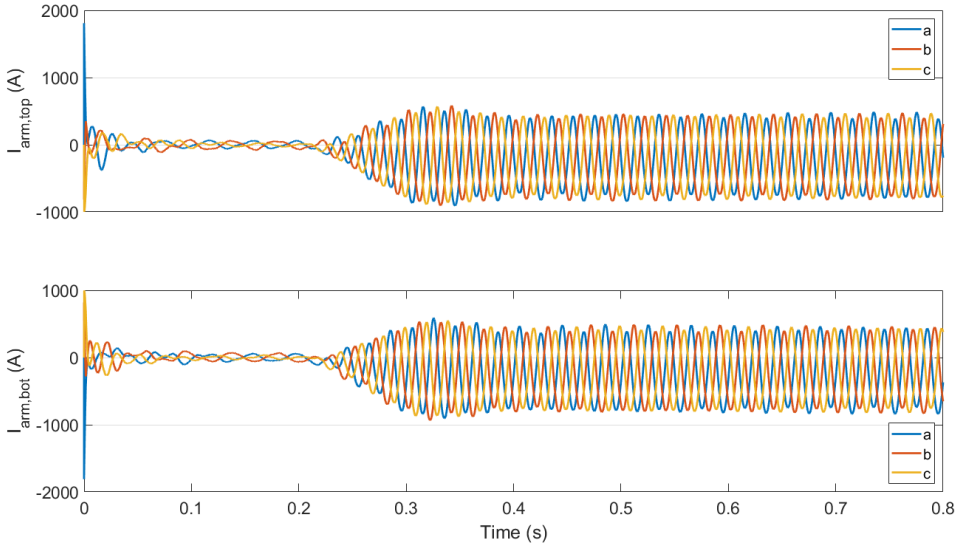


Figure 4.8 - Arm currents in the MMC-FB - case 1

Concerning the AC side, the converter draws balanced and nearly sinusoidal currents from the distribution network, as depicted in Figure 4.9. In addition, the current and voltage of phase ‘a’ in the distribution network are illustrated in Figure 4.10. The phase difference between the phase voltage and current is nearly zero, indicating that the converter transfers active power from the AC side to the DC side while consuming negligible reactive power.

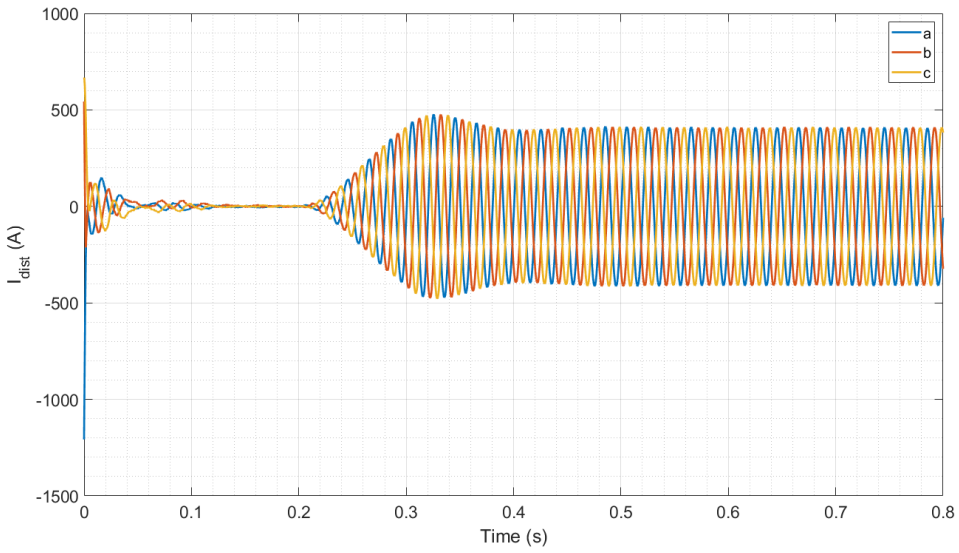


Figure 4.9 - AC currents in 33 kV distribution network - case 1

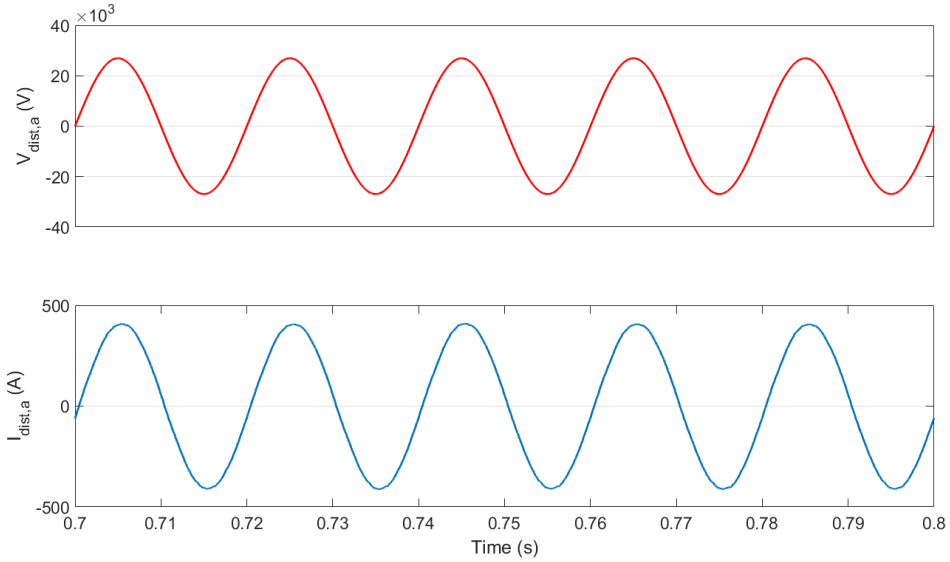


Figure 4.10 - Voltage and current of phase 'a' in 33 kV distribution network - case 1

Assuming that the voltages in the 33 kV distribution network are purely sinusoidal, the power factor is calculated using equation (4-1):

$$PF = \frac{P}{|S|} = \frac{I_{RMS,1}}{I_{RMS}} \times \cos\varphi_1 \qquad (4\text{-}1)$$

where $|S|$ is total apparent power, P is the average of the transferred active power, I_{RMS} is the RMS of the phase current, $I_{RMS,1}$ is the RMS value for the fundamental component of the phase current and φ_1 is the phase difference between the phase voltage and the fundamental component of the phase current.

The power factor is evaluated based on the current and voltage of phase 'a', and in both full-load (the load profile stated in Figure 4.1) and low-load conditions. In the low-load condition, the overall shape of the load profile is similar to that in Figure 4.1, and the only difference is that the maximum value is 10% of the full-load current, i.e., 64 A. As illustrated in Figure 4.11 and Figure 4.12, the steady state power factor is close to unity in both loading conditions.

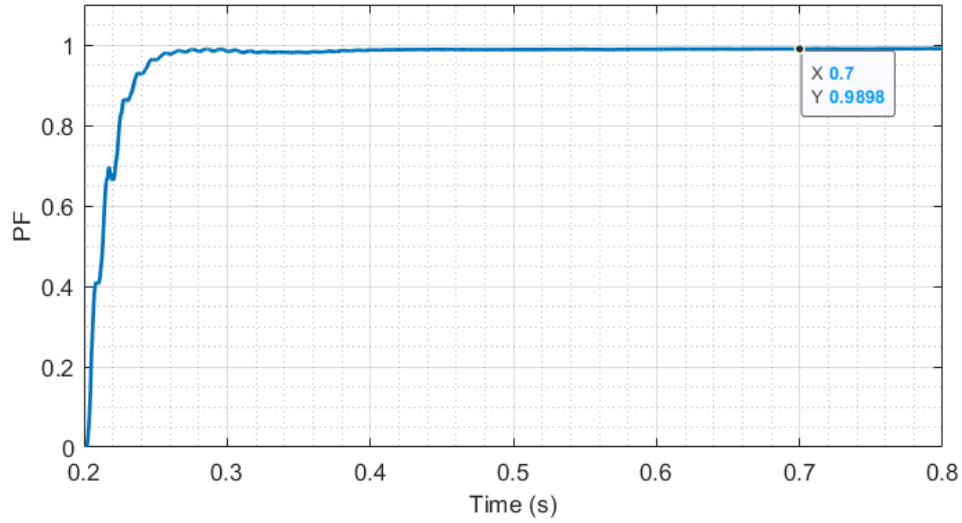


Figure 4.11 - Power factor in 33 kV distribution network (full load) - case 1

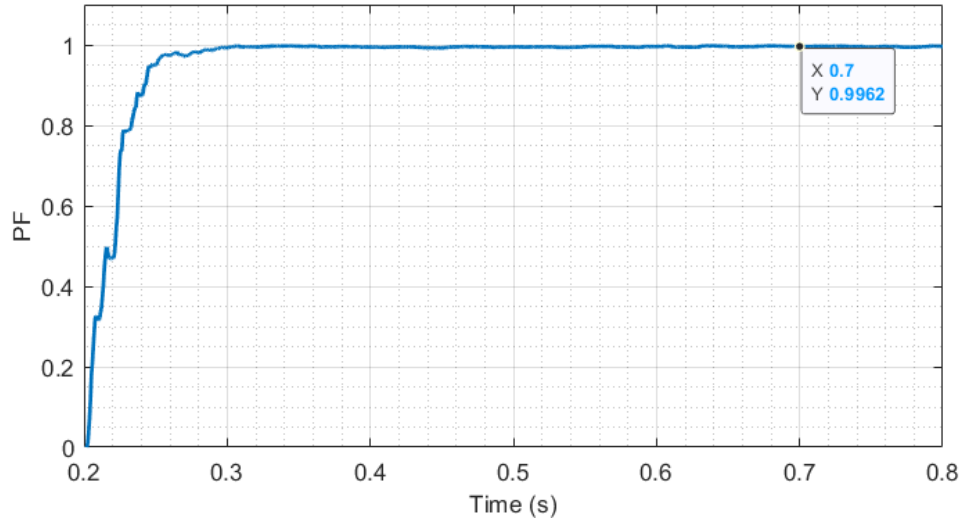


Figure 4.12 - Power factor in 33 kV distribution network (low load) - case 1

To investigate the current quality in the 33 kV network, Total Demand Distortion (TDD) for the phase currents is calculated. Based on the IEEE 519-2014 standard, TDD is “the ratio of the root mean square of the harmonic content, considering harmonic components up to the 50th order and specifically excluding interharmonics, expressed as a percent of the maximum demand current. Harmonic components of order greater than 50 may be included when necessary” [26]. This definition can be expressed as:

$$TDD\ (I)\ \% = \frac{\sqrt{\sum_{2}^{50} {I_{RMS,n}}^{2}}}{I_{L,RMS}} \times 100 \tag{4-2}$$

where $I_{RMS,n}$ is the RMS of the n[th] harmonic component and $I_{L,RMS}$ is the RMS of the maximum demand current.

In this study, $I_{L,RMS}$ is assumed to be the current of the 33 kV network when the MVDC TPS supplies a full load of 20 MW, i.e., 0.35 kA. Considering that the maximum fault level for the 33 kV network is 1000 MVA [27], the short-circuit current level is:

$$I_{sc} = \frac{1000\ MVA}{\sqrt{3}\ \times 33\ kV} = 17.5\ kA \tag{4-3}$$

Hence:

$$\frac{I_{sc}}{I_L} = 50 \tag{4-4}$$

According to IEEE 519-2014 and for $\frac{I_{sc}}{I_L}$ = 50, the TDD of currents should be less than 8% of $I_{L,RMS}$.

Figure 4.13 presents the evaluated TDD for the current in phase ‘a’. In the no-load condition, TDD is below 1%. During the acceleration period, TDD increases to a maximum of 6.46%. After this transient and in the steady state, TDD decreases to below 1%. The analysis of currents in phases ‘b’ and ‘c’ shows similar results to those for phase ‘a’.

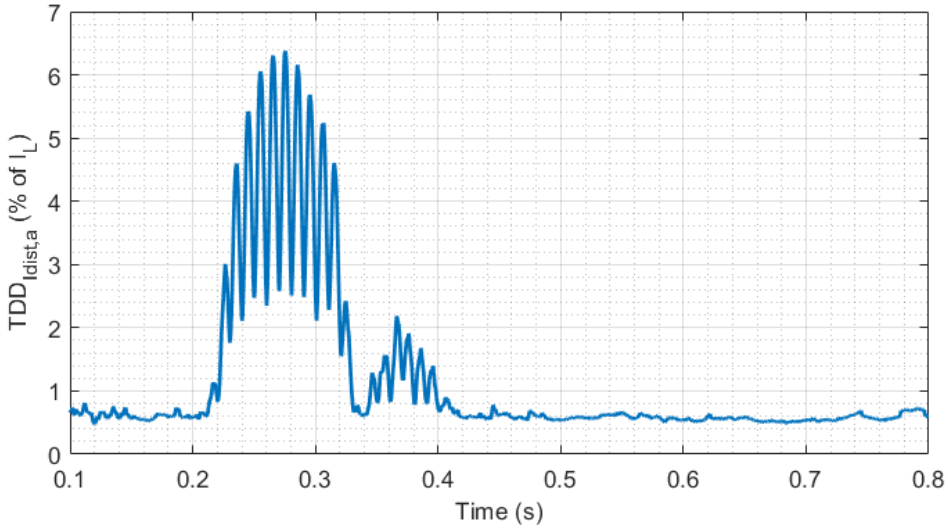


Figure 4.13 - TDD of phase current 'a' in 33 kV network - case 1

4.2 Case 2: An individual MVDC TPS during regenerative braking

The MVDC TPS is able to inject the energy produced during braking of the trains into the AC network. To evaluate the TPS performance during regenerative braking, the load profile of Figure 4.1 is replaced with a load profile with a minimum current of −320 A, as shown in Figure 4.14.

The DC-side voltage, demonstrated in Figure 4.15, increases to a maximum of 25.35 kV during the braking period, then drops to a minimum of 24.90 kV, and finally becomes regulated around the nominal value. According to the operational conditions defined for the MVDC electrification system in the previous chapter, the DC voltage remains in the acceptable range during the braking process.

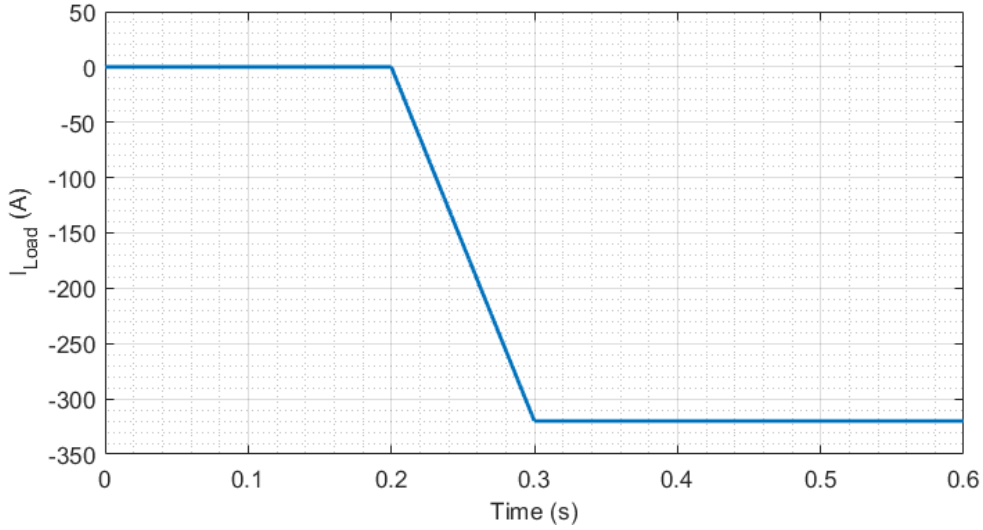


Figure 4.14 - Load profile - case 2

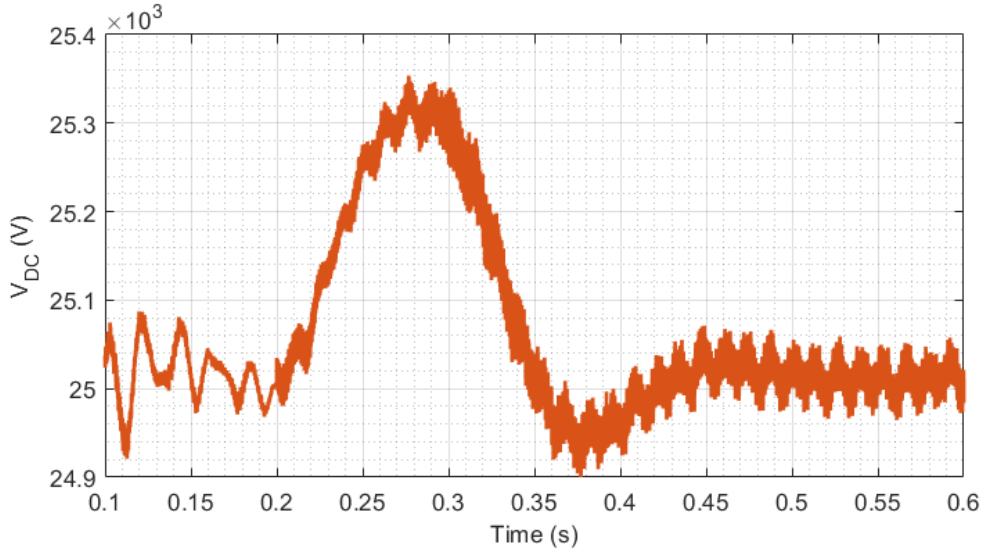


Figure 4.15 - DC-side voltage - case 2

Figure 4.16 represents the voltage and current of phase ‘a’ in the distribution network. The phase difference between current and voltage is nearly 180°, which means the MMC-FB injects active power from the DC side to the AC distribution network while the transferred reactive power is negligible. Moreover, the TDD of a phase current in the AC network is shown in Figure 4.17. Similar to simulation case 1, the TDD is below 1% in the steady state, indicating that the injected phase current is a high-quality sinusoidal current.

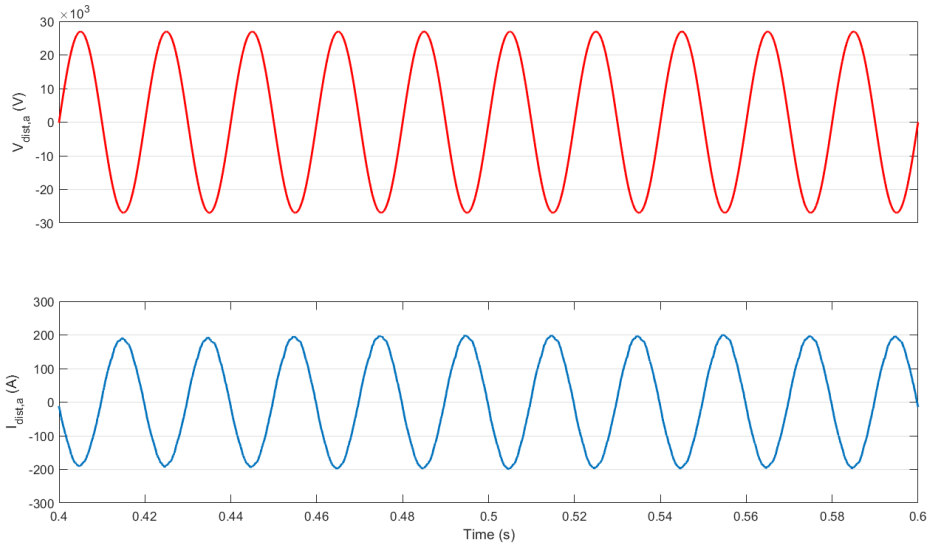


Figure 4.16 - Voltage and current of phase 'a' in 33 kV distribution network - case 2

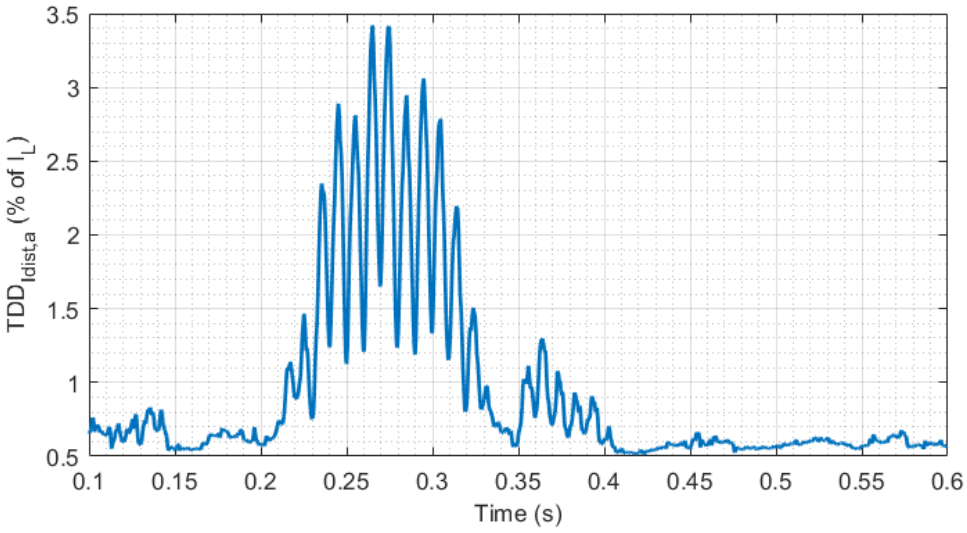


Figure 4.17 - TDD of phase current 'a' - case 2

4.3 Case 3: An individual MVDC TPS during a voltage dip on the AC side

To investigate the TPS performance in abnormal conditions, it is assumed that the AC distribution network experiences a voltage dip while the TPS supplies the same load profile as in case 1. In other words, from t_{d1} = 0.6 s to t_{d2} = 1 s, the voltage of the 33 kV network decreases to 0.9 pu, and after t_{d2}, the voltage is restored to 33 kV. The

simulation stop time is t_{stop} = 1.4 s, and the DC load remains constant at 16 MW from t_1 = 0.3 s until the end of the simulation.

The voltages and currents of the distribution network, capacitor voltages in phase 'a' of the converter, and the DC-side voltage are demonstrated in Figure 4.18 to Figure 4.20, respectively. The AC-side currents increase during the voltage dip, and six cycles after t_{d2} settle to the same level as the normal operation. During the incident, the ripples of capacitor voltages become slightly larger. However, the capacitor voltages remain balanced and controlled around the reference voltage.

On the DC side, the incident causes a DC voltage drop at t_{d1}, where the minimum voltage is 24.84 kV. Moreover, there is a voltage rise at t_{d2}, where the maximum voltage is 25.26 kV. Nevertheless, the DC voltage remains regulated around the nominal value, and the TPS can supply the load normally during the AC voltage dip.

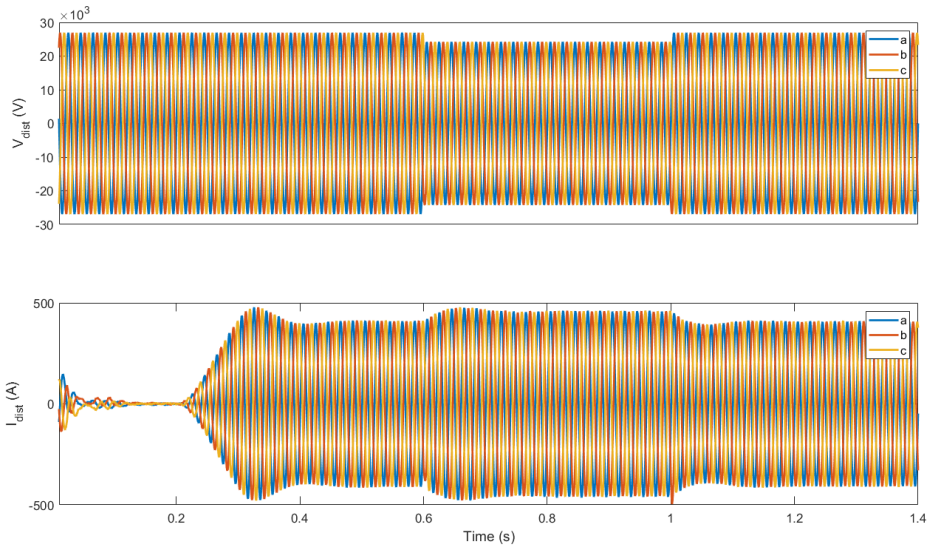


Figure 4.18 - Voltages and currents of 33 kV network - case 3

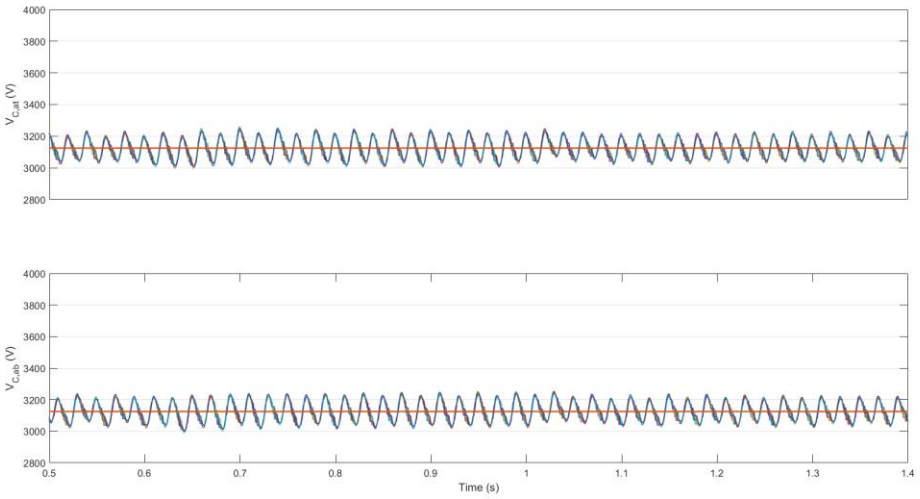


Figure 4.19 - Capacitor voltages in phase 'a' of the MMC-FB - case 3

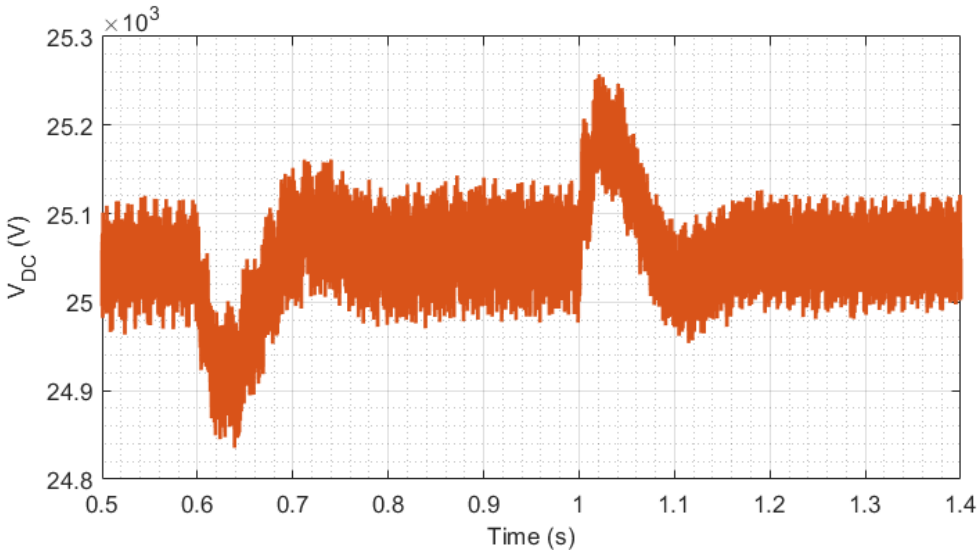


Figure 4.20 - DC-side voltage - case 3

4.4 Case 4: An individual MVDC TPS during DC short-circuit

The modelling process of the DC short-circuit was presented in the previous chapter. In this section, the simulation results are described. Table 4.1 represents the parameters used in simulation case 4. The TPS load before the DC fault is modelled with a fixed load resistor (R_L = 31.25 **Ω**), which is equivalent to power consumption of 20 MW at

25 kV. The DC fault is a non-permanent fault, which happens from t_{f1} = 0.25 s to t_{f2} = 0.45 s by connecting the fault resistor R_{sc} in parallel with the load resistor. The AC-side protection and DCCB are disabled, so the MMC-FB operation can be observed during the non-permanent DC fault.

Table 4.1 - Parameters of simulation case 4

Parameter	Symbol	Value
Fault resistance	R_{sc}	0.5 Ω
Load resistor	R_L	31.25 Ω
Distance of the load and DC fault from the TPS	d_{c4}	100 m
Time of applying the load	t_{l1}	0.1 s
DC short-circuit - start time	t_{f1}	0.25 s
DC short-circuit - end time	t_{f2}	0.45 s
Setpoint for maximum TPS current during the DC fault	$I_{DC,max,fault}$	960 A

The current and voltage of the DC side are illustrated in Figure 4.21 and Figure 4.22. The converter controller limits the DC voltage to around 500 V, by decreasing DC offset of the arm voltages and inserting submodules with a negative output voltage in some time instants, as depicted in Figure 4.23. As a result, the average of DC current is limited to $I_{DC,max,fault}$. The peak of DC current during the fault, however, is 967 A, which is slightly higher than $I_{DC,max,fault}$.

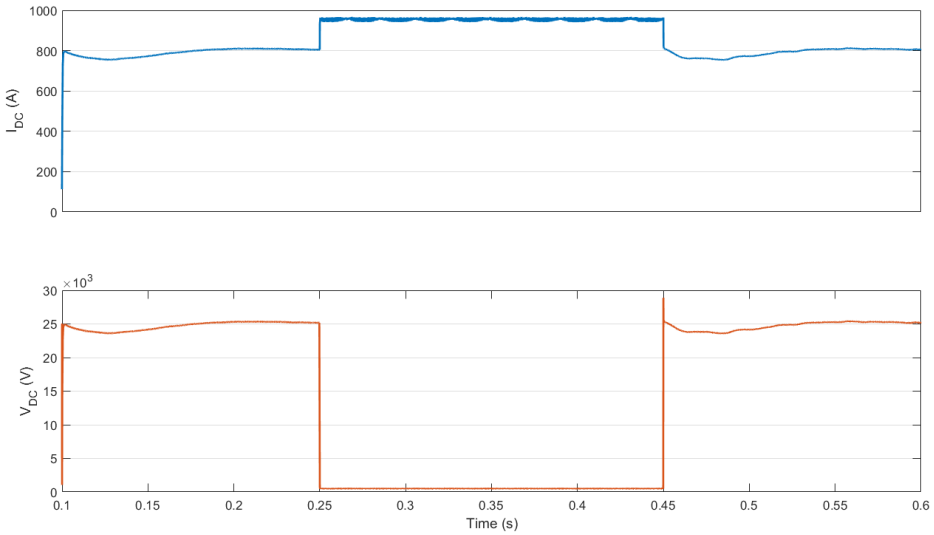


Figure 4.21 - DC-side current and voltage - case 4

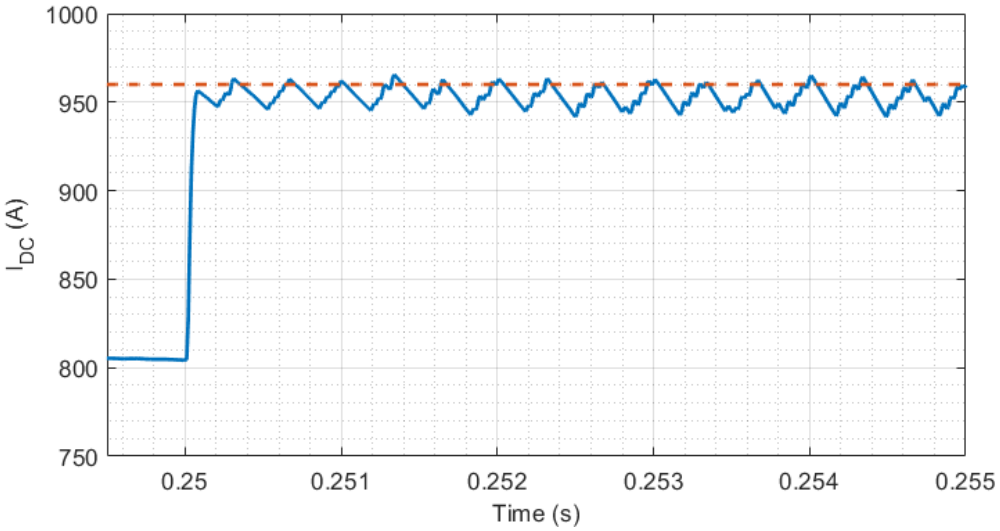


Figure 4.22 - DC current (magnified) - case 4

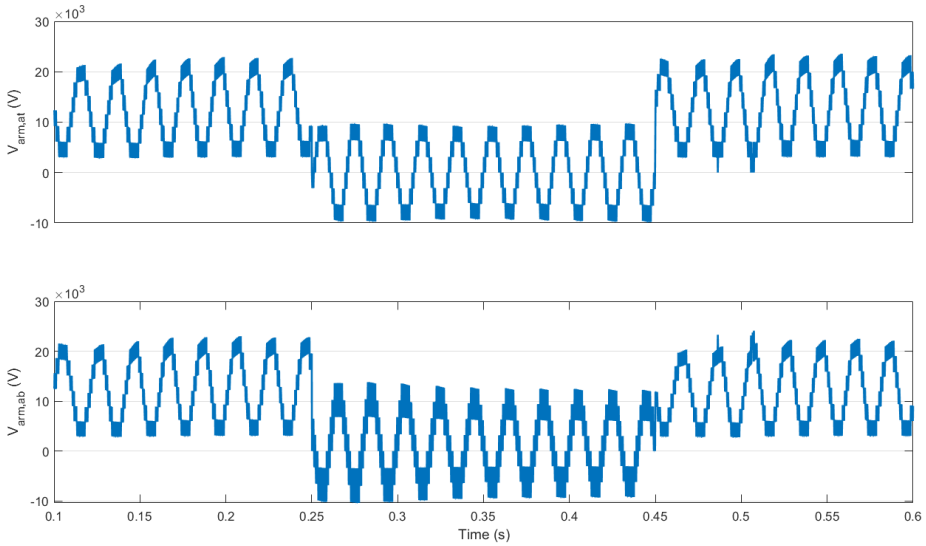


Figure 4.23 - Arm voltages of phase 'a' in the MMC-FB - case 4

After disconnecting the fault resistor, an overshoot with peak of 28.72 kV is seen in the DC voltage, followed by an undershoot with a minimum of 23.56 kV. The voltage is then regulated to the nominal value of 25 kV. Therefore, the TPS is able to restore the power transfer to the load and provide around 800 A after the DC fault.

As shown in Figure 4.24, the currents of the distribution network decrease to around 20 A RMS, indicating that the amount of active power transferred during the fault is insignificant. After the fault, the reactive power controller operates as normal, and the phase currents are in phase with the corresponding phase voltages.

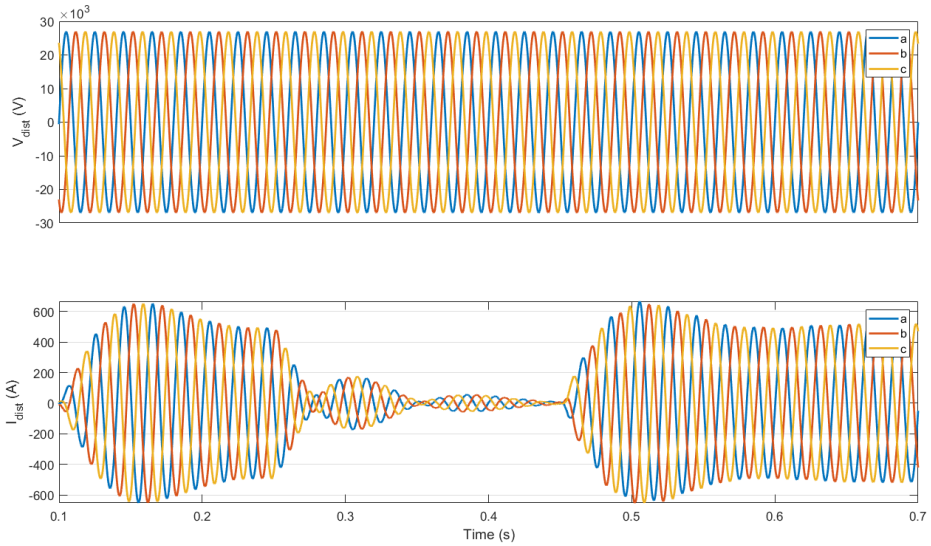


Figure 4.24 - Voltages and currents of 33 kV network - case 4

4.5 Case 5: Double end-fed MVDC railways

In this section, the simulation model is extended to a double-end feeding arrangement, where there are two MVDC TPSs at the two ends of the feeding system. The MVDC network is controlled by a distributed control strategy, in which the set point for the DC-side voltage is 25 kV for both the TPSs.

4.5.1 Case 5-1: Integration of renewable power sources

To investigate the effects of renewable energy sources on the MVDC railway network, a Photovoltaic (PV) farm is connected to the network at TPS 1, as shown in Figure 4.25. The PV farm consists of three groups of PV arrays, where each group is formed by 30 parallel strings. The strings, in turn, are made from 40 series-connected 'SunPower SPR-445NJ-WHT-D' modules. The maximum power and the open circuit voltage of the PV farm are 1.6 MW and 3.62 kV DC, respectively. A boost converter, shown in Figure 4.26, is simulated to step up the PV farm output voltage to 25 kV DC. The PV farm output current is measured and passed to a PI controller inside the boost converter

controller. The PI controller adjusts the boost converter duty cycle, ensuring that the PV farm operates at its maximum power point.

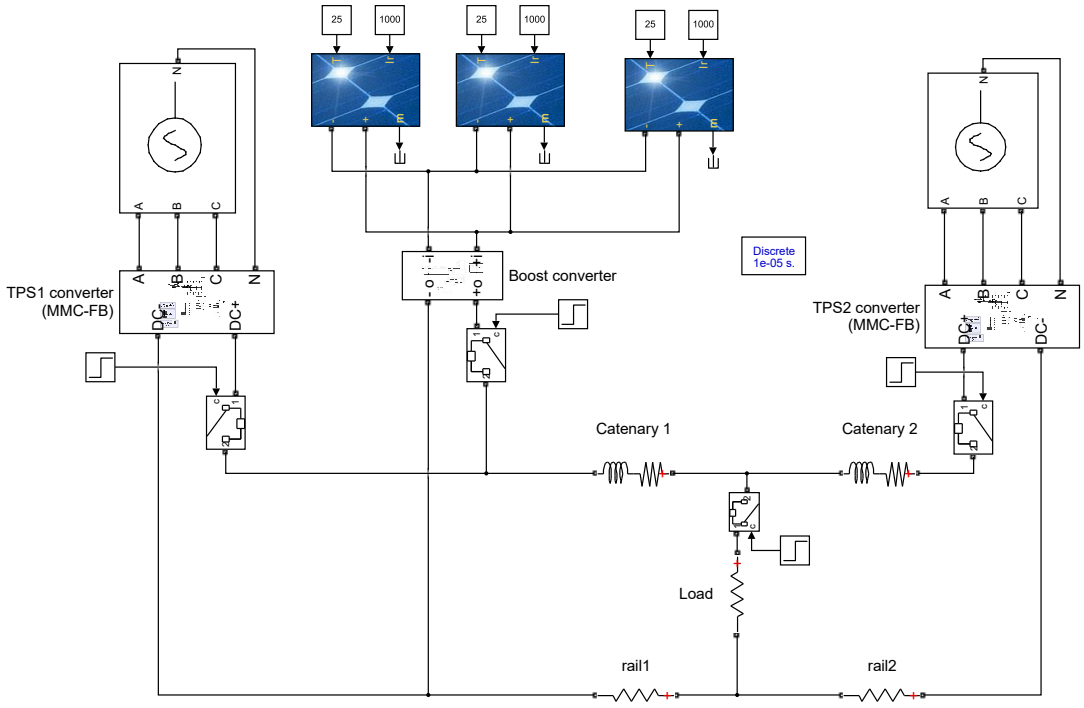


Figure 4.25 - MVDC railway network in double-end feeding arrangement and in the presence of a PV farm - case 5-1

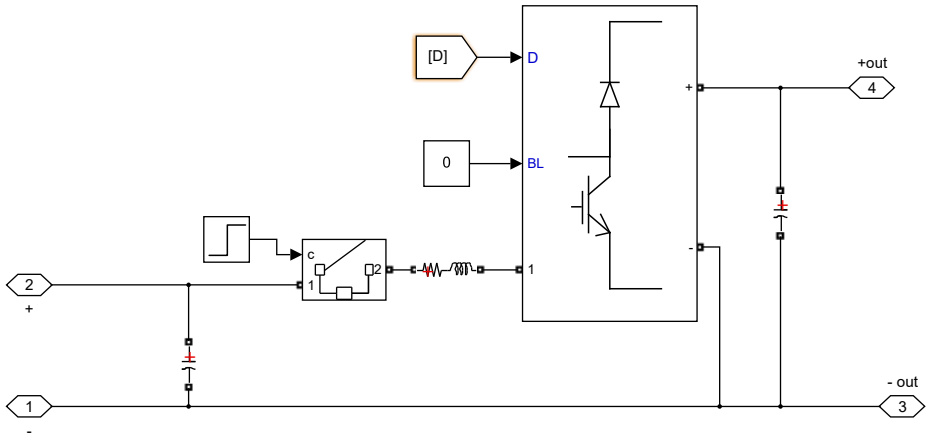


Figure 4.26 - Simulated boost converter - case 5-1

The other assumptions made in simulation case 5-1 are described in Table 4.2. The load consumption is modelled by a constant load resistor located between the TPSs. The

value of resistance corresponds to a power consumption of 16 MW at a fixed voltage of 25 kV. TPS 1, TPS 2, the PV farm and the load resistor are connected to the MVDC railway network at the time instants t_{TPS1} = 0.20 s, t_{TPS2} = 0.21 s, t_{PV} = 0.22 s and t_{Load} = 0.26 s, respectively.

Table 4.2 - Parameters used in simulation case 5-1

Parameter	Symbol	Value
Distance between two TPSs	D	40 km
Distance between TPS 1 and the load	d_1	30 km
Distance between the load and TPS 2	d_2	10 km
Maximum power of the PV farm	P_{PV}	1.6 MW
Power rating of each TPS	P_{TPS}	20 MW
Load resistance	R_L	39.06 Ω
Temperature of PV arrays	T_{PV}	25 °C
Solar irradiance	Irr_{PV}	1000 W/m^2

The aim of this simulation case is to investigate the railway operation in steady state. Therefore, the simulation results are analysed from t_{Load} = 0.26 s onwards. The DC-side voltage of TPS 1, TPS 2, the boost converter (railway side) and the load voltage are presented in Figure 4.27. After the transient related to connection of the PV farm, the voltages lie within the acceptable range for the MVDC railway system. In particular, the average voltage across the load is 24.6 kV (0.98 pu).

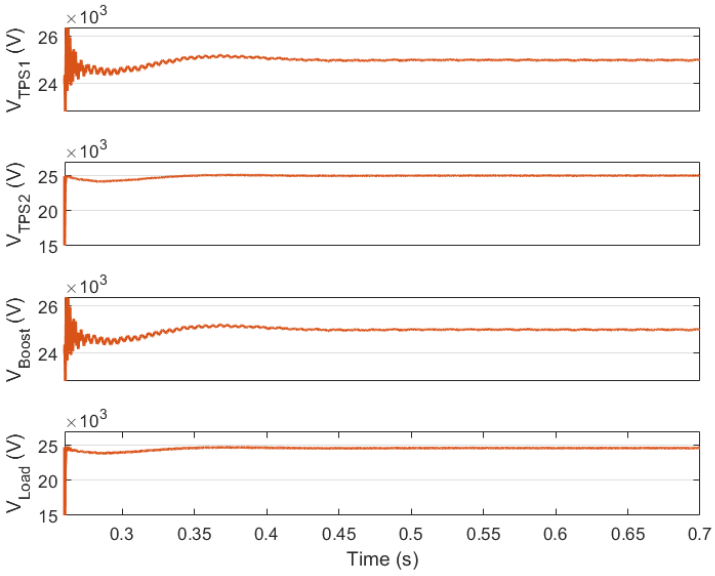


Figure 4.27 - DC-side voltage at TPS 1, TPS 2, boost converter and load voltage - case 5-1

To check the proper functionality of MMC-FB in TPS 1, the voltage of capacitors in phase ‘a’ of the MMC-FB is shown in Figure 4.28. It can be seen that the capacitor voltages are controlled around the set point in steady state. In addition, the evaluated TDD at TPS 1 (distribution network side) indicates that TPS 1 operates normally and TDD remains below 1% in steady state (Figure 4.29).

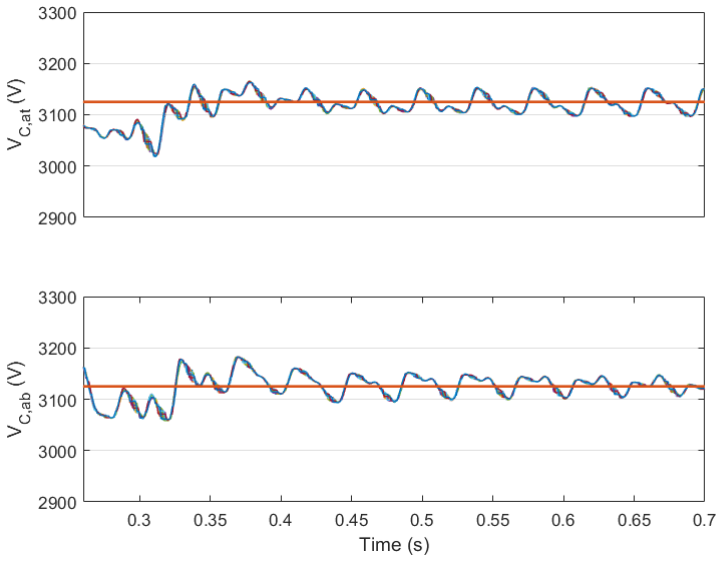


Figure 4.28 - Capacitor voltages of phase ‘a’ of the MMC-FB in TPS 1 - case 5-1

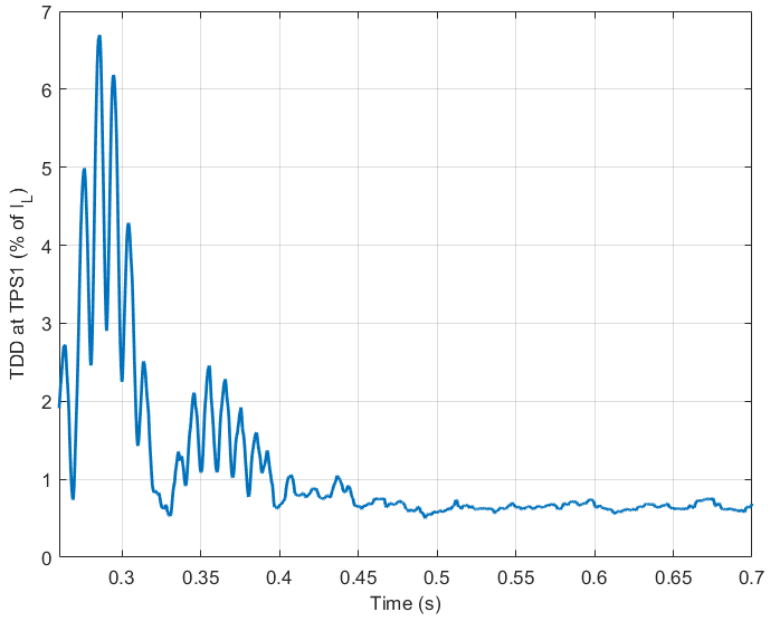


Figure 4.29 - TDD at TPS 1 (33 kV network side) - case 5-1

Concerning TPS 2, the voltages and currents of the distribution network are illustrated in Figure 4.30, showing normal operation of TPS 2 and active power transfer at an approximately unity power factor.

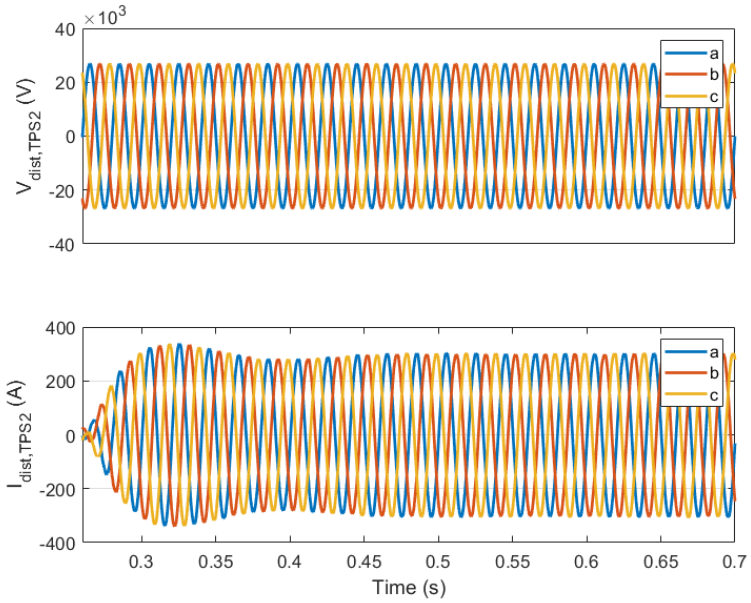


Figure 4.30 - Voltages and currents at TPS 2 (33 kV network side) - case 5-1

Figure 4.31 depicts the power transferred from the TPSs and boost converter (PV farm) to the load. The power oscillation at the boost converter terminals is damped within 0.25 s. The average transferred power and the average power losses in the MVDC network between t_{av1} = 0.5 s and t_{av2} = 0.7 s are presented in Table 4.3, showing that the output power of each TPS is inversely proportional to its distance from the load.

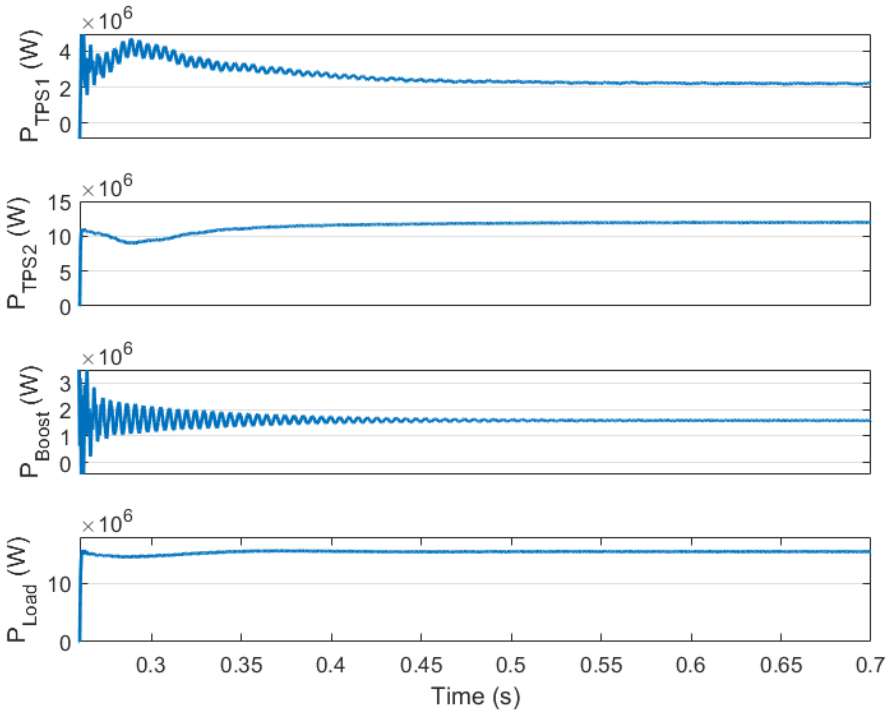


Figure 4.31 - Power of the TPSs, boost converter (PV farm) and load - case 5-1

Table 4.3 - Average transferred power - cases 5-1 and 5-2

	TPS 1	TPS 2	PV farm	Load	Losses
Simulation case 5-1 (MW)	2.23	11.94	1.59	15.5	0.26
Simulation case 5-2 (MW)	−3.75	11.92	7.59	15.5	0.26

4.5.2 Case 5-2: Higher penetration of renewable sources

In this section, operation of the MVDC system in the presence of higher renewable penetration is analysed and all the assumptions are the same as for case 5-1. The only

difference is the maximum power of the PV farm, which is assumed to be 8 MW. The controller of the boost converter is also retuned.

Similarly to case 5-1, the simulation results show the normal operation of the MVDC railways and TPSs. According to Table 4.3, the PV farm delivers an average of 7.59 MW to the MVDC bus, from which 3.84 MW is consumed by the load, overhead lines and running rails, and 3.75 MW is injected into the distribution network by TPS 1. The voltage and current of phase 'a' at TPS 1 (distribution network side) are demonstrated in Figure 4.32, indicating that the active power is normally transferred to the distribution network.

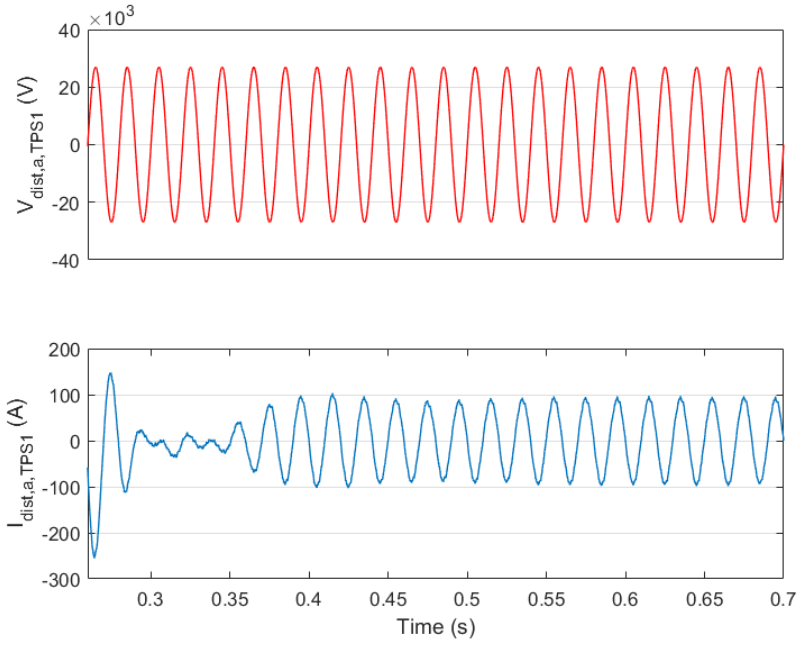


Figure 4.32 - Voltage and current of phase 'a' at TPS 1 (33 kV network side) - case 5-2

4.5.3 Case 5-3: Power sharing between the TPSs

In this simulation case, a centralised control strategy is used to equally share the trains' load between the two TPSs in the network shown in Figure 4.33. The DC voltage

reference for TPS 1 is fixed to 25 kV. For TPS 2, however, the DC voltage reference is determined by the central control unit of the MVDC network.

As shown in Figure 4.34, the voltages and currents in DC terminals of TPS 1 and TPS 2 are measured and transmitted to the central control unit, where a PI controller calculates the DC voltage reference for TPS 2, so that the TPSs provide the same share of the load. The PI controller is enabled at t_{ctrl} = 0.26 s, and the controller output is fixed to 25 kV before the activation. Moreover, the controller output is limited between 19 and 27.5 kV to ensure that the MVDC bus voltage remains within the permitted limits. On the DC side of the TPSs, an LC filter (20 µF, 1.3 mH) is implemented to improve the controller performance. Table 4.4 presents the rest of the simulation parameters.

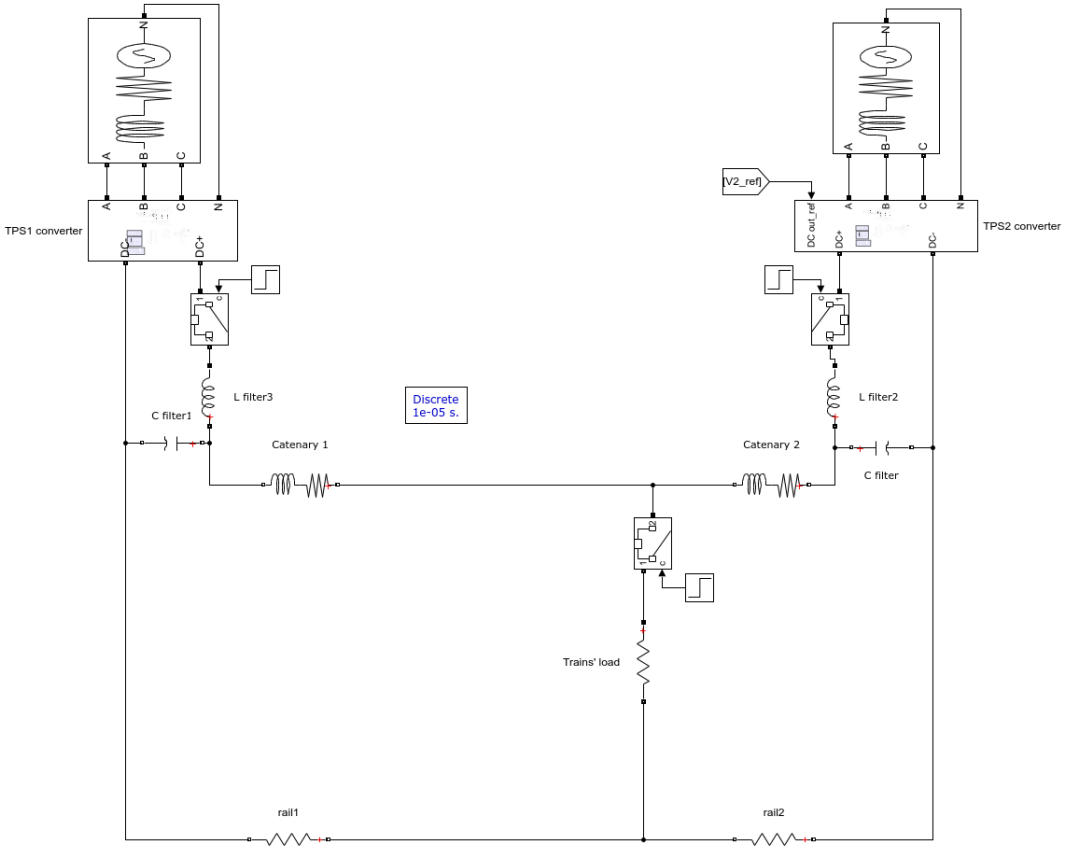


Figure 4.33 - MVDC railway network - case 5-3

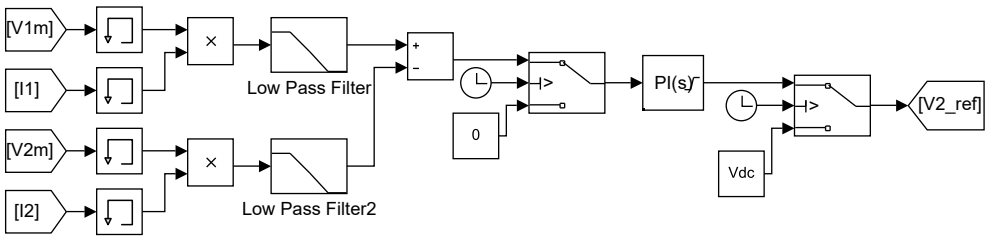


Figure 4.34 - Central controller of the MVDC network - case 5-3

Table 4.4 - Simulation parameters - case 5-3

Parameter	Symbol	Value
Distance between two TPSs	D	40 km
Distance between TPS 1 and the load	d_1	35 km
Distance between the load and TPS 2	d_2	5 km
Power rating of each TPS	P_{TPS}	20 MW
Load resistance	R_L	39.06 Ω
Time of applying load	t_L	0.35 s

Figure 4.35 demonstrates the DC voltage at TPS 1, TPS 2 and the load after t_L, which are close enough to the nominal value of 25 kV. As a result of the PI controller action, the ripples in TPS 1 DC voltage are larger, and the peak–peak ripple in steady state (after t = 0.5 s) is 2.3%.

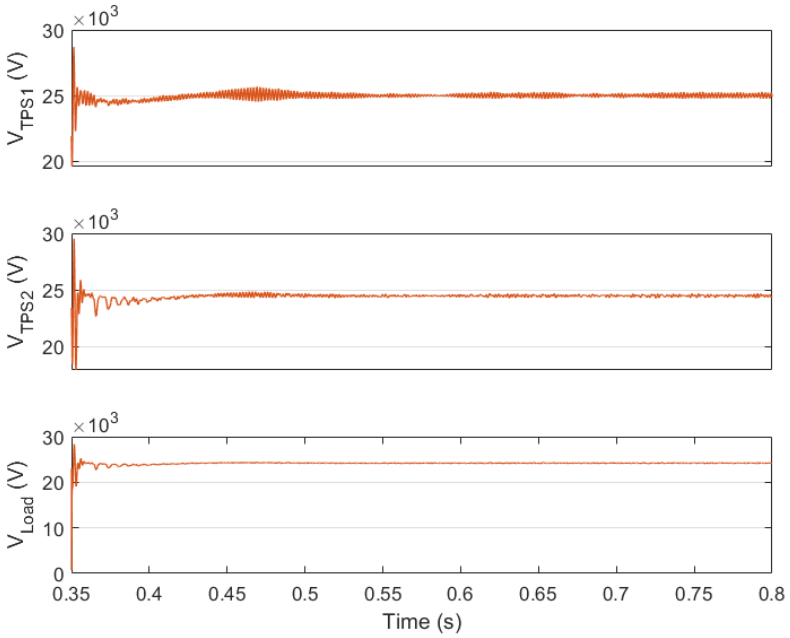


Figure 4.35 - DC voltage at TPS 1, TPS 2 and across the load - case 5-3

The power on the DC side of TPS 1 and TPS 2, and power consumed by the load, overhead lines and running rails are presented in Figure 4.36. The TPSs provide an equal share of the load, with an average of 7.66 MW between t = 0.5 s and t = 0.8 s. This means that the power rating of the TPSs can be decreased, e.g., to 10 MW when the load is shared between the TPSs.

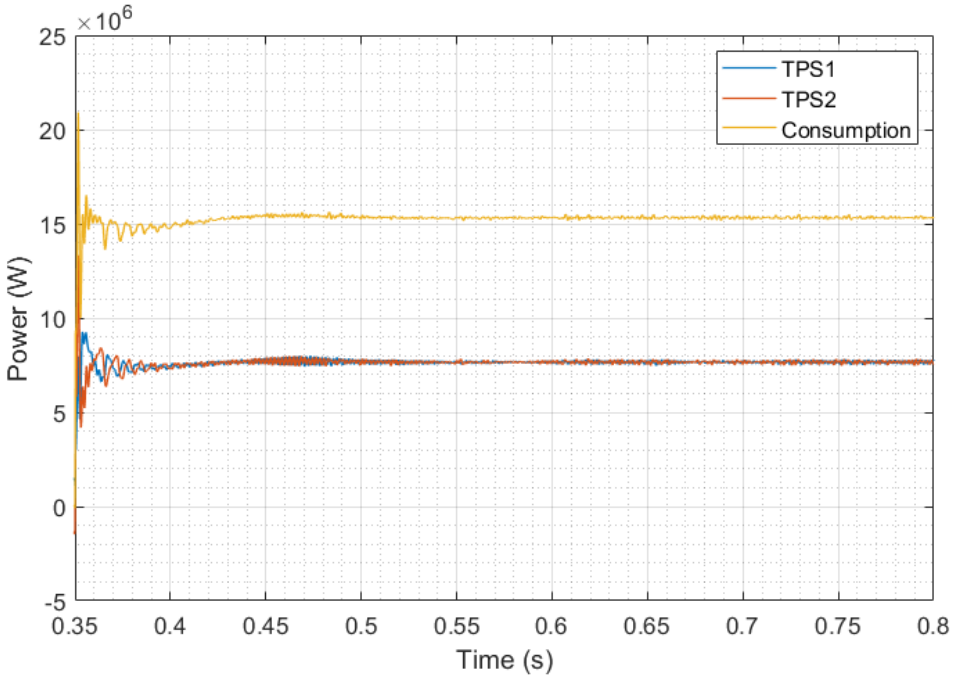


Figure 4.36 - Power of TPS 1 and TPS 2 (DC side), and power consumed by the load and MVDC railway network - case 5-3

On the other hand, the power provided by TPS 1 is transmitted to the load via 35 km of overhead lines. The average power losses of the railway network with and without implementing the centralised control strategy are compared in Table 4.5. The table shows that, with the assumptions made in this simulation case, the total average losses in the MVDC railway network increase when the load is shared equally between the TPSs. Therefore, there is a compromise between decreasing the power rating of the TPSs, and the total losses in the railway network. In addition, the centralised control strategy needs an infrastructure to transmit data from the TPSs to the central controller and vice versa, which makes it more complex and expensive. Hence, the economic feasibility of this control strategy totally depends on the case.

Table 4.5 - Average power losses of the MVDC railway network between t = 0.5s and t = 0.8s - case 5-3

Average power	Central controller enabled	Central controller disabled (DC ref for both TPSs = 25 kV)
$\bar{P}_{OHL1} + \bar{P}_{rail1}$ (kW)	147.8	38.2
$\bar{P}_{OHL2} + \bar{P}_{rail2}$ (kW)	51.5	117.8
Total (kW)	199.3	156.0

4.6 Case 6: MVDC railways with multiple TPSs

To analyse an MVDC railway network with multiple TPSs, the simulation model is extended to the system shown in Figure 4.37. The AC distribution networks connected to

TPS 1 and TPS 2 are in phase. However, the initial phase angles for the distribution networks at TPS 3 and TPS 4 are 30° and 60°, respectively. The MVDC network is controlled by a decentralised control strategy, where the DC voltage reference for each TPS is 25 kV. Table 4.6 summarises the parameters used in this simulation case.

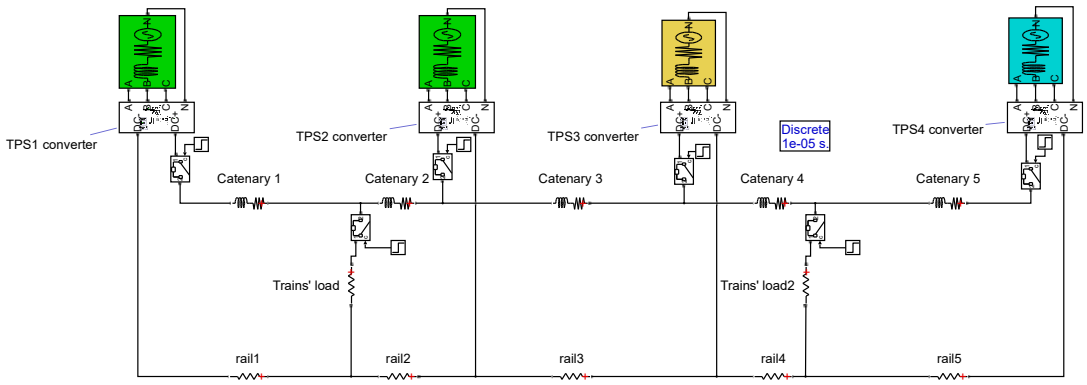


Figure 4.37 - MVDC railways with multiple TPSs - case 6

Table 4.6 - Simulation parameters - case 6

Parameter	Symbol	Value
Distance between TPS 1 and load 1	d_1	20 km
Distance between load 1 and TPS 2	d_2	10 km
Distance between TPS 2 and TPS 3	d_3	30 km
Distance between TPS 3 and load 2	d_4	5 km
Distance between load 2 and TPS 4	d_5	25 km
Power rating of each TPS	P_{TPS}	20 MW
Load 1 resistance	R_{L1}	39.06 Ω
Load 2 resistance	R_{L2}	39.06 Ω
Time of applying loads	t_L	0.3 s

Based on the simulation results, the voltages at the TPS terminals and across the loads are in the allowable limit and regulated at 25 kV. In particular, the average voltages (from t = 0.5 s to t = 0.9 s) across load 1 and load 2 are 24.64 and 24.78 kV, respectively. Figure 4.38 depicts the power of the TPSs on the DC side, indicating that the power profile for each TPS reaches a steady state, and TPS 3 provides the largest share of the consumption.

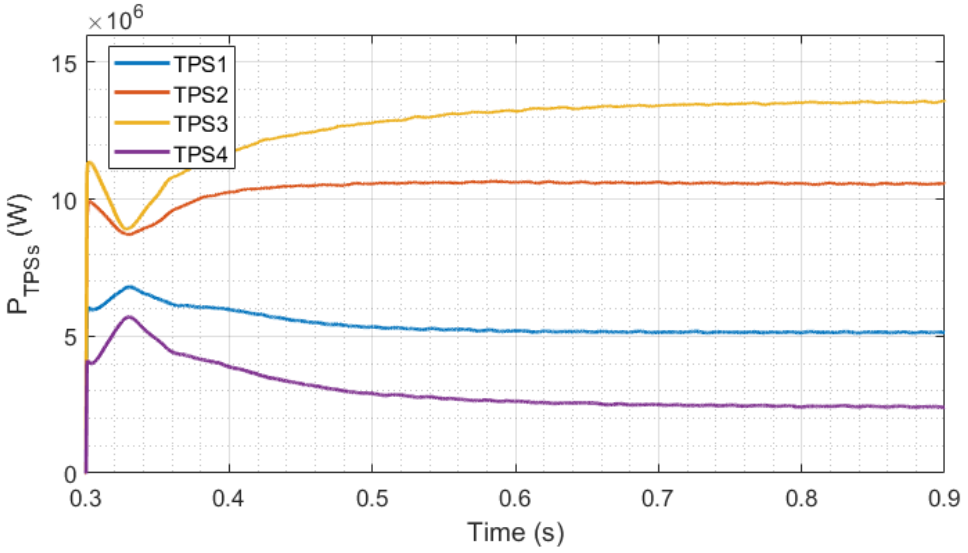


Figure 4.38 - Power of TPSs on the DC side - case 6

The sum of the power provided on the DC side of the TPSs and summation of the power consumed by the loads are demonstrated in Figure 4.39. The difference between the curves equals the power losses in the overhead lines and running rails, which is constant in the steady state.

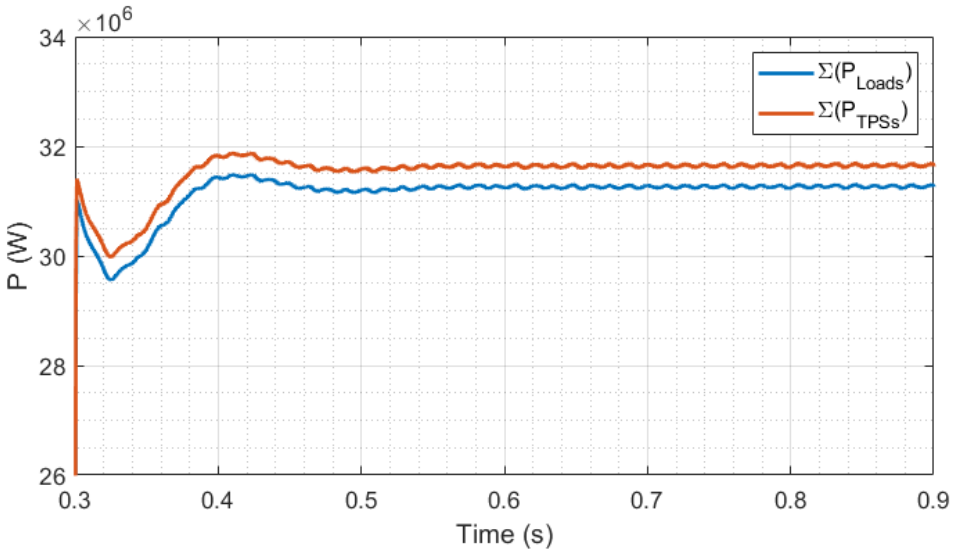


Figure 4.39 - Sum of the power provided by the TPSs and consumed by the loads - case 6

4.7 Case 7: Loss analysis of MMC-FB in an individual MVDC TPS

Based on the methodology presented in the previous chapter, the MVDC network losses and MMC-FB losses are evaluated in this section. The MVDC system under study consists of a TPS and the trains' load is modelled by a controlled current source located at d_{Load} = 1 km. The DC current profile is the same as in Figure 4.1, where the current load is fixed at 640 A (equivalent to 16 MW at 25 kV) between t_1 = 0.3 s and t_2 = 0.8 s. Table 4.7 presents the average power consumed by the load, overhead lines and the rail between t_1 and t_2, implying that the converter losses are the major part of the losses in this simulation case while the rail losses are negligible.

Table 4.7 - Average power consumed in the MVDC railways - case 7

	Load consumption	Losses in overhead lines	Rail losses	Converter losses
Average power (kW)	15995.9	32.8	3.1	346.7

The MMC-FB efficiency is also evaluated in various loading conditions with the same method and the results are illustrated in Figure 4.40. In light loading conditions, the converter losses are considerable in comparison to the output power and the converter efficiency is low. As the load increases, the efficiency improves, and it reaches 97.9% in full load (16 MW). The negative values for the power correspond to the converter operating in regenerative braking mode. Similarly, the MMC-FB efficiency in regenerative braking mode increases when the amount of power injected into the distribution network increases.

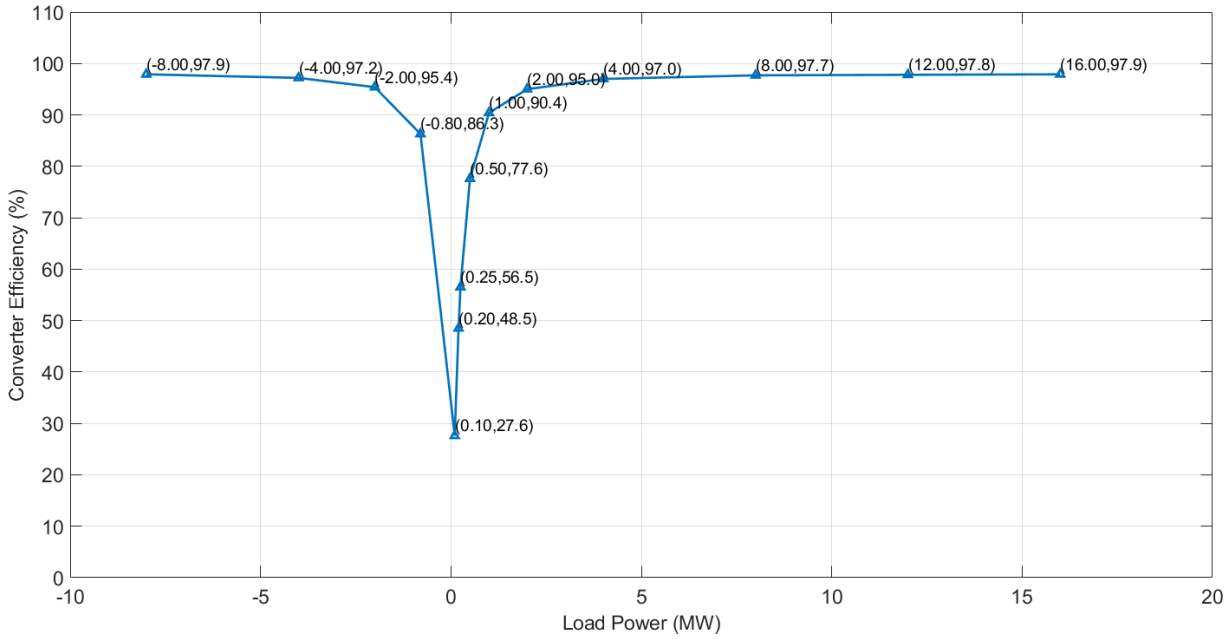


Figure 4.40 - MMC-FB efficiency evaluated under different loads - case 7

4.8 Summary

In this chapter, the MVDC railway models developed in Matlab/Simulink were run in various simulation cases to analyse the railway performance in terms of power quality on both AC and DC sides. First, an individual MVDC TPS was tested in several operating conditions, i.e., in normal operation, during regenerative braking, during an AC voltage dip and during DC-side short-circuit. The simulation models were then extended to a double end-fed MVDC railway system, and integration of renewable sources (a PV farm) was investigated. Moreover, a centralised control strategy for sharing the railway load between the TPSs was examined. The model was then further extended to an MVDC railway with multiple TPSs. Finally, the efficiency of an MMC-FB was evaluated in different loading conditions.

5 EXPERIMENTAL SETUP OF AN MVDC TPS

In this chapter, the designed experimental setup for an individual MVDC TPS is presented. The experimental setup is a small-scale 350 W lab demonstrator, connected to a 415 V three-phase AC network. The AC voltage is stepped down by an autotransformer, and an MMC-FB prototype acts as the AC-DC power converter of the TPS. There are two 175 V submodules in each arm of the MMC-FB, and the converter provides 350 V on the DC side.

Although the experimental setup is a small-scale model, the analyses are still valid for a medium-voltage TPS because the principles of design and operation are similar, and the TPS transformer and converter can be easily scaled up to higher voltage and power levels. As the main part of the TPS, the MMC-FB can operate at higher voltage levels without a dramatic change in the design principles and control algorithm, i.e., by considering a higher voltage rating for the submodules and/or implementing a higher number of submodules in each arm of the MMC-FB.

For instance, the submodules can be designed with 6.5 kV IGBT–diode modules. Having eight submodules per arm, the MMC-FB is able to provide 25 kV on the DC side. Similar to the developed small-scale lab demonstrator, the measurement circuitries and the gate drivers (electronic side) should be isolated from the power circuit in the real-scale MMC-FB. Moreover, the proposed control algorithm is easily extendable for a higher number of submodules.

The MMC-FB in the experimental setup is controlled with the same control algorithm presented in section 3.3.2. The only difference is that the outer loop in the q axis has not been implemented and $i_{q,ref}$ is assumed to be 0. In other words, the reactive power

transfer is only controlled on the converter side, and it is uncontrolled on the network side.

The experimental setup has been simulated in Matlab/Simulink, to estimate the converter behaviour in charging phase and normal operation before the practical implementation.

5.1 Hardware design

5.1.1 Overall arrangement

Figure 5.1 represents the schematic diagram of the developed TPS experimental setup. There is an MMC-FB as the TPS converter, connected to a three-phase AC network through the line inductors and an autotransformer. On the DC side, a DC electronic load (H&H PL 1540) is used to mimic the trains' load. The overall view of the experimental setup, located in the Birmingham Centre for Railway Research and Education (BCRRE) lab at the University of Birmingham, is shown in Figure 5.2. The setup specifications are described in Table 5.1.

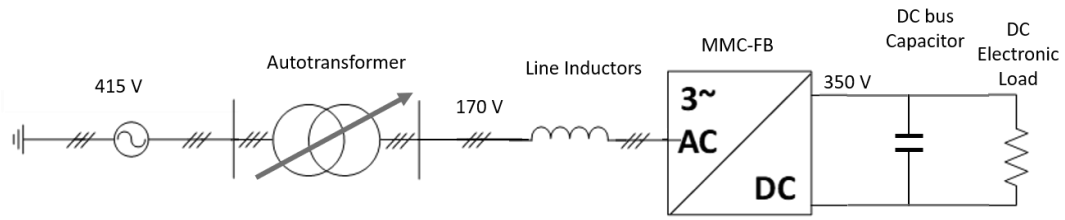


Figure 5.1 - Schematic diagram of the TPS experimental setup

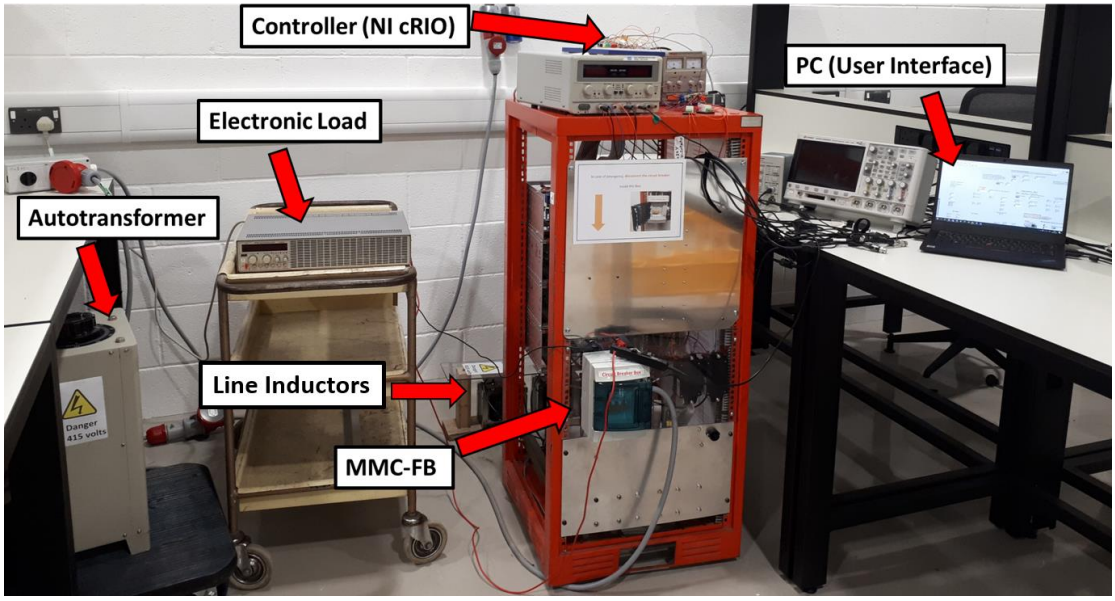


Figure 5.2 - The TPS experimental setup

Table 5.1 – Specifications of the TPS experimental setup

Parameter	Value
Nominal voltage on the DC side	350 V
DC current of the power converter at full load	1 A
AC voltage (network side)	415 V
AC voltage (converter side)	170 V
Arm inductance	650 µH
Line inductance (per phase)	16.5 mH
Number of submodules (per arm)	2
Nominal voltage of the capacitor in each submodule	175 V
Capacitance (per submodule)	2200 µF
Capacitance of DC filter	1000 µF
Carrier frequency	5 kHz

5.1.2 Power circuit and control circuitries of the MMC-FB

The MMC-FB setup was developed as part of a former research project on advanced power converters for railway traction systems (a new traction drive) [28], [29] and was available in the lab. The designed full-bridge submodule is shown in Figure 5.3, and the converter is formed by 12 identical submodules (2 submodules per arm). Each submodule mainly consists of a full-bridge IGBT module (Mitsubishi CM75BU-12H),

isolated gate drivers, an electrolytic capacitor, a voltage sensing circuitry and DC-DC converters for providing isolated supplies to the gate drivers. The submodules, arm inductors, arm current sensor cards, routing cards and the DC bus capacitor are placed inside a rack, as depicted in Figure 5.4 and Figure 5.5. More details about the power circuit and measurement circuitry of the MMC-FB can be found in [28].

Figure 5.3 - Full-bridge submodule

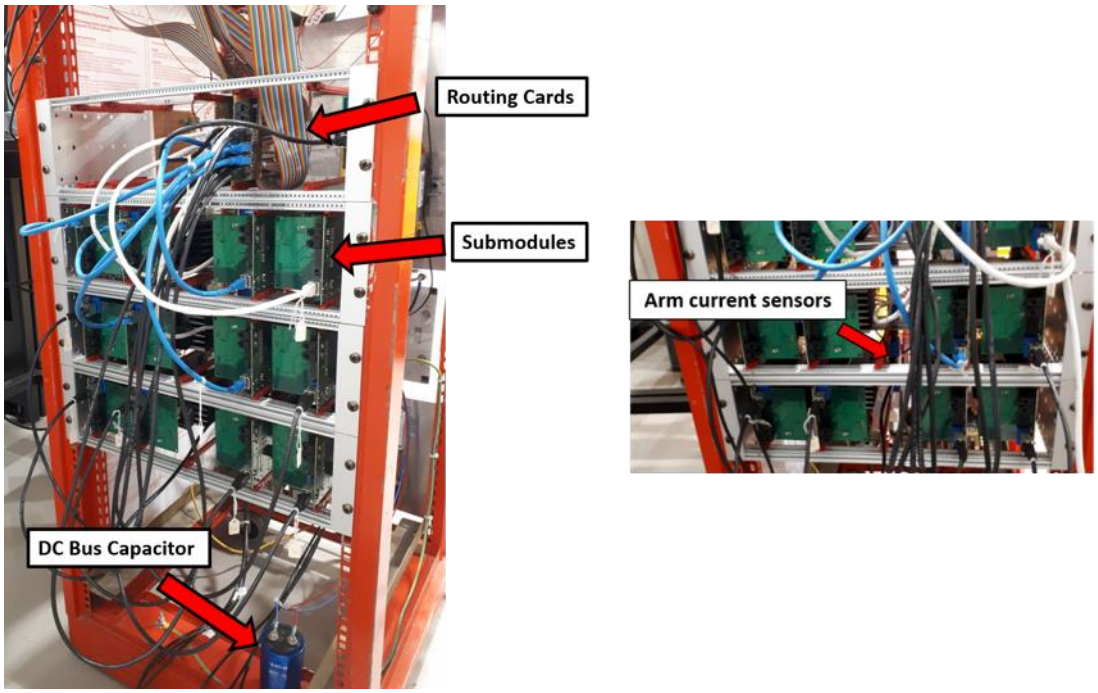


Figure 5.4 - MMC-FB experimental setup

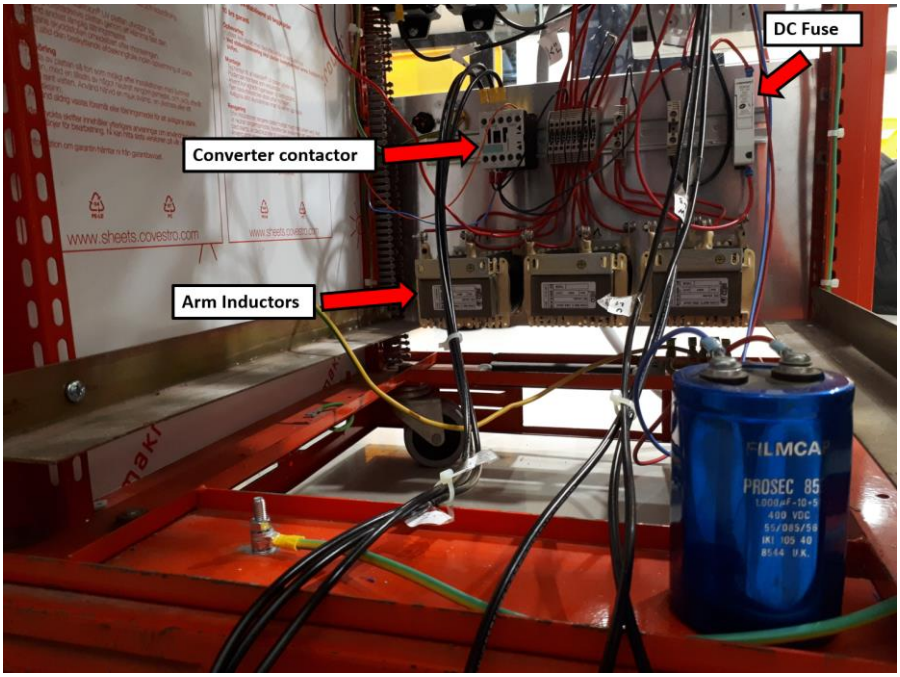


Figure 5.5 - MMC-FB experimental setup

To develop the TPS experimental setup, the existing MMC-FB setup has been modified to operate as a grid-tied AC-DC converter. First, necessary changes have been made to the submodules to increase the operating voltage to 175 V. On the AC side, a main AC circuit breaker, the charging resistors and the line inductors have been installed. Two voltage transducers (LEM DVL 750) have been added to measure two line-to-line voltages, as presented in Figure 5.6 and Figure 5.7. In addition, a DC current sensor card has been developed with a similar design to the arm current sensor cards. The only difference is the turns ratio of the current transducer, which is 4/1000 in the DC current sensor card.

The MMC-FB prototype was originally designed to be controlled with an OPAL-RT controller. In this research, however, a National Instruments Compact RIO-9082 (NI cRIO-9082) has been selected for implementing the control, modulation and sorting algorithms. Therefore, the connectors between the routing cards and controller have been modified, and ribbon cables have been used to connect the routing cards to the

Analogue Input (AI) and Digital Output (DO) modules of the controller. Based on the control algorithm requirements, there are 21 AI channels to transmit the submodule voltages (12), arm currents (6), AC-side voltages (2) and DC current to the controller. Moreover, there are 38 DO channels to send gate signals to the IGBTs (36) and control the contactors through relay modules (2).

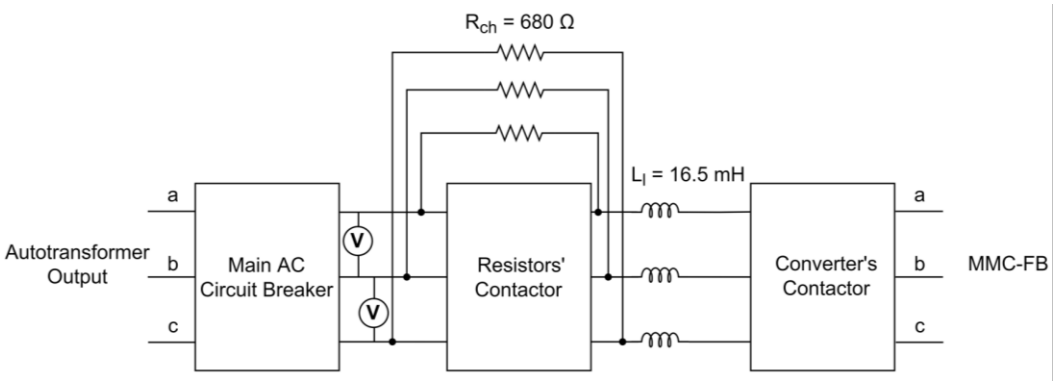


Figure 5.6 - Diagram of connected contactors on the AC side of MMC-FB

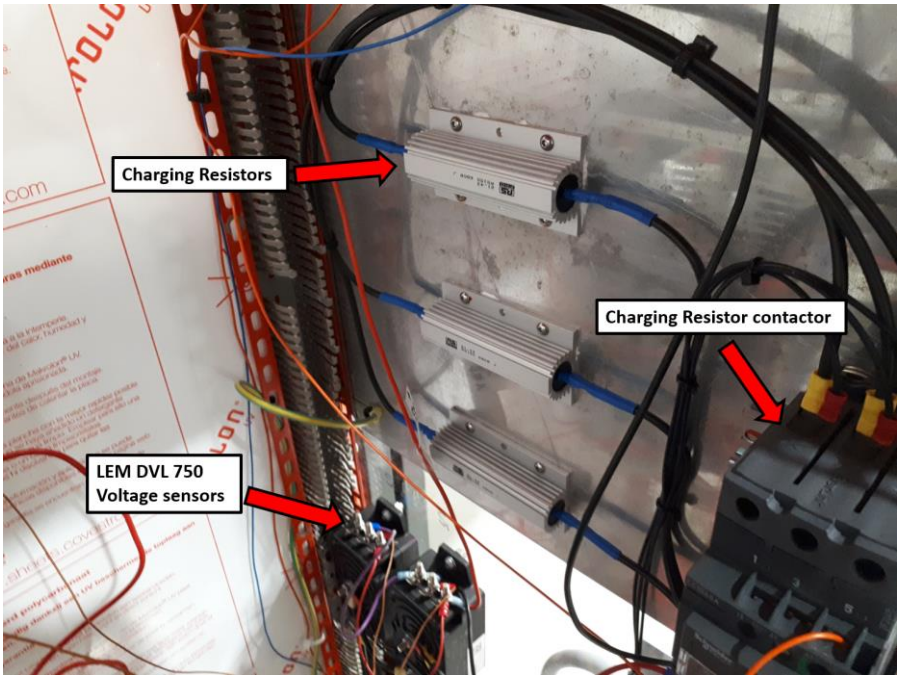


Figure 5.7 - Charging resistors and voltage transducers on the AC side of the MMC-FB

5.1.3 MMC-FB control unit

As shown in Figure 5.8, the MMC-FB control unit (NI cRIO-9082) has been placed on the MMC-FB rack. The NI cRIO-9082 is equipped with an Intel Core i7-660UE CPU which is used as a Real-Time (RT) target. It also has a Xilinx Spartan-6 LX150 Field-Programmable Gate Array (FPGA) board. There are also eight slots on the controller chassis to accommodate the Analogue Output (AO), AI and DO modules. The controller is connected to a laptop through an ethernet cable and is programmed via NI LabVIEW software.

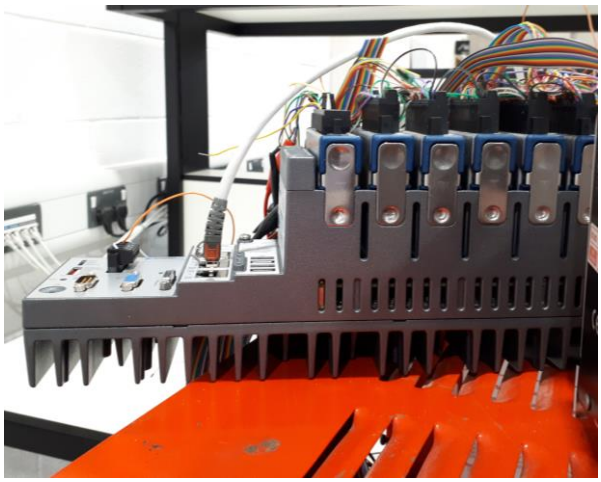


Figure 5.8 - MMC-FB control unit: NI cRIO-9082

5.2 Software design

5.2.1 FPGA program

The controller codes are mainly implemented on the FPGA board. The FPGA board is configured to be directly connected to the AO, AI and DO modules and operate at a clock rate of 40 MHz. The FPGA program is mainly formed by four ‘while loops’, which are run continuously with different loop rates.

Figure 5.9 presents the first loop, which produces a 5 kHz triangular carrier waveform. A Boolean register is used as a flag to synchronise this loop with the second loop. When the value of this register becomes ‘True’, the flat sequence inside the first loop is run. The ‘FXPT Triangle Gen’ function [30] produces triangular carriers between −1 and 1. Therefore, 1 is added to the function’s output and the result divided by 2, so the carrier waveform lies within the range 0 to 1. Finally, the carrier is delayed by 100 steps, so the produced carrier waveform starts from 0 when the sequence is initiated.

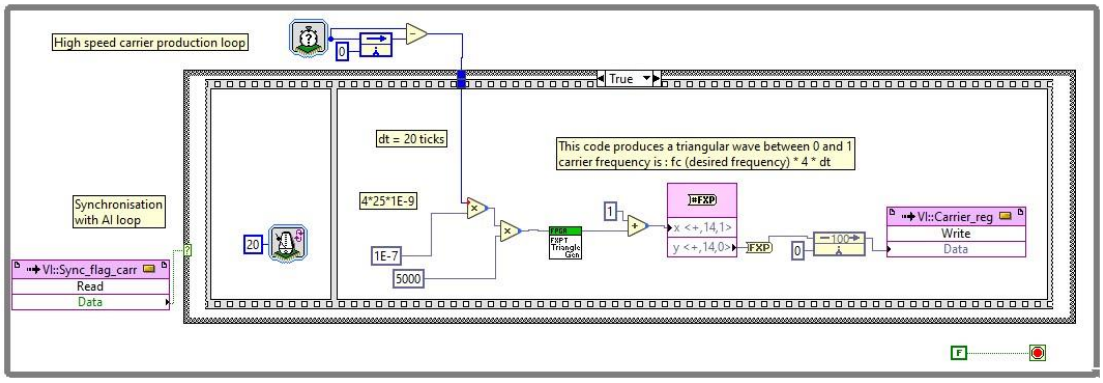


Figure 5.9 - Carrier production loop - FPGA program

The second loop, shown in Figure 5.10, consists of four main parts. In part A (Figure 5.11), the measured voltages and currents are acquired from AI channels every 100 µs and are passed to parts B and C. The samples are also stored in the registers to be used in other loops. In addition, the submodules’ voltages are transferred to the RT target program via a First-Input-First-Output (FIFO) structure for monitoring purposes. There are also two comparators which detect overvoltage fault in the submodules and overcurrent fault in the arms.

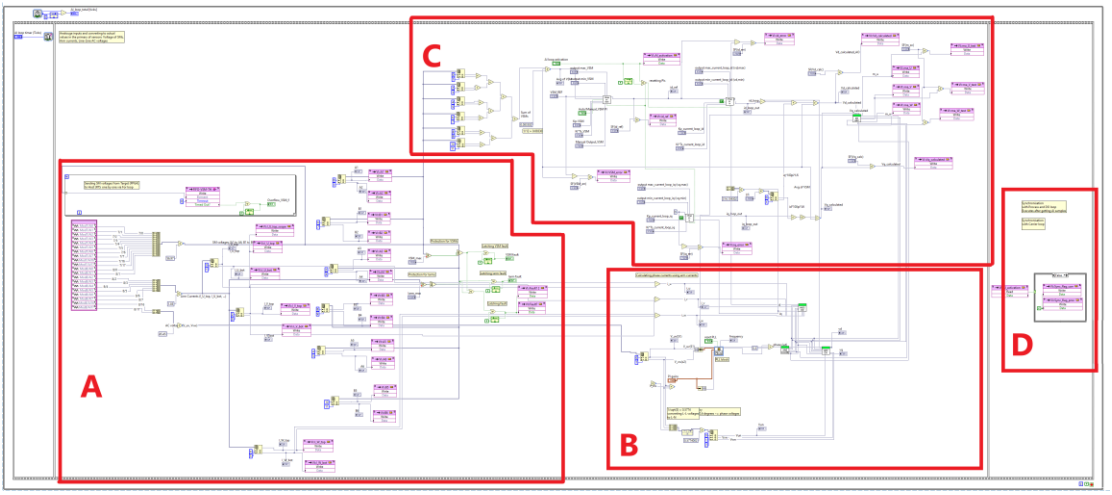


Figure 5.10 - The second loop - FPGA program

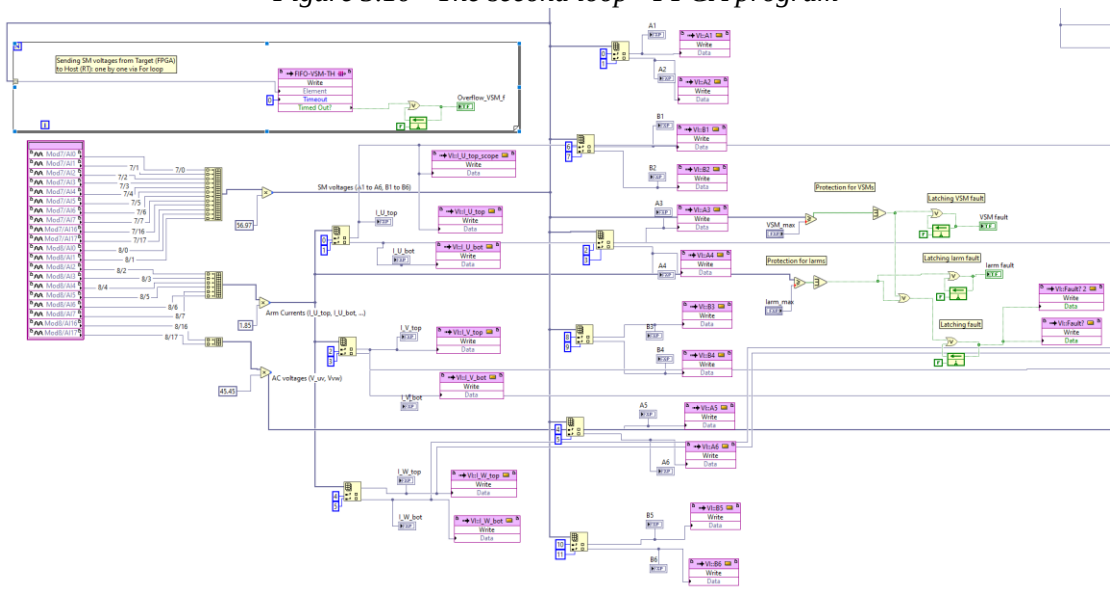


Figure 5.11 - The second loop, part A - FPGA program

In part B (Figure 5.12), the line-to-line voltages V_{ab} and V_{bc} are passed to a PLL block to determine the phase angle. The output of the PLL block is aligned with V_{bc}, i.e., $\sin \omega_t = V_{bc}$. To align the phase angle to the phase voltage V_{an}, 0.5 radians (90°) is added to the output of the PLL block. In addition, the phase voltages V_{an}, V_{bn} and V_{cn} are evaluated by shifting the measured line-to-line voltages and dividing by $\sqrt{3}$. The sine-based abc-dq transformation is then applied to the phase voltages and phase currents to evaluate V_d, V_q, i_d and i_q.

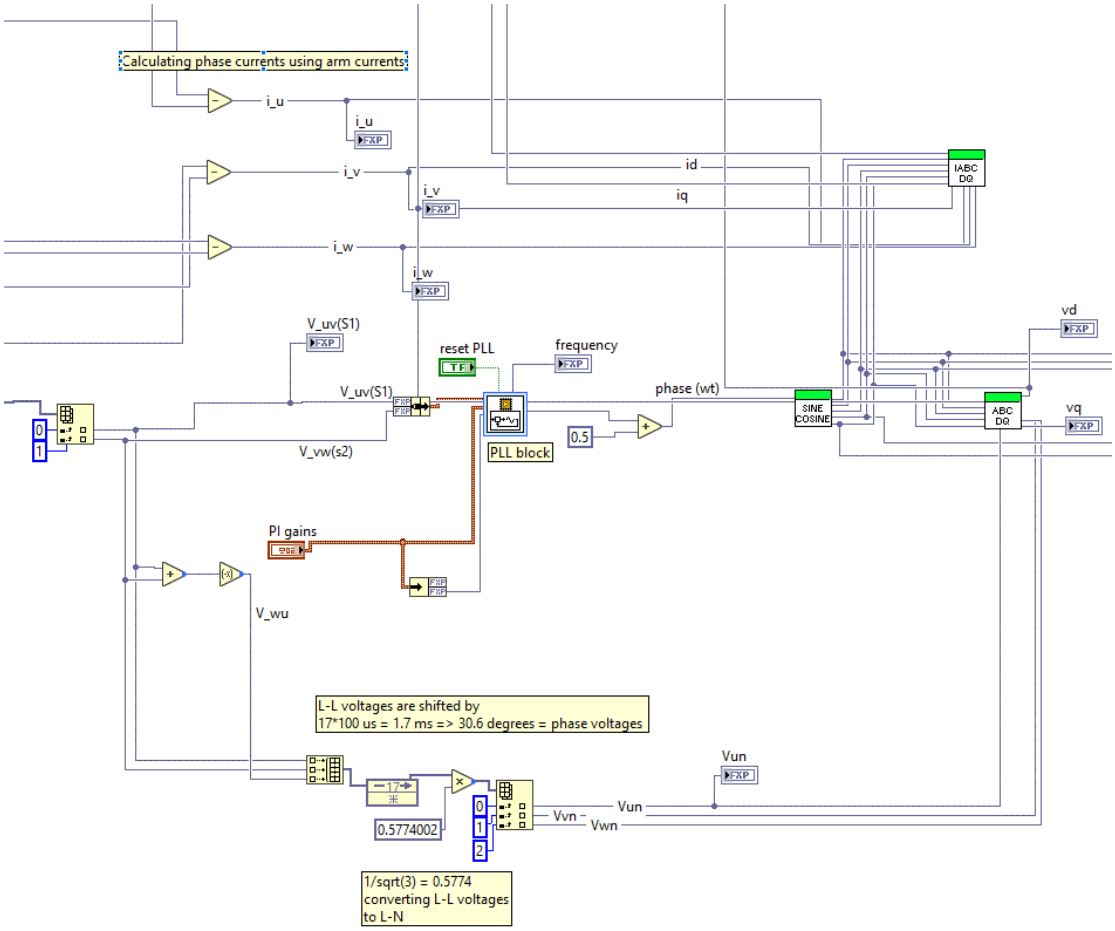


Figure 5.12 - The second loop, part B - FPGA program

In part C (Figure 5.13), the inner q axis, and outer and inner d axis control loops (introduced in chapter 3, section 3.3.2, MMC-FB control scheme) are implemented. The user can activate the PI controllers using a Boolean control. The value of this control is also stored in a register and used to synchronise the loops. As the outputs of the second loop, the calculated AC references are written in three registers and are passed to the third loop.

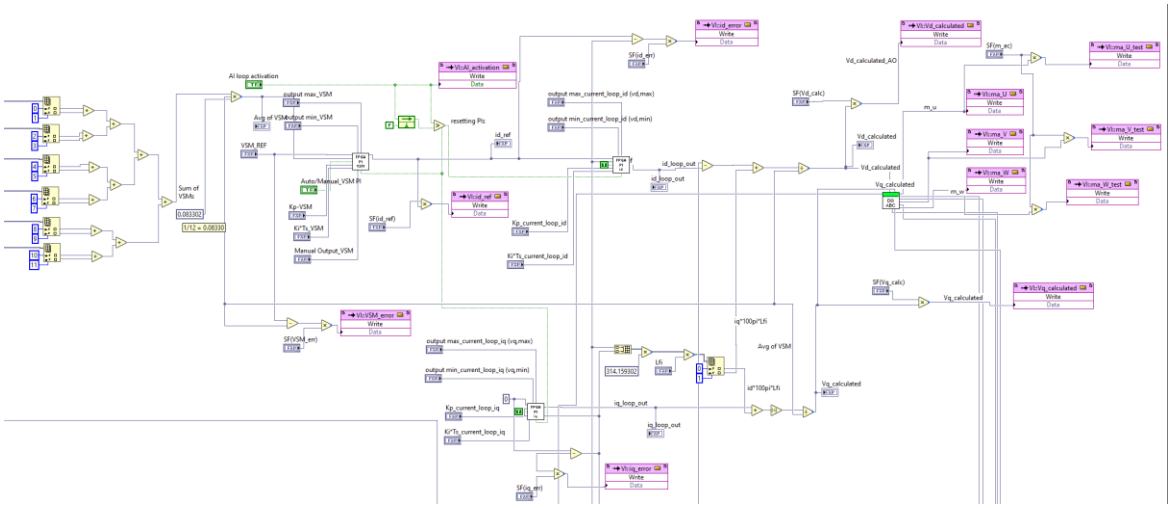


Figure 5.13 - The second loop, part C - FPGA program

In each period of the carrier waveform, the measured quantities are acquired and processed twice in the first loop. The case structure and registers in part D (Figure 5.14) are implemented to synchronise the three loops, ensuring that the sampling and calculations occur at the same time instants in all periods of the carrier waveform.

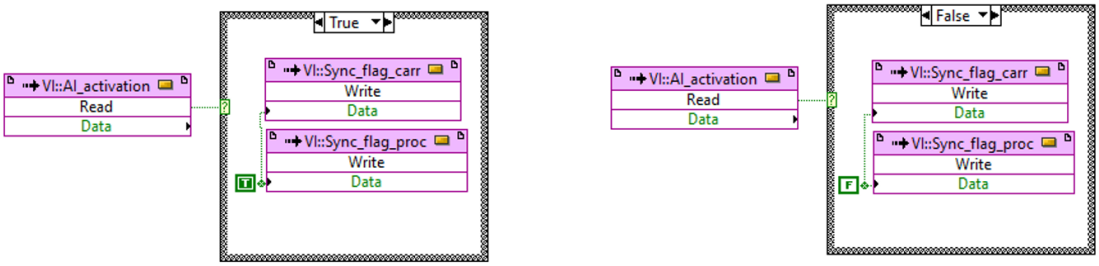


Figure 5.14 - The second loop, part D - FPGA program: (a) True case (b) False case

The third loop is demonstrated in Figure 5.15. Part E is responsible for checking the synchronising register. If the register value is ‘False’, all the gate signals are ‘False’. Otherwise, the flat sequence (part F) is run with a period of 2 µs. The carrier waveform, AC references, arm currents and submodules’ voltages are transferred to this part by

the registers and the logics introduced in chapter 4 are implemented. The blocks shown in Figure 5.15 are identical for all the phases and arms.

In section G, the fault flags transferred from the second loop are checked. In the case of a fault, all the gate signals become ‘False’ to protect the converter. Otherwise, the gate signals are sent to the DO channels after applying rising edge delays [30], which creates dead time between the signals.

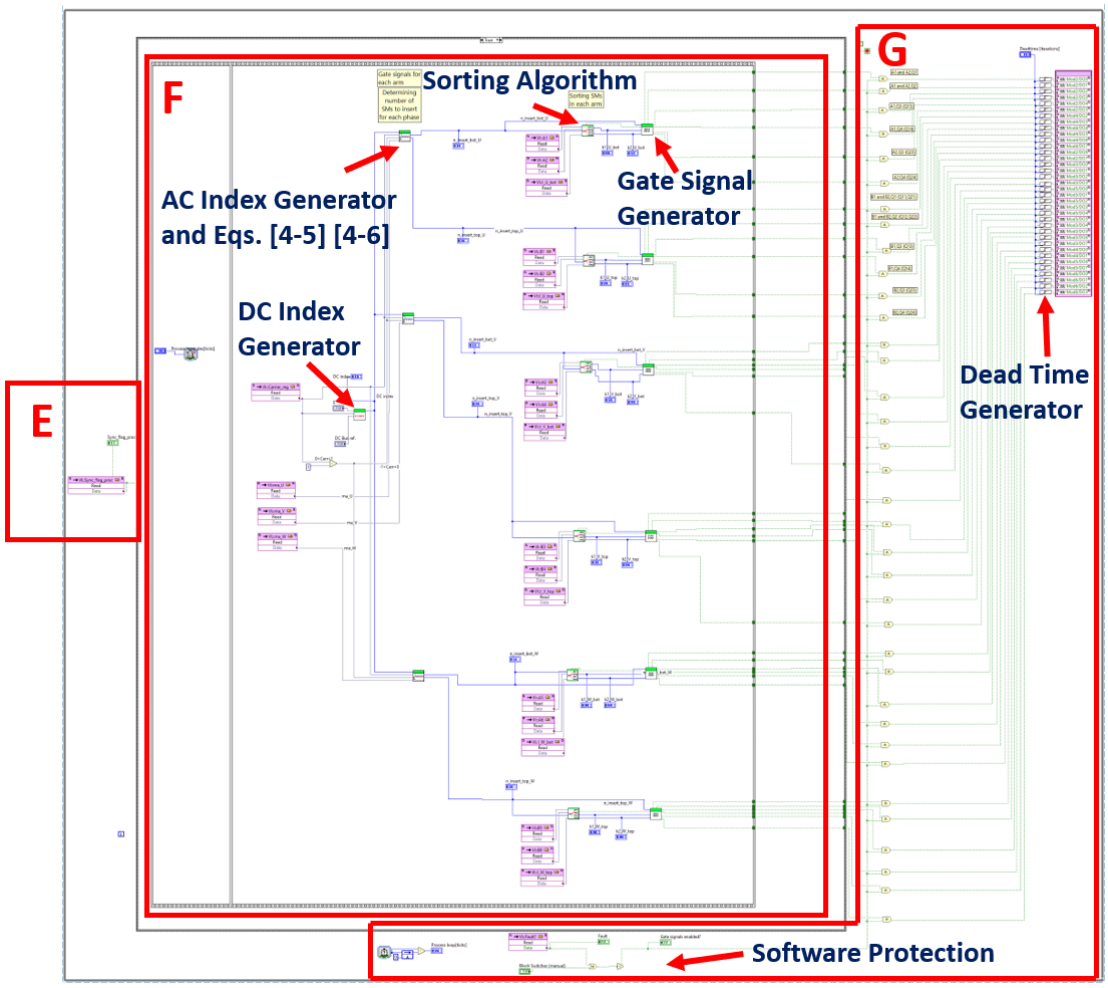


Figure 5.15 - The third loop - FPGA program

In addition to these main loops, there are two other loops in the FPGA program which drive the contactors, disconnect the converter’s contactor if there is a fault and send the selected signals to the AO channels for monitoring purposes. Moreover, for emulating

the DC side short-circuit, a DC short-circuit current controller (explained in section 3.3.4) has been added to the second loop of the FPGA program.

5.2.2 RT target program

The RT target is used to provide an interface between the user and FPGA program. As shown in Figure 5.16, the RT program opens a reference to the FPGA program, resets and runs it. Therefore, the user can set the controls (inputs) and monitor indicators (outputs) of the FPGA program via the RT program front panel (Figure 5.17). The RT program also reads the FIFO element dedicated to the submodules' voltages and shows the voltages on the waveform charts. At the end, the RT program aborts the FPGA program and closes the opened reference.

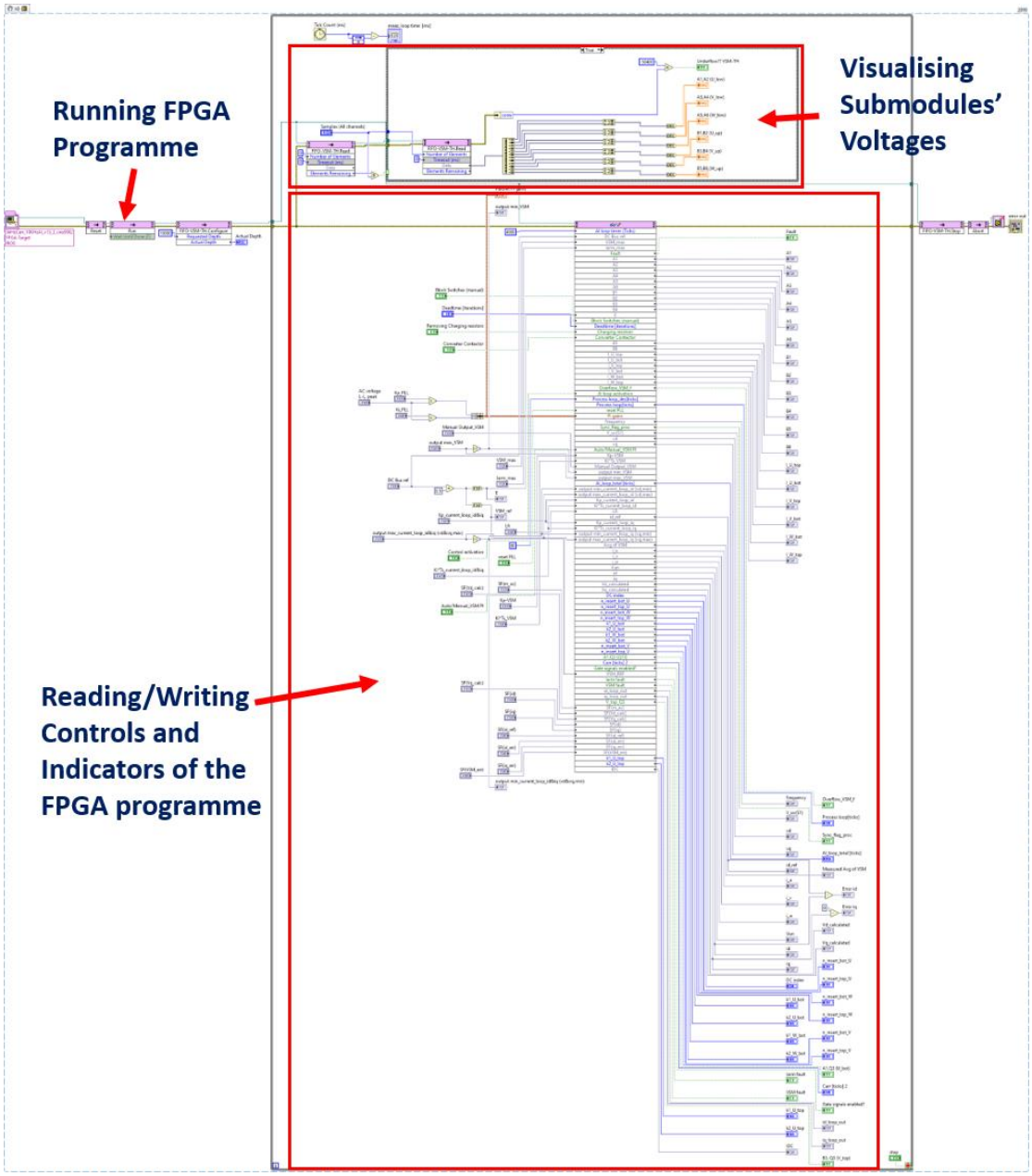


Figure 5.16 - Block diagram of the RT program

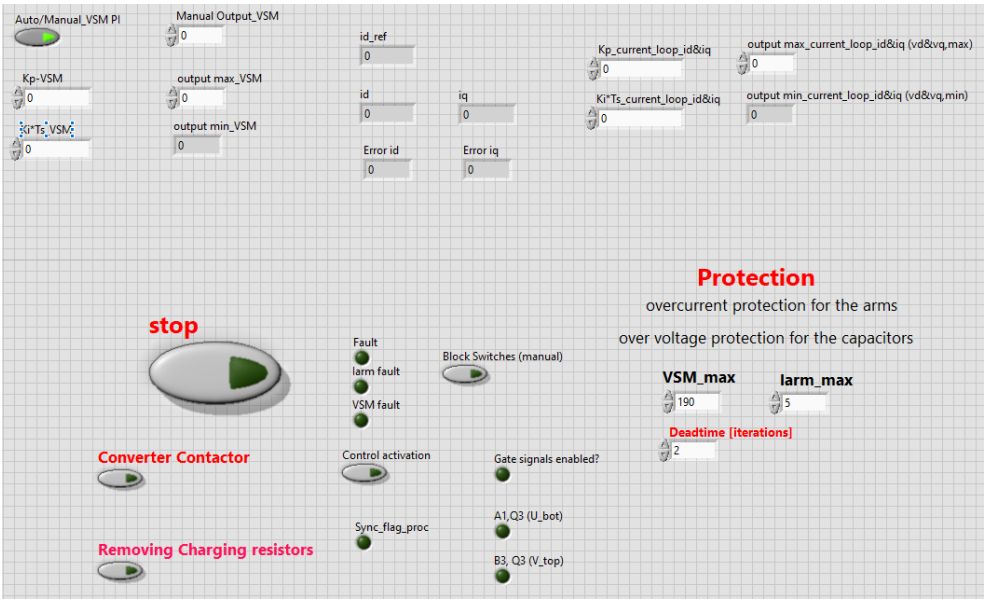


Figure 5.17 - Front panel of the RT program

5.3 MMC-FB operation

The capacitors of the MMC-FB need to be charged to the nominal value before normal operation. To limit the capacitor charging currents, the charging resistors are inserted into the circuit, and the peak of the line-to-line voltage on the converter side is adjusted to 30 V using the autotransformer. The converter is then connected to the AC side by the converter's contactor. When the capacitors are charged, the charging resistors are bypassed by the dedicated contactor and the controller is activated. The variable 'DC bus reference' ($V_{DC,REF}$) in the RT program is then used to control the capacitor voltage reference and variable 'E' (to change the amplitude of the carriers, refer to section 3.3.3), where:

$$E = \frac{V_{DC,REF}}{N_{sub}} = \frac{\text{DC bus reference}}{2} \tag{5-1}$$

$$Capacitor\ voltage\ reference = \frac{V_{DC,REF}}{N_{sub}} = \frac{V_{DC,REF}}{2} \tag{5-2}$$

In the first step, $V_{DC,REF}$ is gradually increased from 35 V to 70 V. Similar to this step, the AC-side voltage and $V_{DC,REF}$ are increased according to Table 5.2. In the final step, the variable 'E' and the capacitor voltage reference reach to their final value, i.e., 175 V, and the converter is ready to be connected to the DC load. Figure 5.18 demonstrates the start-up and shut-down procedures. The controller gains used in the charging phase, normal operation and DC fault emulation are presented in Appendix E.

Table 5.2 – AC-side voltage and $V_{DC,REF}$ in MMC-FB charging phase

Step no.	**Peak of the line-to-line voltage on the converter side (V)**	**Maximum value for $V_{DC,REF}$ (V)**
1	30	70
2	60	140
3	120	225
4	200	320
5	240	350

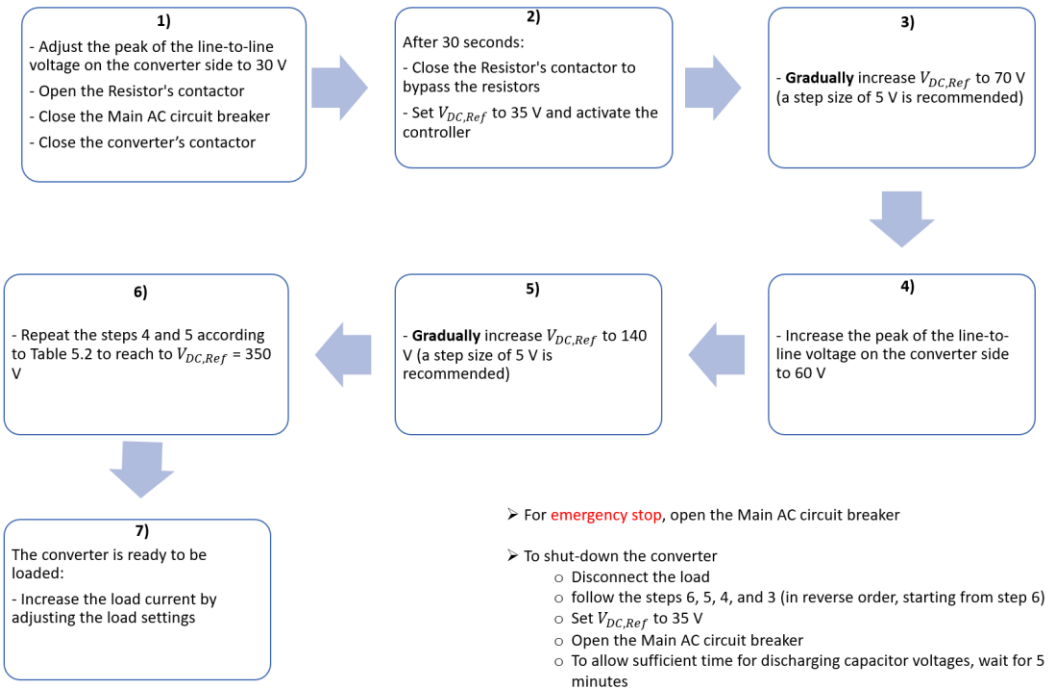


Figure 5.18 - The procedure for start-up and shut-down of the experimental setup

5.4 Summary

The aim of this chapter was to present the small-scale experimental setup of an individual MVDC TPS. The setup mainly consists of an autotransformer, line inductors, an MMC-FB prototype and a DC electronic load. On the AC side, the autotransformer is connected to a 415 V three-phase network and step downs the voltage to 170 V on the converter side. The MMC-FB prototype has two submodules per arm and provides 350 V on the DC side. The NI cRIO-9082 controller has been selected to realise the converter controller unit and the control algorithm introduced in the previous chapters has been implemented in NI cRIO-9082. In this chapter, the hardware design of the experimental setup is described in detail and the FPGA and RT codes deployed on the controller are explained. At the end, initialisation of the MMC-FB and charging of the converter's capacitors are discussed.

6 EXPERIMENTAL RESULTS

This chapter deals with the experimental results from the small-scale MVDC TPS lab demonstrator. The experiments were performed in the nominal conditions presented in Table 6.1. All the results were exported from an oscilloscope in comma-separated values (CSV) format and plotted using Matlab. Although the TPS has been tested in various DC load conditions, only the results for no-load, half-load and full-load conditions are described in this chapter. To analyse the dynamic performance of the MMC-FB and its controller, the TPS was also tested during DC load changes. Finally, the results for a DC short-circuit test are described.

Table 6.1 - Experimental conditions

Parameter	Value
AC voltage (network side)	415 V
AC voltage (converter side)	170 V
DC bus reference ($V_{DC,REF}$)	350 V
Modulation index	0.8
Nominal voltage of the capacitor in each submodule	175 V
Carrier frequency	5 kHz

6.1 Performance analysis in constant DC load

6.1.1 No-load condition (I_{DC} = 0)

To investigate proper functionality of the controller, the AC references produced in the first loop of the FPGA program were monitored by AO channels. The AC references, shown in Figure 6.1, are balanced sinusoidal-like waveforms with an amplitude of 0.8 V. As expected, this value is the same as the selected modulation index. Moreover, the voltage of phase ‘a’ on the autotransformer output (converter side) is shown in Figure 6.1. The AC reference produced for phase ‘a’ is in phase with the measured

phase voltage, indicating that the controller is properly synchronised with the network's voltages.

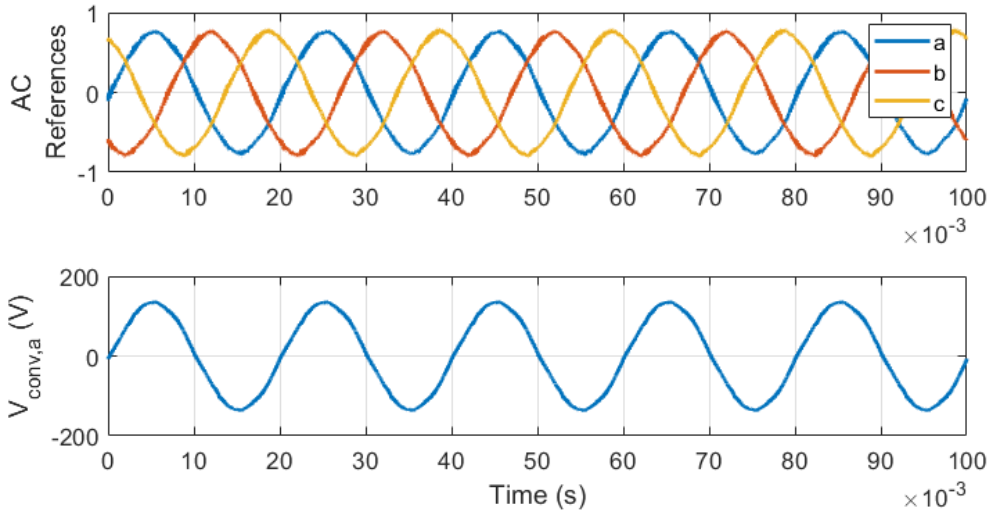


Figure 6.1 - AC references and voltage of phase 'a' on the converter side - I_{DC} = 0

The voltage of the DC bus is presented in Figure 6.2. The average voltage is 340 V, as the controller indirectly adjusts the DC bus voltage by regulating the capacitors' voltages. In other words, the voltage drops on the IGBT–diode modules and arm inductors are not considered by the controller. These voltage drops can be compensated by increasing $V_{DC,REF}$. In all the experiments presented in this chapter, however, $V_{DC,REF}$ has not been changed.

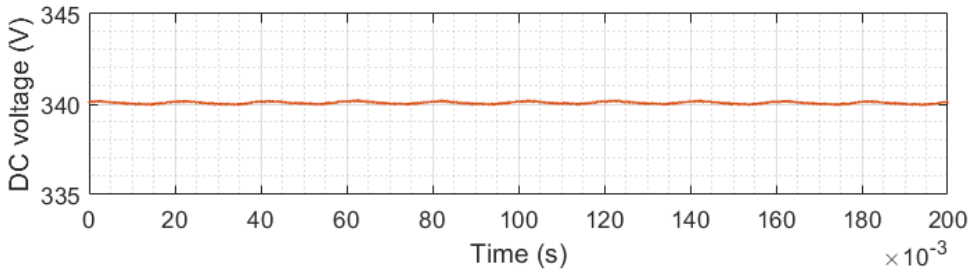


Figure 6.2 - DC bus voltage - I_{DC} = 0

6.1.2 Half-load condition (I_{DC} = 0.5 A)

In the experiments reported in this subsection, the electronic load was set in constant current mode to draw 0.5 A. The DC voltage and current are illustrated in Figure 6.3. As a result of loading, the DC voltage is slightly decreased. Although larger ripples can be seen in the DC voltage, their amplitude is negligible.

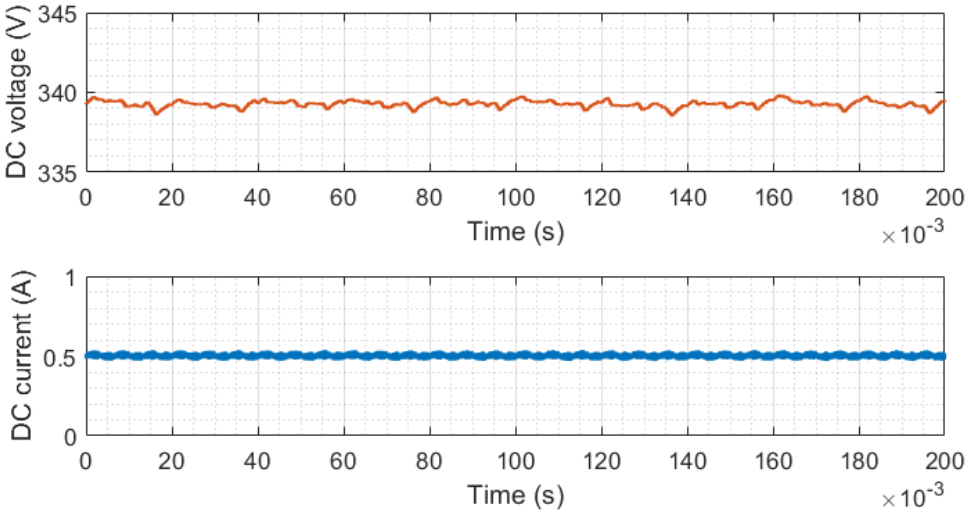


Figure 6.3 - DC voltage and current - I_{DC} = 0.5 A

To investigate the performance of the outer control loop, the capacitor voltages for both submodules in the top arm of phase 'a' are shown in Figure 6.4. The voltages are regulated and balanced, and their average values are slightly less than the setpoint. A DC offset is seen between the voltages, which could be due to errors and differences in the measurement circuitries of the submodules. In addition, the voltage probes used for measuring voltages are not completely identical, and this can cause a DC offset. The capacitor voltages of the first submodule in all arms of the converter (Figure 6.5) also illustrate that the outer controller loop can regulate the voltages close to the setpoint with relatively small voltage ripples.

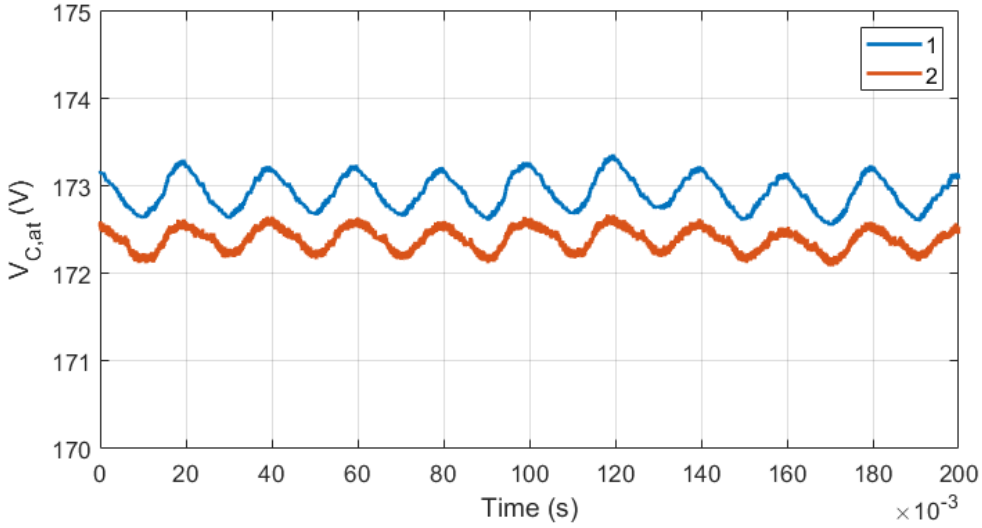


Figure 6.4 - Capacitor voltages in the top arm of phase 'a' of the MMC-FB - I_{DC} = 0.5 A

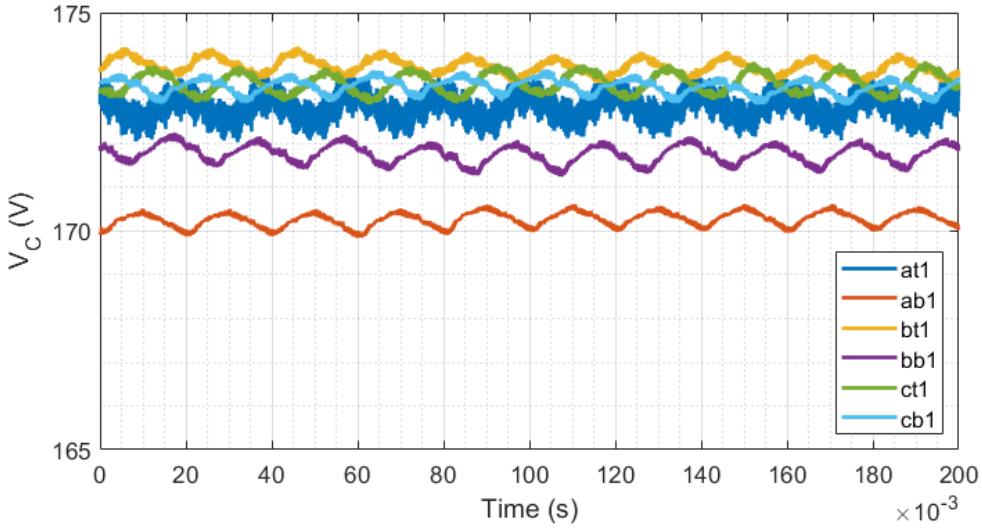


Figure 6.5 - Capacitor voltages of the first submodule in each arm of the MMC-FB - I_{DC} = 0.5 A

Figure 6.6 depicts the balanced phase currents on the converter side. As indicated for phase 'a', the currents are almost in phase with their corresponding phase voltages and the reactive power consumption is controlled on the converter side. Due to the fact that the converter is realised by only two submodules per arm, the phase currents are not purely sinusoidal. Figure 6.7 represents Fast Fourier Transform (FFT) analysis of the current in phase 'a'. After the fundamental component, the fifth, third and second

harmonic components have the highest amplitudes, respectively. Their amplitudes, however, are relatively small. To evaluate the harmonic distortion of the phase current, the Total Harmonic distortion (THD) of the current has been calculated as follows:

$$THD\% = \frac{\sqrt{\sum_{n=2}^{10} {V_n}^2}}{{V_1}^2} \times 100 \tag{6-1}$$

where V_n is the amplitude of the nth harmonic component. The THD for the phase current is 7.3%, which can be decreased by increasing the number of submodules in each arm of the converter.

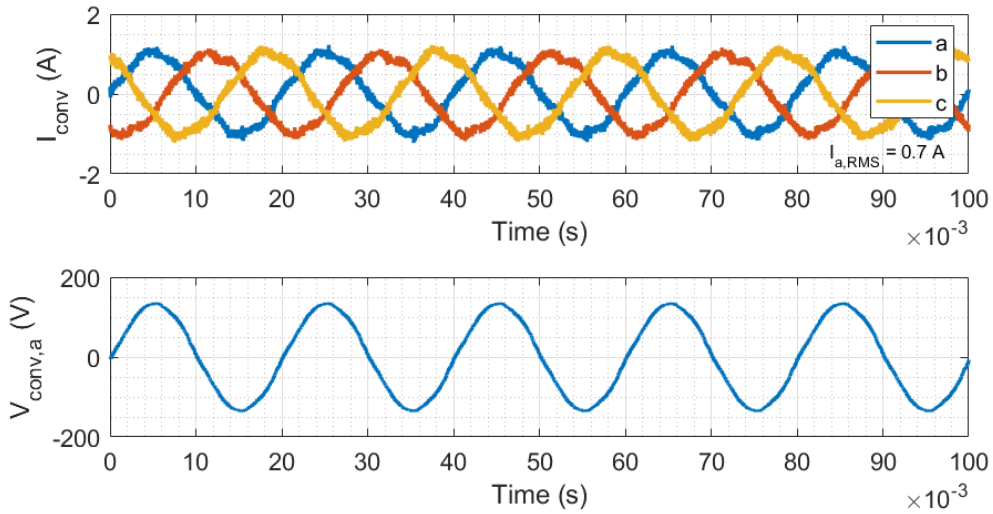


Figure 6.6 - Phase currents and voltage of phase 'a' on the converter side - I_{DC} = 0.5 A

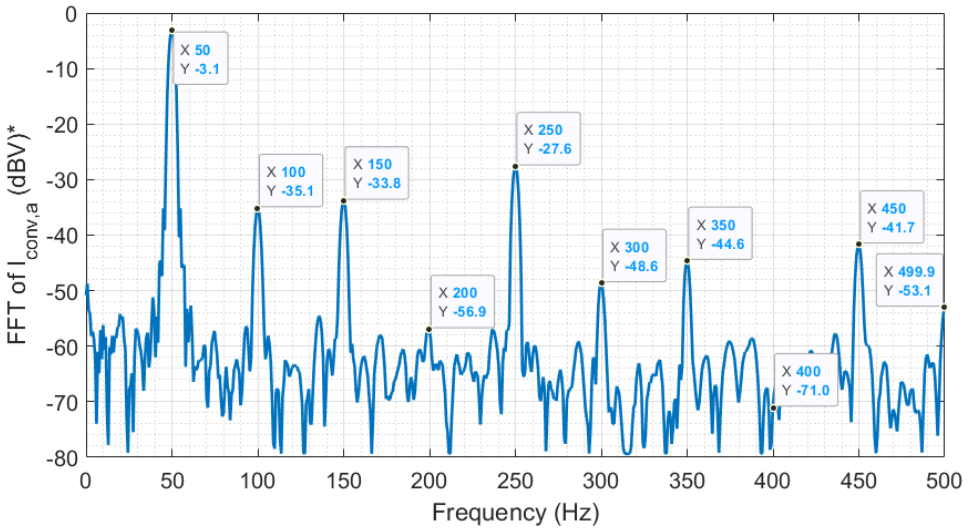


Figure 6.7 - FFT analysis of the phase current (phase 'a') on the converter side - I_{DC} = 0.5 A
** Based on the settings chosen for the oscilloscope, 1 V on the oscilloscope represents 1 A in the circuit.*

The voltage of the bottom arm of phase 'a' in the MMC-FB is presented in Figure 6.8. The arm voltage mimics the sinusoidal AC reference with three levels. To create the DC bus, the average of arm voltage is approximately half of the DC bus voltage. Figure 6.8 also depicts the voltage of phase 'a' on the converter side, showing that the bottom arm voltage is properly synchronised with the phase voltage. Moreover, Figure 6.9 illustrates the top and bottom arm voltages in phase 'a', which are 180° out of phase and balanced.

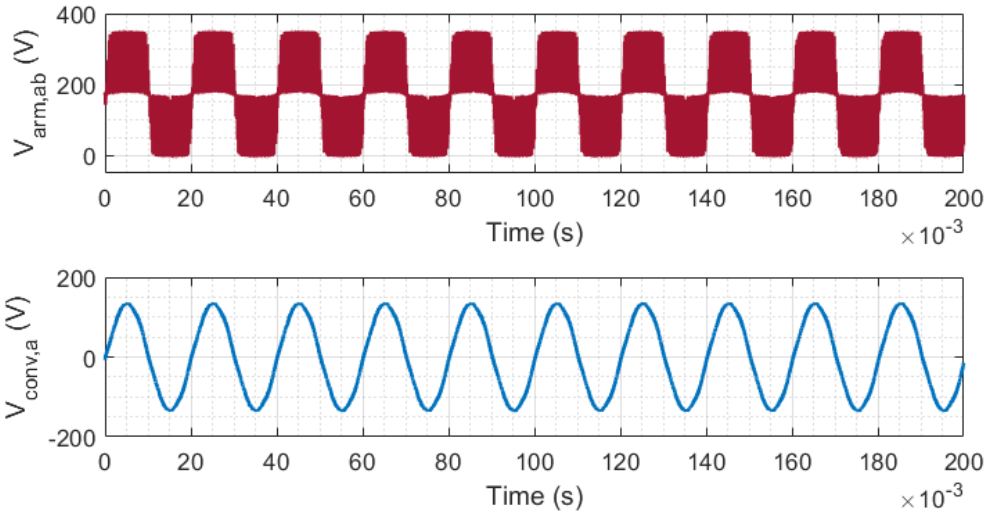


Figure 6.8 - Voltage of the bottom arm in phase 'a' of the MMC-FB and voltage of phase 'a' on the converter side - I_{DC} = 0.5 A

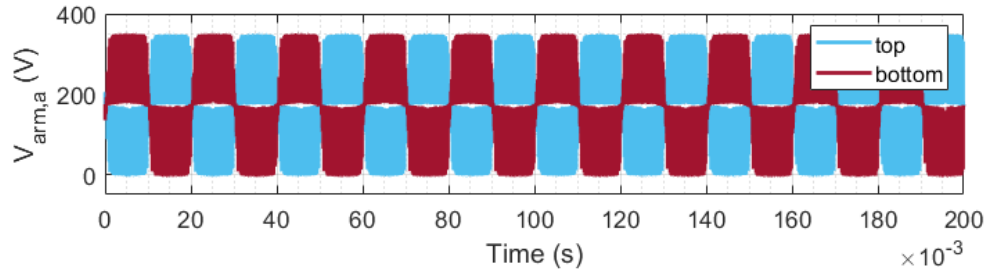


Figure 6.9 - Voltage of the top and bottom arms in phase 'a' of the MMC-FB - I_{DC} = 0.5 A

As shown in Figure 6.10, the voltage drop on the arm inductor in phase 'a' lies within the range −5 to +5 V, which is not considerable in comparison to the arm voltages. The top arm current is in phase with the top arm voltage, as the load is purely resistive.

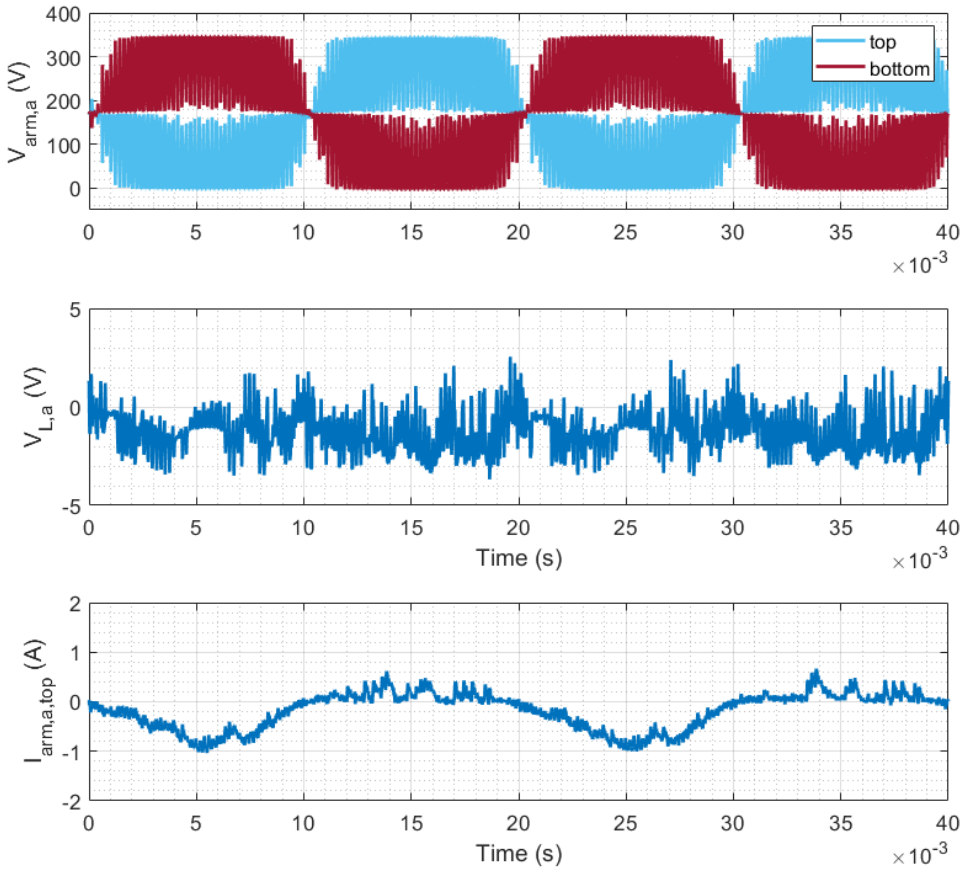


Figure 6.10 - The arm voltages, arm inductor voltage and top arm current in phase 'a' of the MMC-FB - I_{DC} = 0.5 A

The top and bottom arm currents in phase 'a' together with the arm voltages are presented in Figure 6.11. The arm current waveforms are similar and there is a 180° phase difference between the two currents. The top arm current, for instance, has a negative DC offset of −0.2 A and minimum of −1 A. The FFT analysis of the top arm current, shown in Figure 6.12, indicates that the arm current mainly contains the fundamental and second harmonic components.

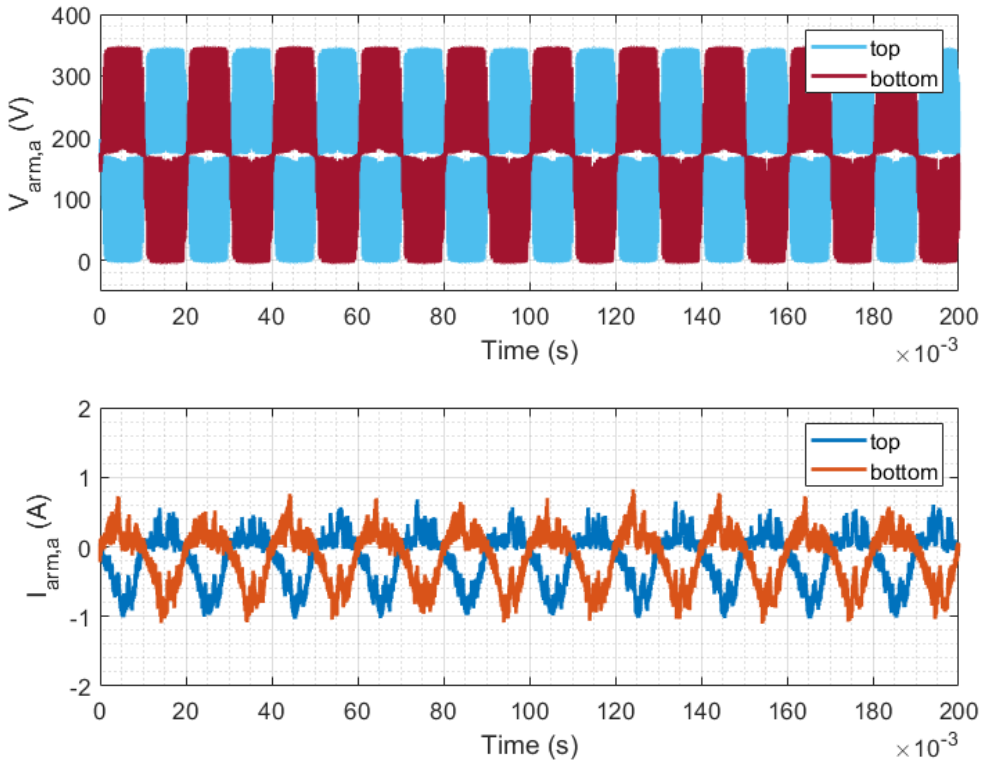


Figure 6.11 - The arm voltages and currents in phase 'a' of the MMC-FB - I_{DC} = 0.5 A

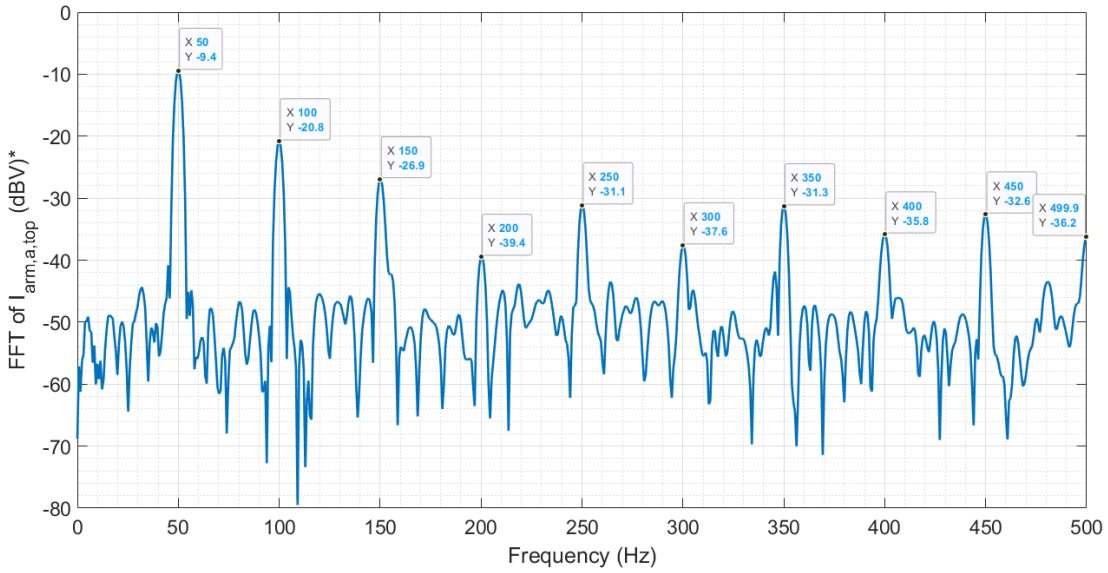


Figure 6.12 – FFT analysis of the top arm current in phase 'a' of the MMC-FB - I_{DC} = 0.5 A
** Based on the settings chosen for the oscilloscope, 1 V on the oscilloscope represents 1 A in the circuit.*

6.1.3 Full-load condition (I_{DC} = 1 A)

In this subsection, the performance of the TPS at the full load of 1 A is investigated. As depicted in Figure 6.13, the average of the DC bus voltage remains constant, and no significant voltage drop is seen in comparison to the half-load condition. The voltage ripples have increased slightly but their amplitude is still negligible.

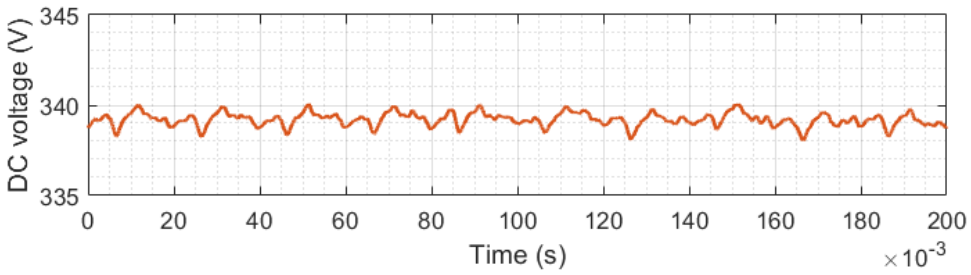


Figure 6.13 - DC bus voltage - I_{DC} = 1 A

The capacitor voltages in the top arm of phase ‘a’ are illustrated in Figure 6.14. In comparison to the half-load condition, the decrease in the average of the voltages is insignificant. Although the voltage ripples are larger, the voltages are smooth enough for proper MMC-FB operation on the DC and AC sides. Figure 6.15 presents the capacitor voltages in the first submodule of the MMC-FB arms, indicating that the outer control loop can regulate the voltages close to the nominal value with relatively small ripples.

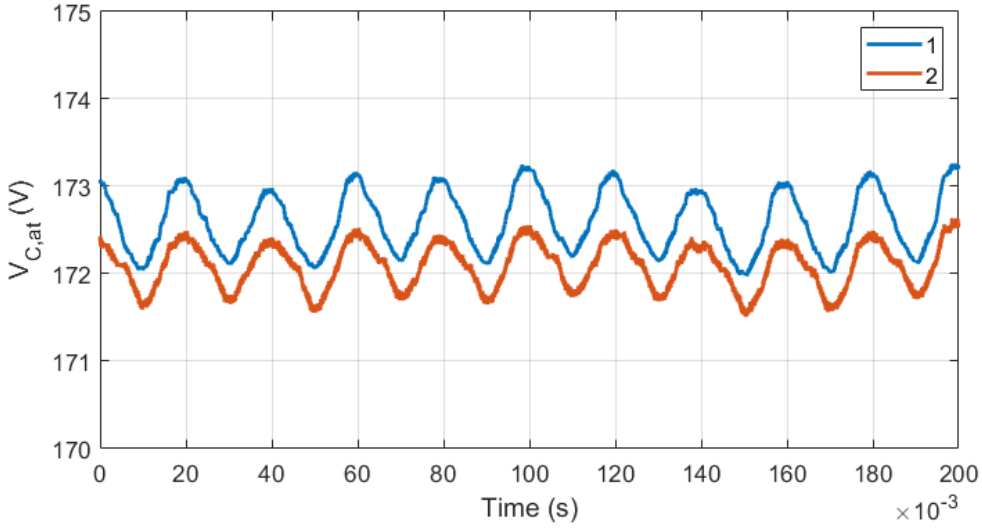


Figure 6.14 - Capacitor voltages in the top arm of phase 'a' of the MMC-FB - I_{DC} = 1 A

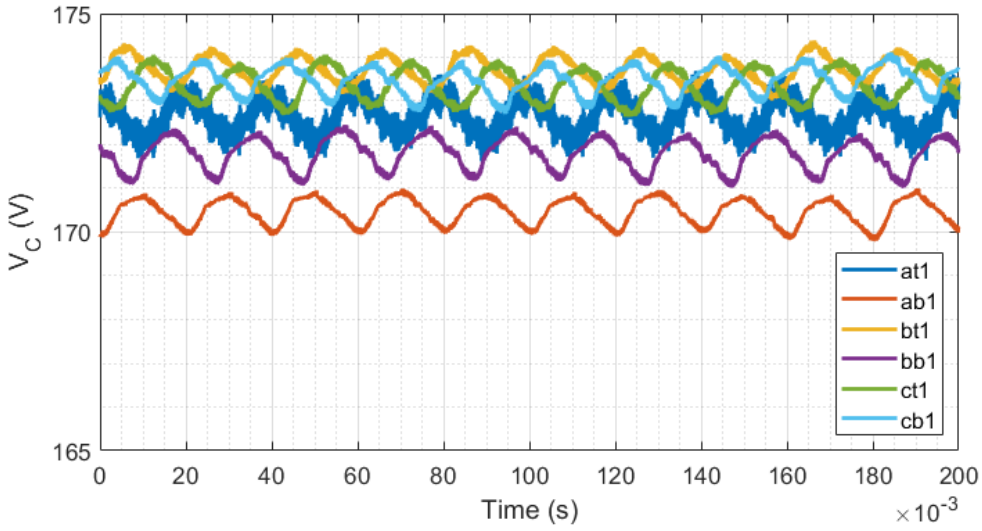


Figure 6.15 - Capacitor voltages of the first submodule in each arm of the MMC-FB - I_{DC} = 1 A

As depicted in Figure 6.16, the phase currents on the converter side are balanced. The shape of the currents is nearly sinusoidal with an RMS value of 1.4 A. The reactive power consumption in full load is almost zero, as the currents are in phase with their corresponding phase voltages.

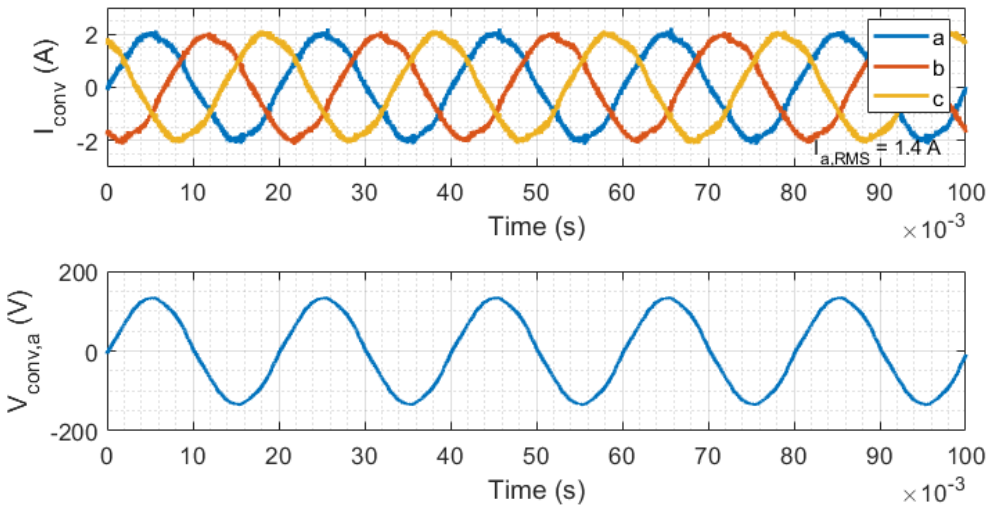


Figure 6.16 - Phase currents and voltage of phase 'a' on the converter side - I_{DC} = 1 A

6.2 Performance analysis for DC load change

6.2.1 Low-load to full-load condition

The results of testing the MVDC TPS and its converter during a load change are presented in this subsection. As an extreme case and to model a step load change, it is assumed that the TPS initially supplies a DC load of 0.2 A (low-load condition). The electronic load setting is then suddenly changed from 0.2 A to 1 A. The objective is to observe the dynamic performance of the MMC-FB and its controller. The rest of operating conditions in this subsection are the same as those shown in Table 6.1.

Figure 6.17 presents the trace of i_{dref}, i_d and i_q during the transient. The reference for i_d is updated and settled in less than 1 second. As a result of action of the inner control loops, the variable i_d follows the reference with a small steady state error. This is also the case for i_q, as the reference for i_q is zero.

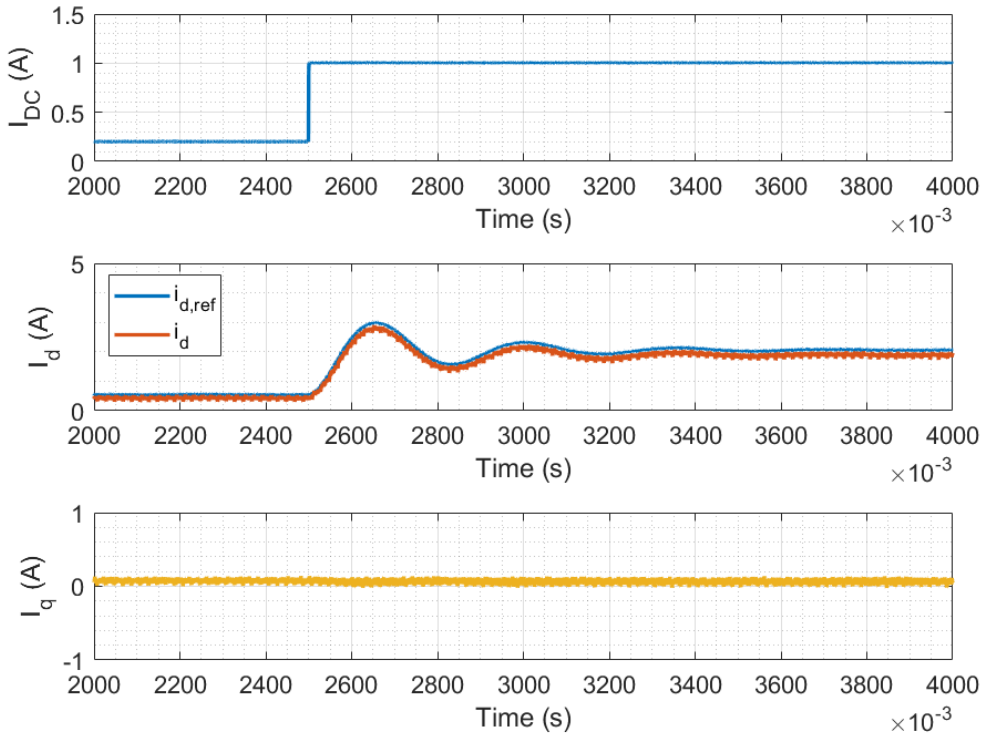


Figure 6.17 - DC current, i_d and i_q during the load change from 0.2 A to 1 A

As depicted in Figure 6.18, there is a voltage drop followed by a relatively small overshoot in the DC-side voltage. The DC voltage is then restored to the nominal value. Considering the phase 'a' current, there is an increase in the current to a peak of 3 A and then the peak current is decreased to 1.5 A. In the steady state, the peak of the current is fixed at 2 A. The top arm current of phase 'a' follows the same pattern as the phase current, with a minimum of −2.6 A during the transient.

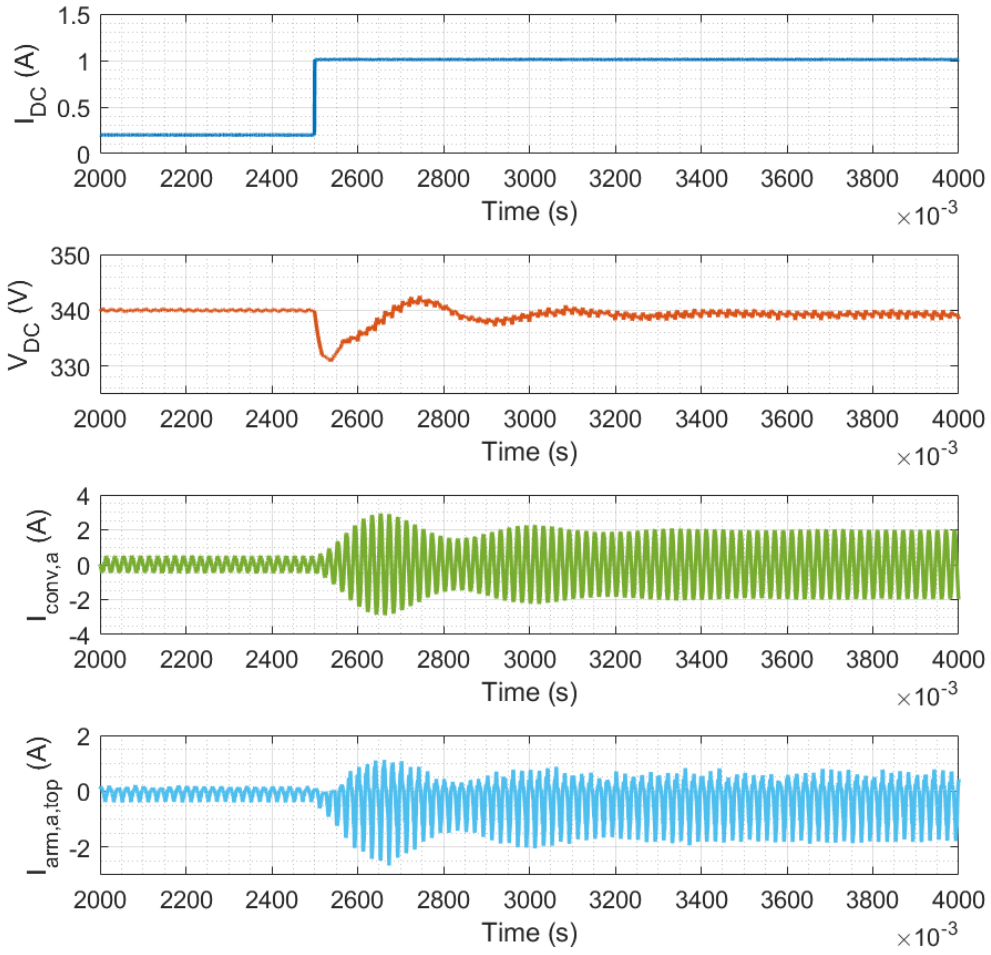


Figure 6.18 - DC voltage, current of phase 'a' on the converter side and top arm current in phase 'a' of the MMC-FB during the load change from 0.2 A to 1 A

The voltage of the capacitors in the top arm of phase 'a', shown in Figure 6.19, indicates that the voltages remain balanced during and after the step change. This is also the case for the first submodules of the arms, as illustrated in Figure 6.20. During the transient, there is a voltage drop followed by an overshoot in all the capacitor voltages. Nevertheless, the voltages remain sufficiently close to the setpoint. Overall, the converter remains stable when the load is suddenly increased and the phase currents, arm currents and capacitor voltages lie within the allowable limits defined in the

hardware design stage. Moreover, the change in DC voltage is not considerable and the TPS can seamlessly supply the load.

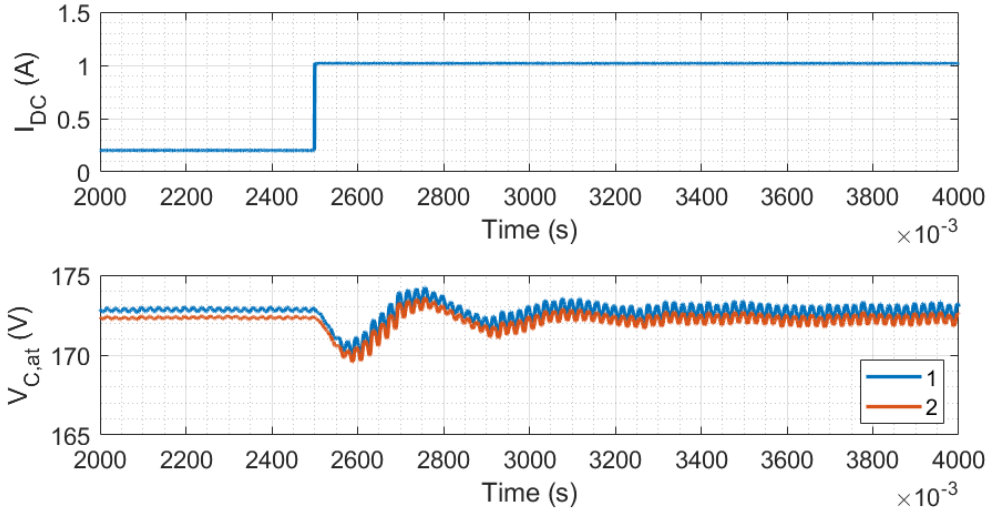


Figure 6.19 - Capacitor voltages in the top arm of phase 'a' of the MMC-FB during the load change from 0.2 A to 1 A

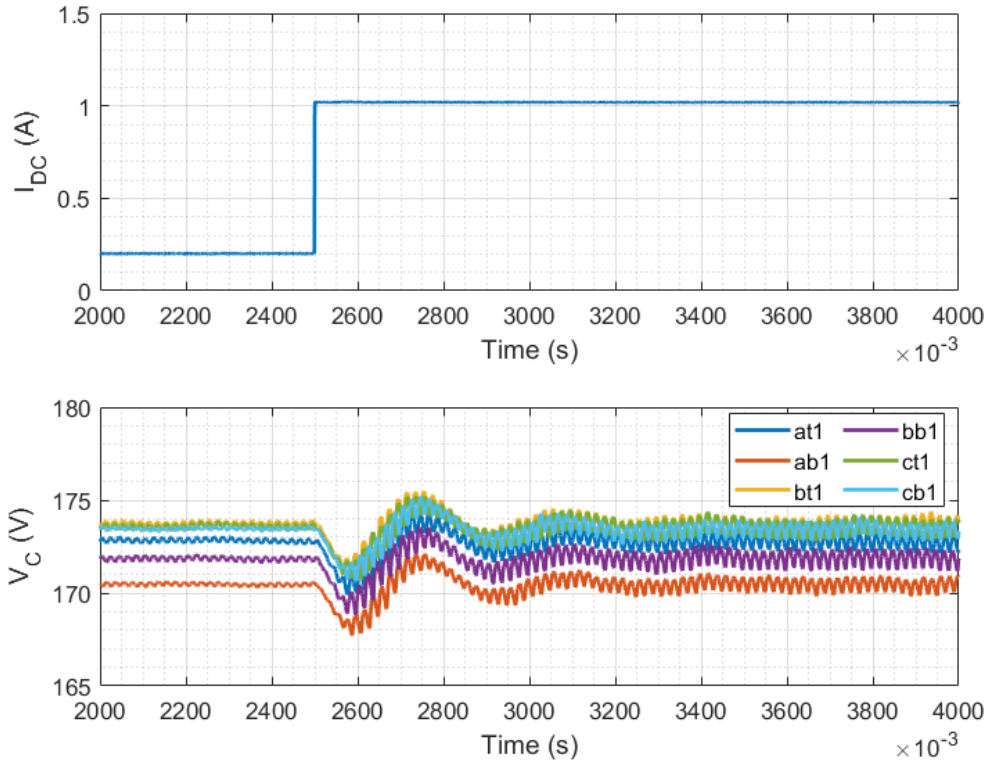


Figure 6.20 - Capacitor voltages of the first submodule in each arm of the MMC-FB during the load change from 0.2 A to 1 A

6.2.2 Full-load to low-load condition

In this subsection, it is assumed that the trains' load is suddenly decreased from a full load of 1 A to 0.2 A. As shown in Figure 6.21, the inner control loops can follow the load change. Similar to the previous subsection, i_d and i_q follow the references while there is a small steady state error for both of them.

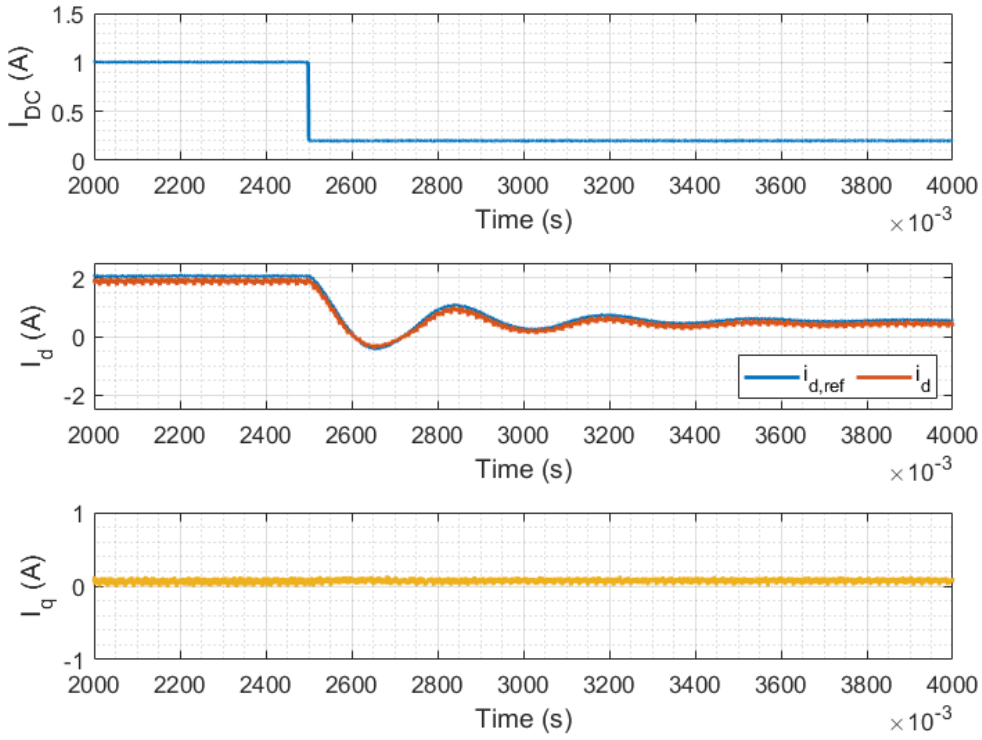


Figure 6.21 - DC current, i_d and i_q during the load change from 1 A to 0.2 A

As a result of decreasing the load, there is an overshoot followed by a voltage drop in the DC voltage. The DC voltage is then regulated at 340 V after the fluctuations, as depicted in Figure 6.22. This figure also illustrates the traces for the phase current and top arm current in phase 'a', confirming that the converter remains stable during the transient.

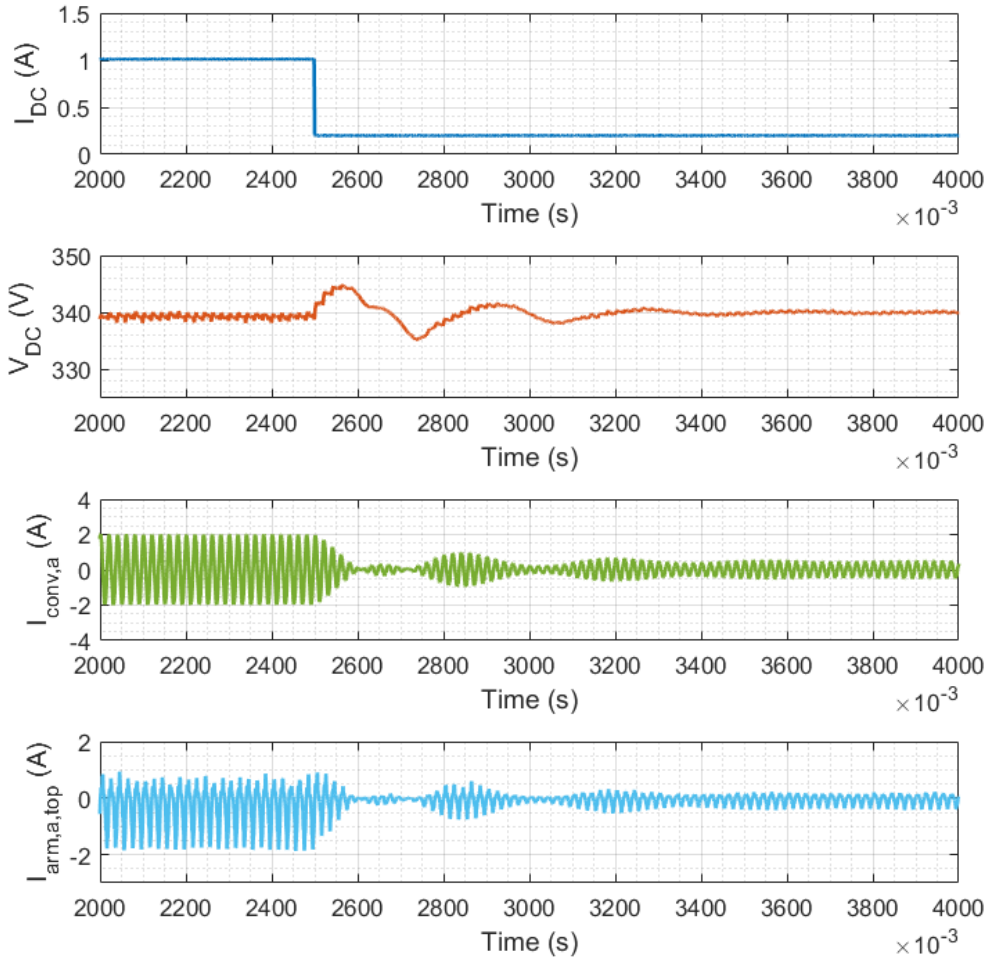


Figure 6.22 - DC voltage, current of phase 'a' on the converter side and top arm current in phase 'a' of the MMC-FB during the load change from 1 A to 0.2 A

The capacitor voltages in the top arm of phase 'a' (Figure 6.23) and the first submodules in all the MMC-FB arms (Figure 6.24) demonstrate quite the same results as those shown in the previous subsection. The only difference is that the voltages have experienced an increase in the first instances of the load change, which is due to a sudden decrease in active power consumption on the DC side.

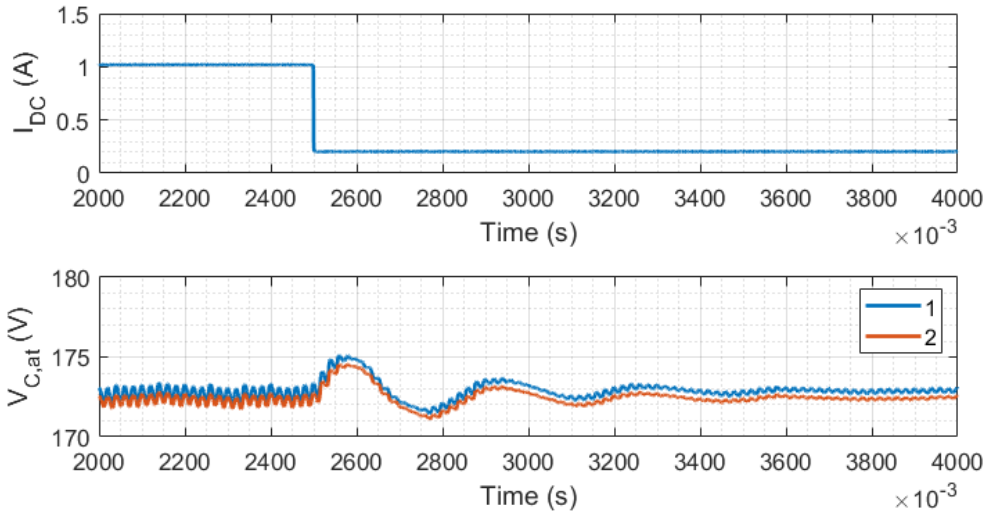


Figure 6.23 - Capacitor voltages in the top arm of phase 'a' of the MMC-FB during the load change from 1 A to 0.2 A

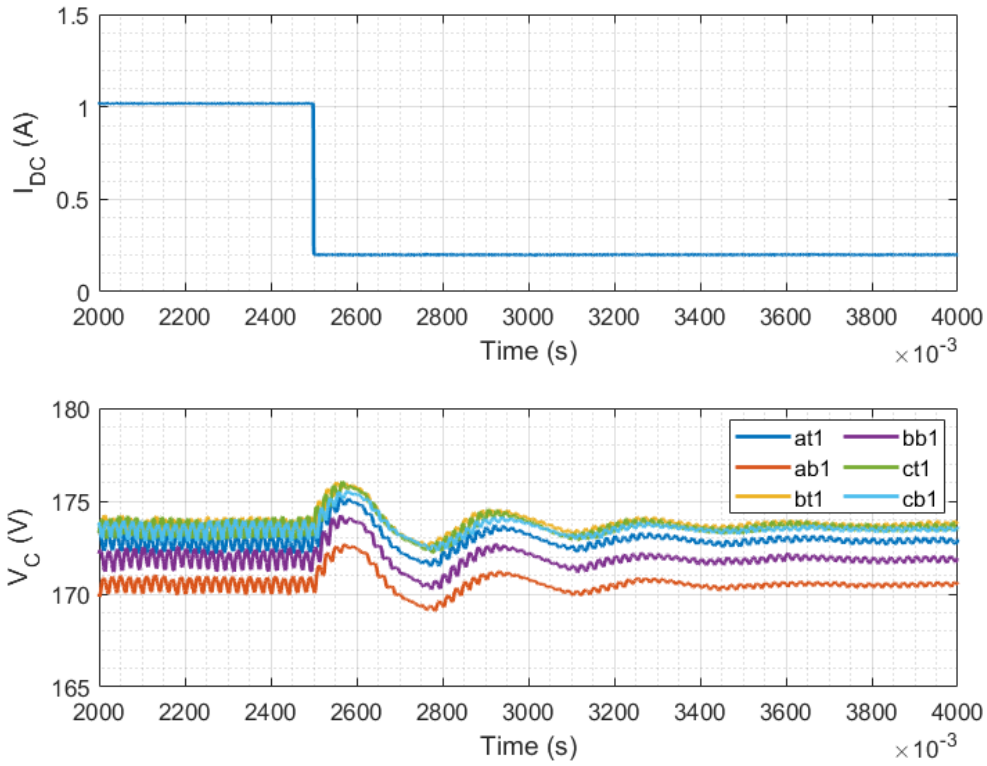


Figure 6.24 - Capacitor voltages in the top arm of phase 'a' of the MMC-FB during the load change from 1 A to 0.2 A

6.3 DC-side short-circuit test

In this section, the ability of the MMC-FB to limit DC short-circuit current is demonstrated. The nominal DC voltage in this experiment has been selected to be 100 V to protect the converter during the test. Therefore, the reference for capacitor voltages is 50 V. In addition, the voltage on the output of the autotransformer (converter side) is 42 V (equivalent to a modulation index of 0.7). Similar to the previous tests and because of the voltage drops on the IGBT–diode modules and the arm inductors, the converter provides a DC voltage with an average of 95 V.

The maximum allowable DC current is set to be 0.5 A through the front panel of the RT program. The DC electronic load has been set in constant resistance mode. Load setting ‘A’ has been set to draw 150 mA at 95 V (633 Ω), and load setting ‘B’ has been set to draw 960 mA at 95 V (99 Ω). To imitate a DC short-circuit, the load setting is suddenly changed from ‘A’ to ‘B’.

Figure 6.25 presents the DC current and arm voltages of phase ‘a’ in the MMC-FB during the DC short-circuit test. Due to the action of the short-circuit controller, the DC index is reduced and the averages of top and bottom arm voltages are decreased. These in turn cause a decrease in DC voltage. Consequently, the DC current is limited to 0.54 A. The steady state error of 0.04 A can be related to a DC offset in DC current measurement circuitry.

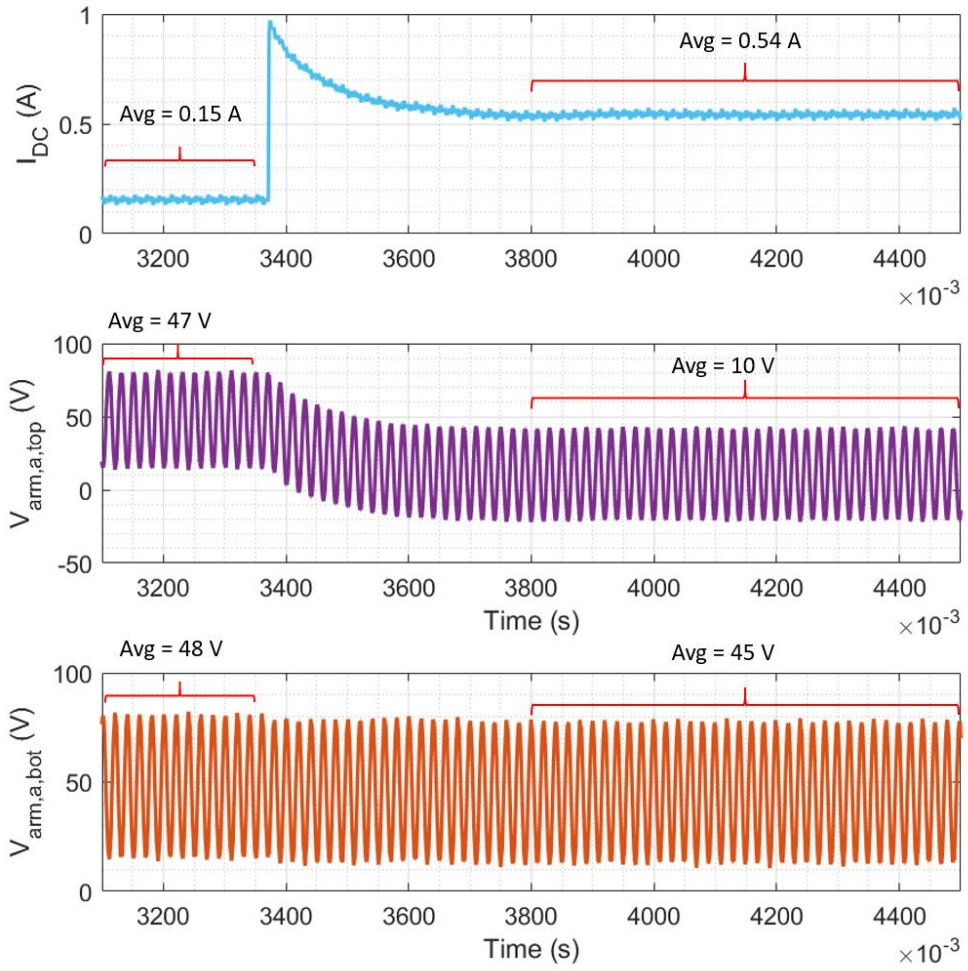


Figure 6.25 - DC current and arm voltages in phase 'a' of the MMC-FB - DC short-circuit imitation

To check the action of the short-circuit controller when the DC fault is cleared, the load setting is changed from 'B' to 'A'. As illustrated in Figure 6.26, the controller restores the arm voltages and DC current to the pre-fault situation.

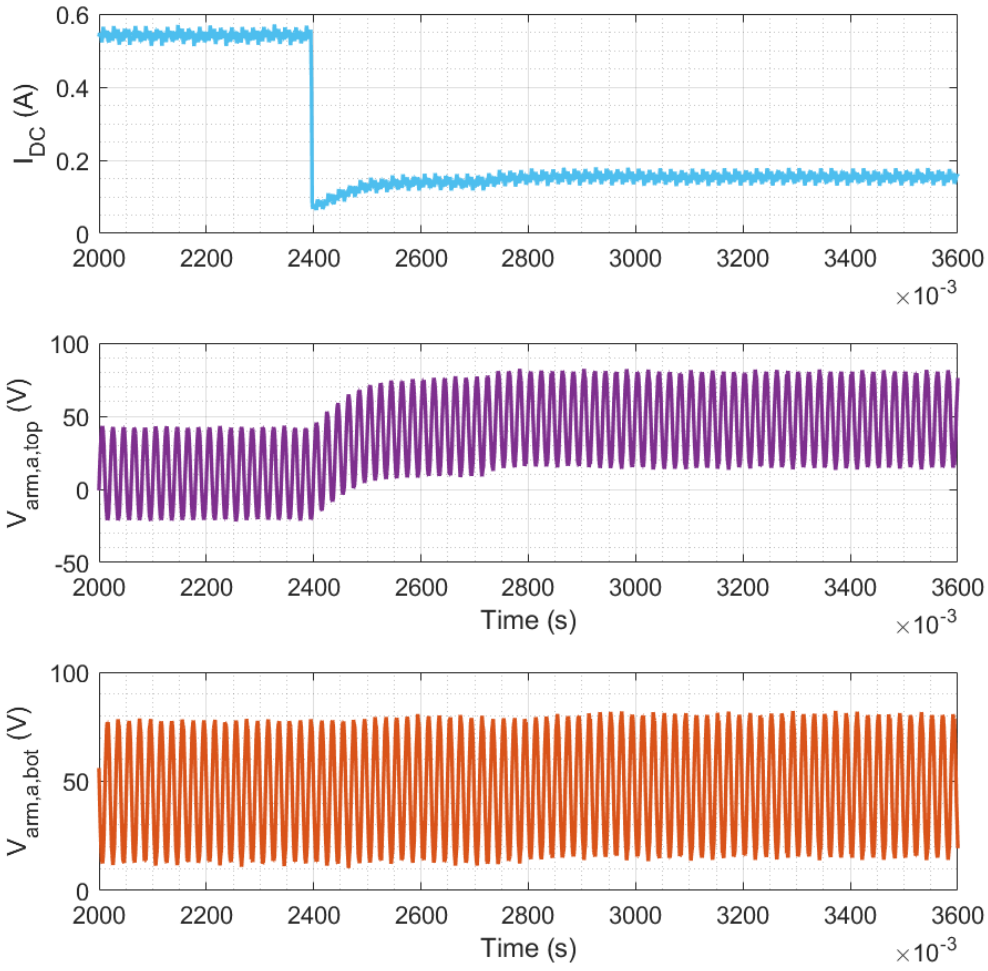


Figure 6.26 - DC current and arm voltages in phase 'a' of the MMC-FB - cleared short-circuit

Figure 6.27 demonstrates the DC voltage and top arm current of phase 'a' during the short-circuit. While the average of DC voltage is decreased to 55 V to limit the current, the arm current lies within the allowable limits defined for the hardware setup. In addition, the phase currents remain balanced and stable during the DC current limitation, as shown in Figure 6.28.

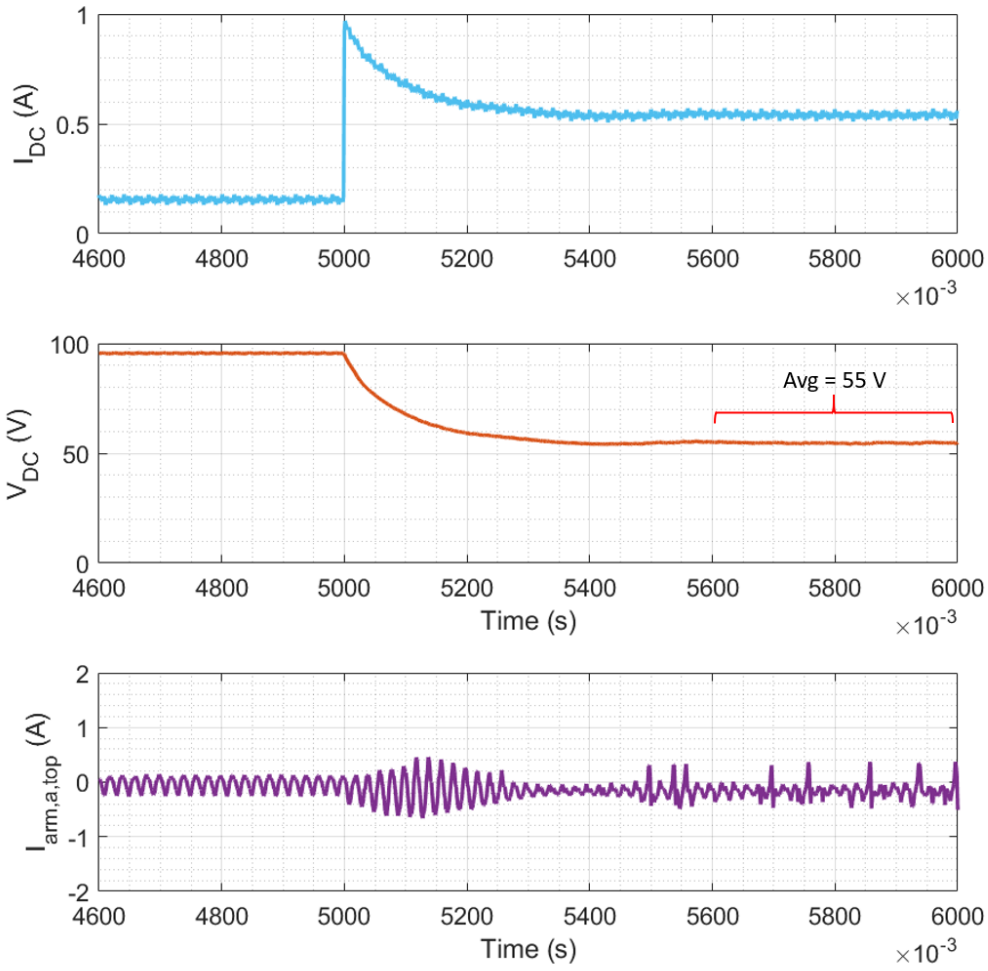


Figure 6.27 - DC current, DC voltage and top arm current in phase 'a' of the MMC-FB - DC short-circuit imitation

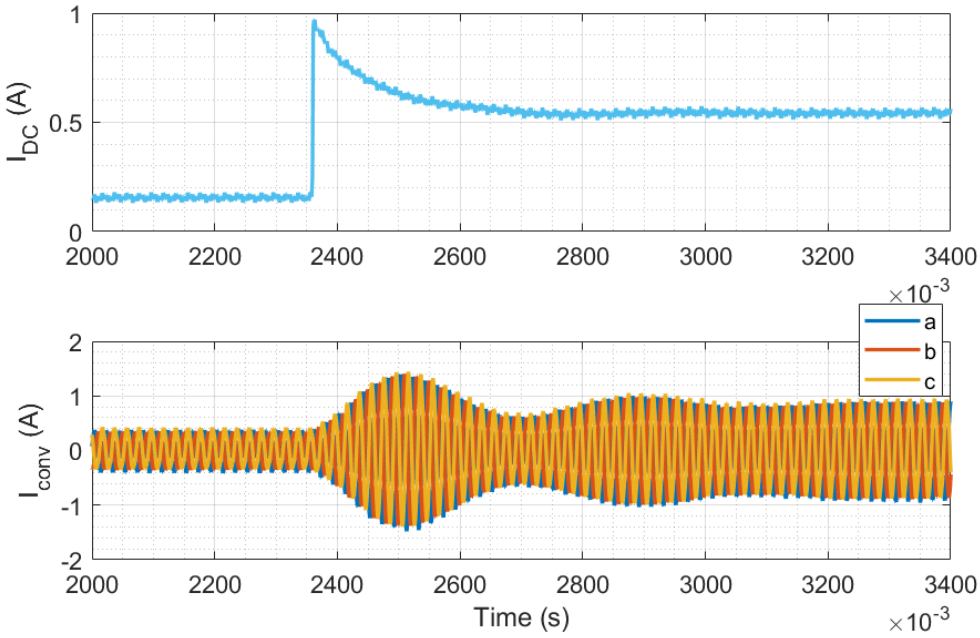


Figure 6.28 - DC current and phase currents on the converter side - DC short-circuit imitation

6.4 Summary

The aim of this chapter was to describe and analyse the results from the MVDC TPS experimental setup. The TPS setup was tested under no-load, half-load and full-load conditions. Then the TPS performance during a step change in DC load (full-load to low-load and vice versa) was investigated. The results confirmed the feasibility of the proposed controller and modulation scheme as the TPS was able to seamlessly supply the load in all the scenarios. In the final part of the chapter, the ability of the TPS converter to limit DC short-circuit current was shown. In the case of a DC overcurrent, the short-circuit controller decreases the average of the arm voltages and, thus, the DC-side voltage. This in turn leads to a decrease in the DC current. While the DC current is limited to the desired value, the phase and arm currents remain stable as the arm voltages are compatible with the AC-side phase voltages.

7 CONCLUSION AND FUTURE WORK

7.1 Conclusion

Mitigating the limitations of the AC and DC railway electrification systems, the MVDC railways are new solutions for the high-speed railways. These new systems have a wide range of advantages including simpler and cheaper connection to the AC distribution networks, possibility of creating DC microgrids and integrating renewable power sources, flexible control over the power transfers, less voltage drops, and simpler power supply diagram due to inexistence of the neutral sections. The review of feeding arrangements proposed for the MVDC railway electrification systems in the literature indicates that there are still technical barriers to realising MVDC railways in the railway industry.

This research has proposed an MVDC railway electrification system for high-speed lines. In the proposed MVDC electrification system, AC-DC power converters are installed in the MVDC TPSs to supply 25 kV DC overhead lines from widely available AC distribution networks. The allowable voltage ranges, power and current ratings of the MVDC TPSs, the parameters for the transformer of the TPSs, AC side cables and the MVDC overhead lines have been determined to model the MVDC railway in Matlab/Simulink.

The design of the power converters for the MVDC TPSs is a crucial task due to specific requirements of the MVDC railway networks. Based on reviewing high-power AC-DC converter topologies suitable for the medium-voltage applications, MMC-FB has been found to be a promising solution for the MVDC TPSs. Therefore, an MMC-FB with eight submodules per arm has been designed and modelled for the MVDC TPSs to complete the MVDC railway model.

In addition, a control scheme for the MMC-FB has been developed in a dq frame synchronised with the distribution network. In this scheme, the outer control loop in the d axis regulates the average of the capacitor voltages to the reference value (3.13 kV), while the outer loop in q axis controls the reactive power consumption on the primary side of the transformer (grid side). The inner control loops are responsible to regulate the phase currents transformed to the dq frame. The AC references produced by the control scheme are then passed to the proposed level-shifted carrier modulation algorithm. Using the AC index generator, DC index generator, sorting and gate signal generator blocks, the modulation stage provides proper gate signals for the IGBTs.

Moreover, the MMC-FB design and the proposed control and modulation units have been evaluated by the simulation models:

- An individual MVDC TPS simulation model has been analysed in normal operation under a rapid traction load change. The results indicate that the designed MMC-FB can provide a smooth and regulated DC voltage while the AC side currents are balanced and have low TDD. The capacitor voltages, arm voltages and currents remain stable and balanced, and the reactive power consumption is properly controlled to zero on the AC network side. The simulation analysis during regenerative braking also confirms the proper functionality of the converter and its controller in delivering the regenerated power to the AC distribution network.
- As an abnormal operating condition, the MVDC TPS model has been tested during a non-permanent voltage dip on the AC side. Although during the incident, the ripples of the capacitor voltages slightly increase, the DC-side voltage remains regulated around the nominal value and the TPS can normally supply the load.

- The short circuit current controller has been also tested during a non-permanent DC short-circuit. As shown in Figure 4.21, the converter controller reduces the DC voltage, and thus, the average of DC current is limited to $I_{DC,max,fault}$. After clearance of the fault, the DC voltage experiences an overshoot with peak of 28.72 kV, which is smaller than allowable highest non-permanent voltage. The DC voltage is then become regulated to the nominal value of 25 kV and the MVDC TPS serves the railway load normally.
- The MMC-FB power losses under various load conditions (including regenerative braking condition) have been evaluated using a single TPS simulation model and the method presented in section 3.4. The MMC-FB efficiency curve (Figure 4.40) shows low efficiencies in light loading conditions. However, the converter efficiency improves by increasing the load consumption and reaches to a peak of 97.9% in the full load of 16 MW. The efficiency curve illustrates the same pattern for the MMC-FB efficiency when the converter operates in regenerative braking condition.
- The simulation model has been extended to a double-end feeding arrangement, where there are two MVDC TPSs at the two ends of the feeding system. To investigate the effects of renewable energy sources on the MVDC railway network, a 1.6 MW PV farm has been added to the simulated network at TPS 1. The analysis reveals that the MMC-FBs in both TPS 1 and TPS 2 operate properly and after the transient related to connection of the PV farm, the voltages lie within the acceptable range for the MVDC railway system. In particular, the average voltage across the load is 24.6 kV (0.98 pu). This is also the case when the installed capacity of the PV farm is increased to 8 MW, where

the MVDC TPSs successfully inject the excess produced power to the AC distribution network.

- The performance of the double-end fed MVDC railway has been also analysed when the load is equally shared between the two TPSs by implementing a centralised control strategy for the MVDC railway network. The results show that the network controller is able to adjust the power transfers and share the load, which can lead to decrease in the power ratings of the TPSs. Due to considerable power transfer from a distant TPS, however, there is a compromise between decreasing the power rating of the TPSs, and the total losses in the railway network.
- Using the TPSs as building blocks, a simulation model of an MVDC railway network with multiple TPSs has been developed. The simulation analysis confirms that the TPSs can normally supply the railway load and the voltages at the TPS terminals and across the loads are in the allowable limit defined for the MVDC railway network.

In the next step of the research and to examine the technical feasibility of the proposed control and modulation scheme on a hardware setup, a small-scale 350 W lab demonstrator of an individual MVDC TPS has been developed. The lab demonstrator mainly consists of a three-phase autotransformer, an MMC-FB prototype with two submodules per arm, and a DC electronic load. The lab demonstrator is connected to a 415 V three-phase AC network. On the DC side, the voltage set point for the MMC-FB protype is 350 V. NI cRIO-9082 has been selected for implementing the control, modulation and sorting algorithms. The codes have been mainly implemented on the FPGA board of the NI cRIO-9082, and

its RT target has been used to provide an interface between the user and FPGA program.

- Testing the TPS experimental setup under constant DC loads (no-load, half load, full-load) indicates the proper functionality of the MMC-FB. The capacitor voltages are regulated with relatively small ripples, the DC-side voltage is smooth, the AC-side currents are balanced, and the converter arm voltages are matched with the AC references produced by the controller.
- During a step change in the DC load, the PI controllers of the MMC-FB can follow the references with relatively small errors, and thus, the TPS is able to handle the rapid load change scenarios.
- Testing the TPS lab demonstrator in a DC short-circuit scenario reveals that the controller is able to limit the DC current while the converter remains stable. After clearing the fault, the controller restores the DC voltage to the normal value.

7.2 Future work

7.2.1 Research areas

Considering the benefits of the MVDC railway electrification systems, it is necessary to continue the research and facilitate their industrialisation. Although there are studies on stability analysis [31], [32], network control schemes [33]–[36], PETTs [37]–[40] and corrosion issues [41], [42] in the MVDC railways, there are areas which need to be investigated:

- Developing a real-scale test rig of a 25 kV DC railway system would help to further demonstrate the technical feasibility of the proposed system.

- The economic analysis of an MVDC railway system can show the potential cost savings and attract the railway industry to accept this new electrification system.
- The developed simulation models in this research can be further expanded and used to optimise the distance between the TPSs, implement more complex network control strategies, and simulate a DC microgrid with more power sources.
- An in-depth reliability analysis of the TPS power converters and their controller units will help the stakeholders to have a fair comparison between the traditional electrification systems and the MVDC system.
- New standards and regulations need to be developed for the MVDC electrification systems, so that MVDC railway lines in all countries can use the same design and rolling stocks.

7.2.2 Industrial implementation

In this study, the proposed MVDC railway electrification system has been designed and theoretically studied. Following this, the small-scale lab protype has been used to validate the core functionality and performance of the new electrification system. Similar to any new technology, the MVDC electrification system needs to be further developed and tested to be accepted by the railway industry.

The next step towards this can be validating the whole system in the lab environment, by connecting more MVDC TPS prototypes to a number of PETT lab prototypes. The system should then be tested and demonstrated in a relevant environment that closely represents operational conditions. This involves testing on a smaller-scale track or controlled section of a railway network to assess the performance, safety, and

interoperability. As the next step, the system is ready to be demonstrated in a real-world operational condition, including limited deployment on a specific route or section of a railway network. In this stage, necessary certifications and regulatory approvals can be obtained. This involves conducting environmental impact assessments and addressing any concerns related to noise, visual impact, or ecological considerations. After successful completion of the above stages, the system is ready for widespread implementation.

8 APPENDICES

8.1 Appendix A: The paper "Medium-voltage DC electric railway systems: A review on feeding arrangements and power converter topologies"

This appendix presents the published paper by the author of this PhD thesis and his colleagues in MVDC-ERS project:

Sharifi, S., et al.: Medium-voltage DC electric railway systems: A review on feeding arrangements and power converter topologies. IET Electr. Syst.Transp.12(4),223–237(2022).

Available online: https://doi.org/10.1049/els2.12054

© 2022 The Authors. IET Electrical Systems in Transportation published by John Wiley & Sons Ltd on behalf of The Institution of Engineering and Technology.

Licence: Creative Commons: Attribution (CC BY). In this appendix, the paper has been reformatted to single column style, the reference numbering has been changed, and section 6 (references) has been omitted.

Medium-Voltage DC Electric Railway Systems: a review on feeding arrangements and power converter topologies

Sina Sharifi [1*], Izsák Ferdinánd Ferencz [2], Tamer Kamel [1], Dorin Petreuș [2], Pietro Tricoli [1]

[1] Department of Electronic, Electrical and Systems Engineering, University of Birmingham, Edgbaston, Birmingham, United Kingdom

[2] Department of Applied Electronics, Technical University of Cluj-Napoca, Str. George Barițiu, No. 26, Cluj-Napoca, Romania

* sina.sharifi.90@gmail.com

Abstract: Medium-voltage DC (MVDC) electric railway systems have several advantages over conventional DC and AC railway electrification systems. These advantages include higher capacity, possibility of connecting to power networks at lower voltage, removal of neutral sections, smaller line voltage drops, and longer distances between traction power substations. This paper reviews in depth the arrangements for MVDC railway electrification systems proposed in the technical literature and the topologies used for high-power medium-voltage AC-DC converters. With reference to typical requirements of a MVDC railway electrification system, the pros and cons of the topologies are critically analysed. Moreover, this paper reviews the DC-DC power converter topologies for on-board power electronics traction transformers, required to interface the MVDC power supply with the traction motors. Finally, the review highlights the existing challenges of MVDC electric railway systems and the potential areas of future research.

1. Introduction

Medium-voltage DC (MVDC) electric railway systems have been widely proposed to address the typical limitations of conventional DC and AC railways. Unlike low-voltage DC (LVDC) railways, the spacing between traction power substations (TPSs) of MVDC railways can be much higher, thanks to the higher voltage level. Unlike AC railways, MVDC systems do not introduce imbalance on the AC utility grid [1] and, can be connected to the widely available power distribution grids at lower voltage levels via cheaper and simpler connections. There is less voltage drop and reactive power consumption, as a result of less reactance in the MVDC railway systems [6]. Due to lack of skin effect, the MVDC overhead lines can be realised with simpler cable and wire layout. In addition, MVDC TPSs can be easily paralleled, reducing their power rating [1], [7]. There is no need for neutral sections, so power transfer to the trains is

not interrupted. This means that the high-speed trains can maintain their speed [7]. MVDC TPSs can also be integrated into DC microgrids, facilitating the use of renewable power sources, energy storage systems and distributed generation units [1], [3].

The MVDC railways have not been implemented in industry yet, due to some technical challenges. For instance, the MVDC network should be controlled properly, avoiding undesired power circulation between TPSs. Protecting MVDC feeders against short circuit is another issue, as the DC circuit breakers are expensive and complicated [3]. Concerning the power converters used in TPSs and trains, the choice of topology is quite critical to ensure that energy efficiency and reliability are similar to components already in use, i.e. transformer-rectifiers for DC railways and transformers for AC railways.

There are various proposals for implementing MVDC railways, which can be classified into two major approaches: the use of MVDC intermediate feeders for feeding LVDC or medium-voltage AC (MVAC) overhead lines; or the use of MVDC overhead lines to directly feed the trains. Both approaches use AC-DC converters in TPSs to provide MVDC. In the first approach, the MVDC has mainly the objective of reducing transmission losses in comparison with conventional systems, while overhead lines and trains remain substantially unchanged. In the second approach, the trains use PETTs to reduce the voltage of the MVDC power supply to levels acceptable for the traction motors.

To the knowledge of the authors, there is no comprehensive review on the proposed schemes for MVDC railways. Therefore, the aim of this paper is to review technical solutions proposed for the MVDC railways, and discuss existing power converter

topologies to assess suitable options for MVDC TPSs and PETTs in a feeding system with MVDC overhead lines.

2. Technical solutions for MVDC railway systems

2.1. Systems with MVDC intermediate feeders

A three-wire electrification system has been proposed in [43] to reduce the voltage drop, minimise power losses and increase the capacity of existing LVDC TPSs. The concept is similar to the AC supply systems with autotransformers and is realised by installing a third wire for transferring the power at double the nominal voltage level, while the trains are supplied at nominal voltage. Fig.1 shows the case where additional rectifiers are installed between the rails and third wire, and the third wire voltage polarity is negative with respect to the rails. Besides, multilevel DC-DC converters are used every few km to ensure that the train current returns through the additional feed-wire in a way similar to autotransformers for MVAC systems.

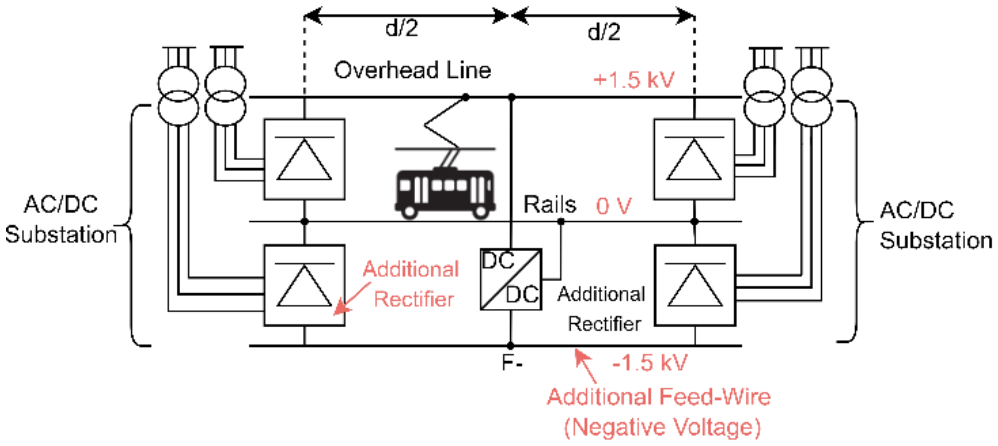


Fig. 1. *Three-wire arrangement for DC supply proposed in* [43] *with additional feed wire with negative polarity with respect to the rails*

This configuration has also been simulated in [44] with voltages of 3, 6 and 9 kV DC for the third wire. Moreover, the power losses in feeders, contact lines and rails for different substations' intervals have been calculated and compared with conventional

DC systems. In one study, the interval of two TPSs has been considered as 8 km, and the substation rectifiers and intermediate DC-DC converters have been assumed to be lossless. In this scenario, the average power losses for conventional 1.5 kV DC system have been calculated as 813.3 kW for a nominal power of 4,500 kW. Using 3, 6 and 9 kV DC third wire and one intermediate DC-DC converter, the average losses reduce by 42.8%, 55.3% and 57.4%, respectively. However, the average losses for 3, 6 and 9 kV DC three-wire systems are still higher than conventional

3 kV DC system. On the other hand, the study suggests that increasing the number of intermediate DC-DC converters in three-wire systems improves the efficiency. For instance, adding another intermediate converter to the 9 kV DC three-wire system decreases the power losses by 48.8% with respect to the case where there is only one intermediate DC-DC converter in the system. This is clearly dependent on the actual efficiency of the DC-DC converter that has not been considered in the study.

In [45], thyristor rectifiers have been proposed to feed an intermediate MVDC feeder, and fully controllable synchronous buck converters operate as TPSs and feed a traditional DC catenary, as shown in Fig. 2 for a 750 V system. The simulation results for a load of 1 MW show that, in comparison to conventional 750 V DC systems, the new configuration improves the efficiency of the feeding system (feeders and overhead contact lines) by up to 2% and reduces catenary voltage drop by up to 3%. The losses of the power converters, however, have been neglected in this study and will certainly reduce the benefits of the solution. The reference does not clearly mention the voltage level of the AC side and the MVDC feeder. Besides, the proposed system encounters some challenges including the control of circulating current between the buck converters and possible low-frequency power oscillation between the converters, which are not addressed in the study.

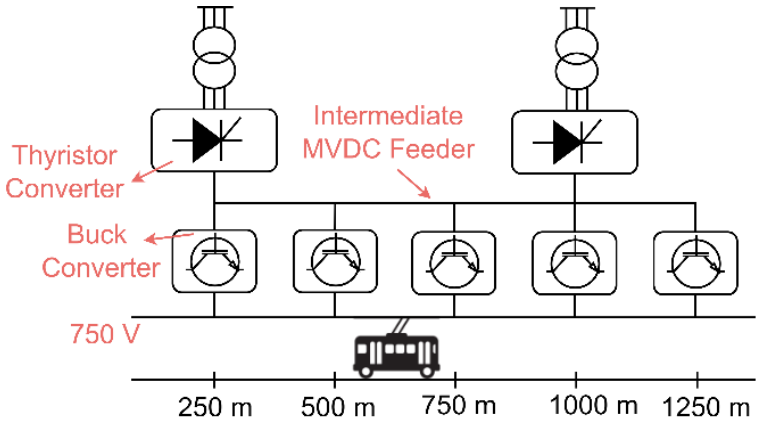


Fig. 2. *Feeding 750 V DC railway from MVDC feeder as proposed in* [45]

As another approach, supplying urban 750 V DC railways from MVDC distribution grid has been investigated in [46]. The proposed arrangement consists of a dual active bridge converter that converts MVDC to LVDC, and charging stations for electric vehicles in the railway TPSs. In urban railways, the substations are normally close to the train stations. Hence, the charging stations are located in vicinity of transport hubs and can be used by electric vehicles such as electric cars and public electric buses. The charging stations enable the railway operator to utilise the electrification infrastructure during railway idle periods. This paper, however, gives no details about the control architecture, protection issues and other practical challenges.

In [47], the authors have proposed a configuration where a small number of high-power rectifiers are supplied by a HVAC grid to generate a multi-terminal MVDC bus alongside the railway. This MVDC feeder, shown in Fig. 3, operates with the voltage level of 120 kV DC and can feed both DC and AC railways. The minimum distance between the rectifiers is 100 km. In case of AC railways, several inverter substations, located at distances smaller than the rectifiers, provide a suitable single-phase AC voltage for the overhead line. A possible realisation for the AC-DC converter has been also suggested, where several converter cells are connected in series at both AC and

DC sides. Each converter cell consists of a voltage source converter (VSC), which is connected to a cycloconverter through a medium-frequency transformer (MFT). This topology, however, requires series connection of power electronic switches, and the paper does not describe it in detail. Moreover, undesired current circulation between the converters is a critical issue which has not been discussed.

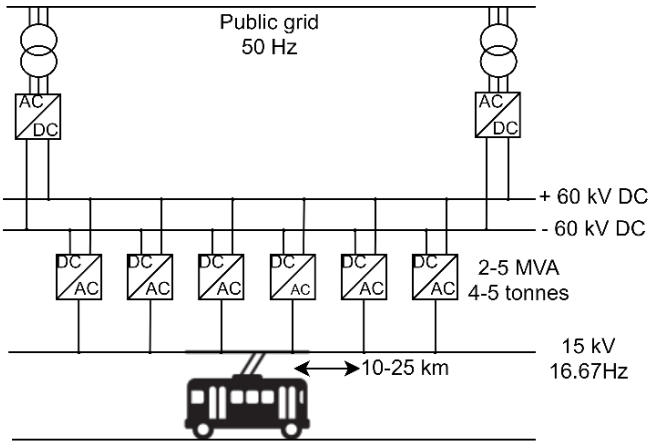


Fig. 3. *The multi-terminal MVDC bus concept proposed in* [47]

Reference [48] has further evaluated the above proposal using a unified AC-DC optimal power flow model and an on/off control of DC-AC converters feeding the overhead line. In comparison to a 16 2/3 Hz, 15 kV MVAC system, a MVDC feeder would reduce the voltage drop of the catenary and reduce transmission losses. Furthermore, an optimisation problem has been formulated to determine the optimal control of the converters [49] to minimise total active power losses. The performance of MVDC feeder solution has been compared with both centralised and decentralised 16 2/3 Hz 15 kV MVAC systems, showing better voltage regulation and less power losses in the MVDC system.

A similar approach has been presented in [50], where modular multilevel converters (MMCs) are connected to 110 kV AC main grid and create a 160 kV DC intermediate

feeder. Single-phase MMC inverters and step-down transformers are then used to feed the 27.5 kV AC railway electrification line. This arrangement benefits from high power quality, simple overhead line without neutral sections, modular design of power converters, and easy integration of renewable energy resources and energy storage systems, which can be connected to the MVDC intermediate feeder. However, due to high voltage level of the AC grid and the MVDC feeder, the number of required submodules in the MMCs are high, and step-down transformers are still needed on the railway side. In addition, the MMC rectifiers have been implemented with half-bridge submodules, which are unable to block the DC fault current. Thus, the system should be protected by MVDC circuit breakers, which are costly [3].

2.2. Systems with MVDC overhead lines

MVDC overhead lines have been first proposed in [16], based on a monopolar multi-terminal radial network fed by 12-pulse thyristor converters. To keep reasonable insulation levels for the catenary, the system voltage has been chosen at 30 kV, similar to existing AC electrification systems. This feeding arrangement can limit the DC fault current by using controlled thyristor rectifiers. The paper has also proposed a design for locomotives with a simple line-commutated high-voltage inverter, a MFT operating at few hundred Hertz, a four-quadrant rectifier and a three-phase voltage source inverter feeding the traction motors. However, the paper gives no details on the design of controllers, and especially how the fault current is determined and limited with acceptable time response. In addition, the high-voltage inverter installed on the locomotives has been implemented with thyristors, which require complicated commutation circuits.

Starting from the results of [16], a more practical solution with a new MVDC multi-terminal system is introduced in [1]. The proposed system uses VSCs as building blocks

of the converters, which allow a better integration of the railway with distributed generation and energy storage units. As shown in Fig. 4, various subsystems with different voltage levels can be connected to a 15-25 kV DC railway line as a distributed energy hub. In this paper, MMCs with half-bridge submodules have been proposed for TPSs, implying that the system should be protected by MVDC breakers.

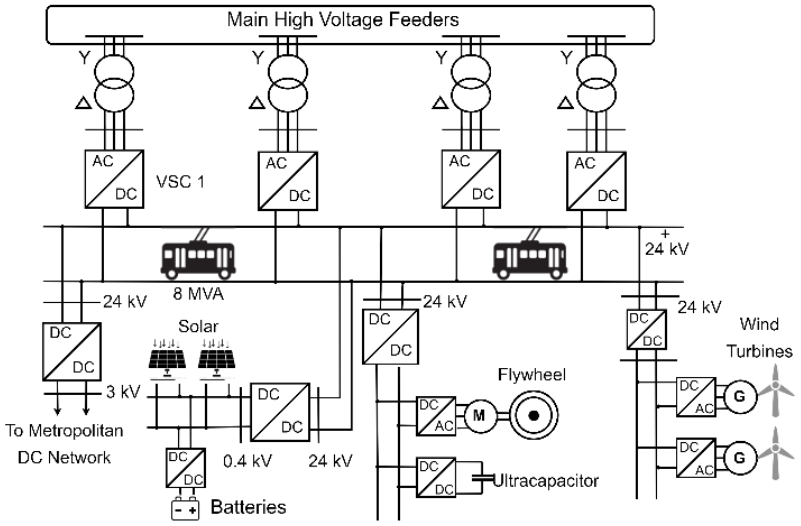


Fig. 4. *Proposed MVDC multi-terminal system* [1]

The authors have also suggested two architectures for real-time control and power balancing in the MVDC network. The first is based on local VSC controllers and targeted at maintaining a constant DC voltage at the point of common coupling. The second proposal is to implement a central controller, where the DC voltage reference for each local controller is obtained from a droop function. The reference signal is inversely proportional to the substation output current. Moreover, a signal from a secondary central control loop is added to the DC voltage reference to optimise and coordinate the power drawn from the AC grid, considering constrains of transmission system operator.

In addition, two novel structures for rolling stocks which are compatible with both 3 kV DC and 24 kV DC supplies have been introduced. The first structure uses bidirectional

isolated DC-DC converter implemented with multilevel VSC, MFT, and conventional VSCs. The second scheme has a simpler design, where two VSCs are connected to each traction motor in parallel. For 3 kV systems, the DC side of VSCs are connected in parallel, while for 24 kV DC supplies, a switch changes their connection to series. The paper has also shown by means of numerical simulations that the proposed system has higher capacity over a conventional 2×25 kV AC railway supply system while it benefits from the mentioned advantages of MVDC systems.

The concept of integrating electric railway systems into smart grids has been also described in [3]. Various structures for smart grids have been proposed, including LVDC, MVDC, and AC railway microgrids. Because of the aforementioned advantages of MVDC electrification systems and in particular, facilitating direct connection of distributed energy resources, implementing fast and ultrafast charging stations for electric vehicles, and integrating LVDC systems like metropolitan railways, MVDC railway microgrids have been considered as the most promising solution. The overhead line voltage should be in the range of 7.5-24 kV DC, which can be selected based on the existing infrastructure and regional and geographical conditions.

The authors of [6] have also proposed a simulation model to compare the MVDC catenary with auto-transformer based MVAC systems at mains frequency. The results show that the MVDC supply draws balanced currents from the three-phase grid, and provides better overhead line voltage regulation in comparison to the MVAC system. Since the simulated MVDC system includes a droop control system, the power consumption is shared among the TPSs. In the MVAC systems, however, each TPS feeds the trains on its own section, as the feeding sections are electrically isolated. This increases the average power supplied by each substation, leading to higher power ratings for each MVAC substation in comparison to their MVDC counterparts.

Furthermore, reactive power consumption in the MVDC system is limited to the transformer and AC side cables in TPSs, and this reactive power can be compensated by the TPS converters.

As another comparison, a simulation in which a portion of Paris-Lyon high-speed line operated in 25 kV AC is replaced with 25 kV DC system has been reported in [51]. The results show that due to lack of inductance in DC systems and parallel operation of TPSs, 25 kV DC supply improves the voltage profile. Specifically, the catenary average and minimum voltage for the MVAC system are 23 kV and 18 kV, while for the MVDC system, are 25 kV and 24.5 kV. In addition, the average active power consumption decreases by 3.5% in the MVDC system. The analysis also shows that with the same voltage profile as the MVAC railways, MVDC substations can be located 30% further apart when they are feeding the same load.

The effect of the MVDC catenary voltage level on the overhead line cross-sectional area and spacing between TPSs has been investigated in [7]. This has been done for both suburban and high-speed transport services via a mathematical model which considers the rail-to-ground voltage, pantograph voltage and temperature of the overhead line. Voltage levels between 1.5 kV and 10.5 kV with steps of 1.5 kV have been examined, and the results show that for voltages above 7.5 kV DC, both cable cross-sectional area and substation spacing are comparable with common AC systems.

Furthermore, a case study based on Paris-Strasbourg line with real data of traffic conditions has shown that a 9 kV DC system has the same performance of a 2×25 kV AC system, while having simpler power supply diagram and not requiring neutral sections and autotransformers. In this paper, however, the suggested topology for the TPS converters is a full bridge diode converter protected by high-cost solid-state circuit breakers.

Following this research, SNCF-Réseau has started a study to convert its 1.5 kV DC railway lines to 9 kV DC [52]. A strategy for replacing the DC railway supply system from low-voltage (1.5 kV or 3 kV) to 9 kV has been introduced in [53] and is shown in Fig. 5. In the first step of the evolution, the conventional rectifiers are still connected to the overhead line. However, some intermediate substations are replaced by a DC-DC power electronic transformer, which feed the low-voltage overhead line from a 9 kV feeder. At the final step, the voltage level of the catenary is raised to 9 kV, and all of the conventional rectifiers are removed. In this stage, power electronic transformers must be installed on the trains. A similar study on the Italian railway [54], has shown similar advantages for 9 kV DC systems.

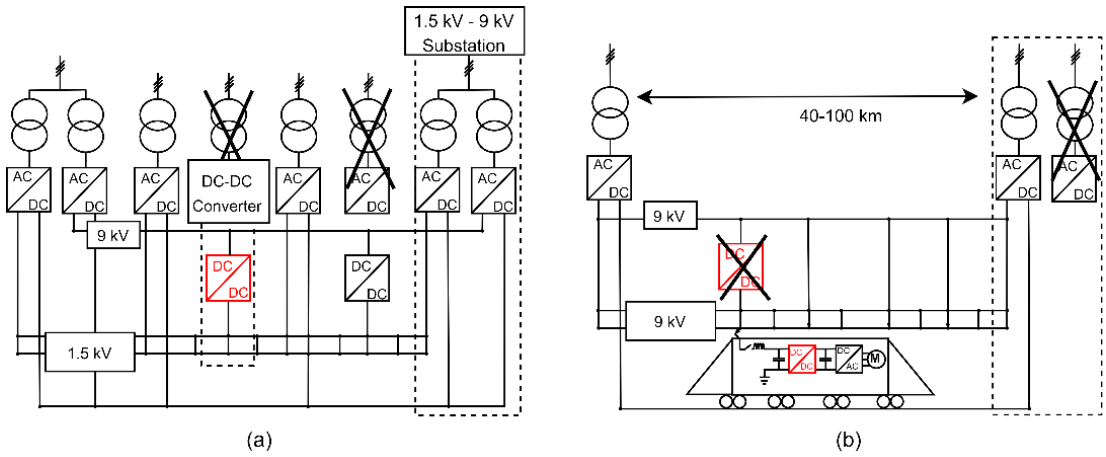


Fig. 5. *The strategy for changing the low-voltage DC to 9 kV DC supply proposed in* [53]*: (a) Low-voltage catenary along with 9 kV feeder and power electronic transformer, (b) 9 kV catenary and on-board power electronic transformer*

The advantages of increasing the voltage level of DC railways to up to 24 kV have also been discussed in [55], [56] in which their former study has investigated series connected 24-pulse current source converter as the most efficient topology for the TPSs, and has suggested the use of rolling stocks working with both LVDC and MVDC

voltage levels. However the TPS converter [55] and the train converter [56] have not been investigated in terms of performance and control.

Moreover, modelling and simulation of a double-end fed 24 kV DC railways with two TPSs have been presented in [57], as shown in Fig. 6. In this study, a local control strategy is used, in which one of the TPSs is operated in constant power mode, and the other one is operated in constant DC voltage mode.

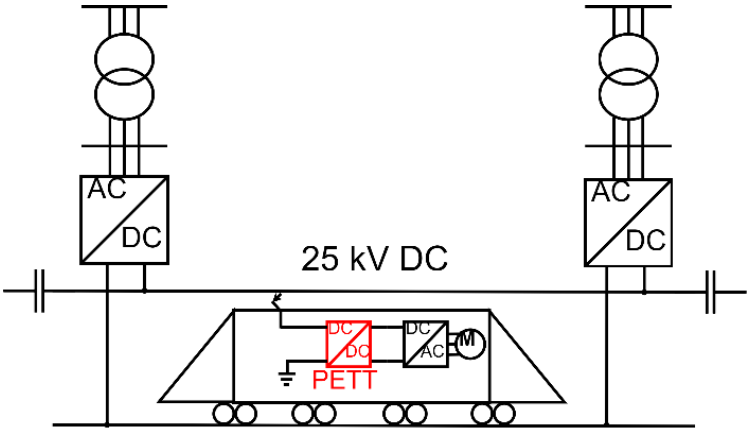


Fig. 6. *Double-end fed MVDC railway electrification system*

In the MVDC railway networks, there is the possibility of having circulating currents between the supply points. Therefore, it is important to implement a developed control scheme to avoid this situation. The control scheme can be even more advanced and incorporate conditions for which the circulation of current is intentionally sought, for example to de-ice conductors for low temperatures or for create a parallel path between the nodes to ease congestion on the AC grid.

3. Power converters for MVDC electrification systems

3.1. Converter topologies for TPSs

The topologies for MVDC TPSs can be classified to VSC and current source converter (CSC) families and are discussed in the following. All converter topologies include on transformer to ensure galvanic isolation from the grid. This is because railway operator

needs to maintain control on their grounding systems and the isolation reduce interference with other railway equipment, such as signalling.

3.1.1 *Voltage source converters*: High-voltage, high-power VSC topologies which can potentially be implemented in the MVDC TPSs are shown in Fig. 7.

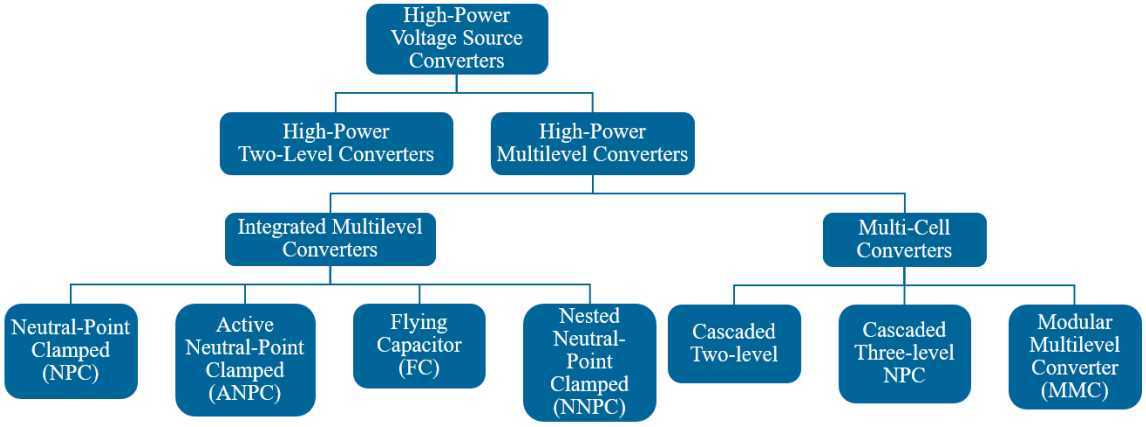


Fig. 7. *High-power VSCs for the 25 kV MVDC railway*

For high-voltage application, it has been implemented a two-level VSC for a small scale high-voltage DC (HVDC) transmission network with the voltage of 20 kV DC and power rating of 3 MW [58], [59]. At the AC side, this converter has been connected to 10 kV AC without a transformer. A large number of insulated-gate bipolar transistor (IGBT) switches have been connected in series to enable the converter to operate at high voltages. In order to turn on/off the series IGBTs simultaneously, a special gate unit has been designed. In addition, voltage dividers have been used to evenly distribute the voltage across the series IGBTs and decrease the switching losses. Adding these extra circuitries, however, increases the total losses, initial and maintenance costs, and the design efforts and decreases the converter's reliability.

Developing multilevel VSCs has provided new solutions to high-power applications and they are extensively used in motor drives, static volt-ampere reactive compensators (SVCs), flexible alternating current transmission systems (FACTS), battery energy

storage systems and HVDC transmission systems [60]. Multilevel converters in MVDC applications have been implemented to interconnect two asynchronous AC power systems with two back-to-back three-level neutral-point clamped (NPC) converters via a common 15.9 kV DC bus. The converters are responsible for reactive power support as well as active power transfer [61]. The NPC converter does not have a modular configuration and needs a large number of series semiconductor switches to operate at higher voltage levels, which leads to complex and expensive designs [60]. The voltage balancing across the elements in NPC converters is another challenge regarding their use at high voltages [62]. The active neutral-point clamped (ANPC) topology is similar to the NPC topology, and it has solved the unequal loss distribution problem in NPC topology by replacing the clamping diodes with IGBT-Diode modules. The flying capacitor (FC) topology has also a similar arrangement to the NPC topology, where the clamping didoes are replaced with capacitors. The nested neutral-point clamped (NNPC) topology is a combination of NPC and FC topologies [63].

Multi-cell converters family have been proposed to avoid series connection of devices. Cascaded two-level VSC and cascaded three-level NPC are two members of this category. In these converters, shown in Fig. 8, a number of two-level (three-level NPC) converters are cascaded, so each stage can be realised by low-voltage devices. The stages can be controlled independently, and thus, the converter can reach to higher resulting switching frequency without increasing the actual switching frequency at the cost of more complicated control [64], [65]. The AC input for each stage, however, should be isolated from the other stages. This implies that the converter needs $N_{Two-level}$ transformers, or a multi-winding transformer with $N_{Two-level}$ isolated secondaries.

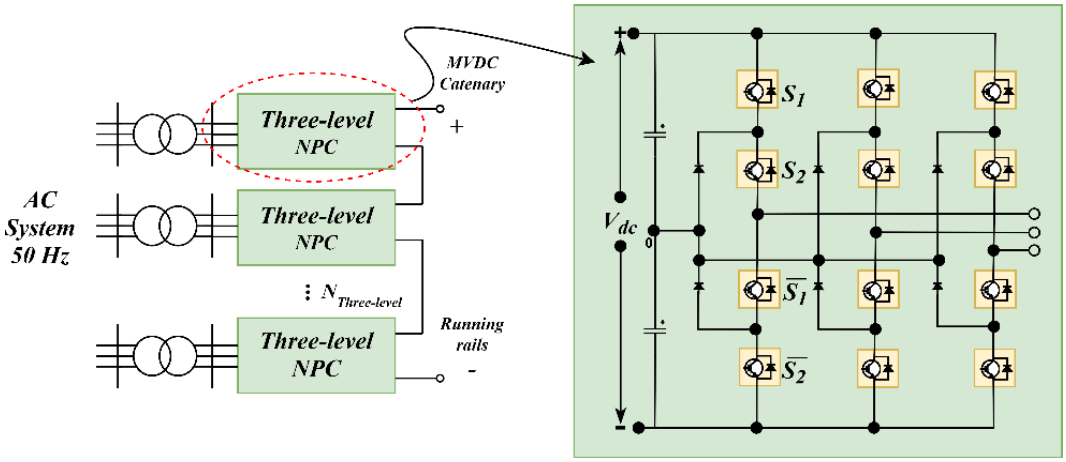


Fig. 8. *(a) Cascaded two-level converter, (b) Cascaded three-level NPC converter*

MMCs also belong to multi-cell converters family. Instead of cascaded converter bridges, MMCs consist of several submodules in each phase. The DC sources in submodules are not isolated and are directly charged and discharged through the common DC bus. Fig. 9 and Fig. 10 depict the MMC topology and various submodule arrangements. Comparison of well-known submodule arrangements for the MMCs is presented in Table 1. Table 2 presents several studies on using MMCs in MVDC applications. In particular, the performance of MMCs in 9 kV DC railways has been analysed by real-time simulations in [66], showing the feasibility of using MMCs in the MVDC railways.

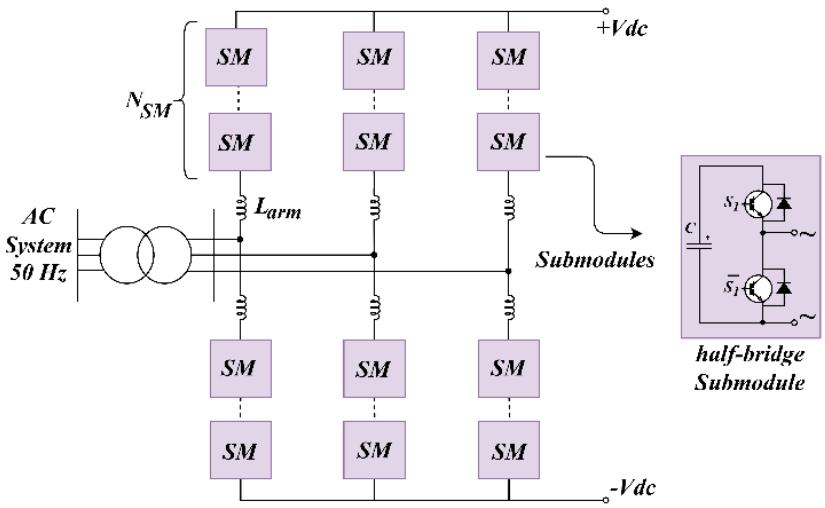


Fig. 9. *MMC topology and half-bridge submodule*

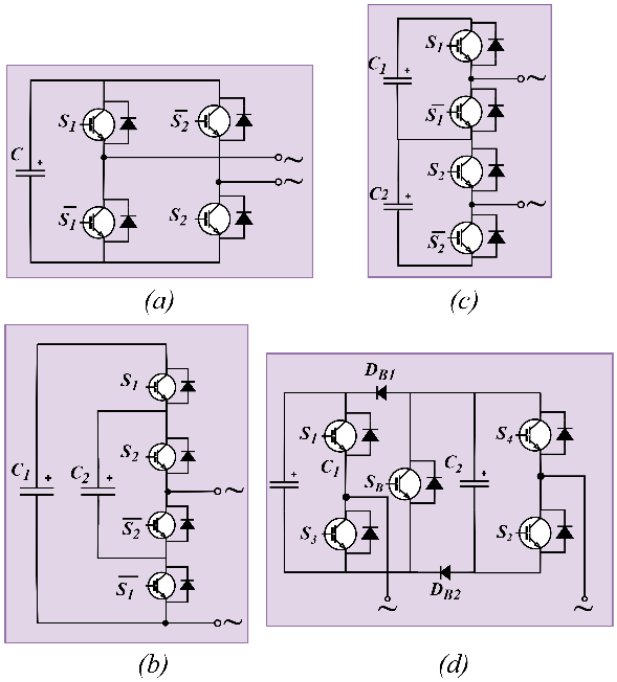


Fig. 10. *Submodule arrangements for MMCs:*

(a) Full-bridge, (b) Flying capacitor, (c) Cascaded half-bridge, (d) Double clamp [63]

Table 1 Comparison of submodule arrangements, as indicated in [63]

Characteristic	**Half-bridge**	**Full-bridge**	**Flying capacitor**	**Cascaded half-bridge**	**Double clamp**
Number of output voltage levels	2	3	3	3	4
Maximum blocking voltage of submodule	Vc*	Vc	2×Vc	2×Vc	2×Vc
Maximum Number of DC capacitors normalized to Vc	1	1	3	2	2
Number of devices normalized to Vc	2	4	4	4	7
Maximum Number of devices in conduction path	1	2	2	2	3
Power losses	Low	Moderate	Moderate	Moderate	High
Design complexity	Low	Low	High	Low	High
Control complexity	Low	Low	High	Low	Low
Bipolar operation	No	Yes	No	No	Yes
DC fault blocking	No	Yes	No	No	Yes

* Vc is the capacitor nominal voltage in the submodules. For the submodules with more than one capacitor, Vc refers to the lowest nominal voltage among capacitor voltages.

Table 2 Studies on the use of MMCs in MVDC applications

Application	Submodule	Voltage Level (kV)		Power Rating	#Modules (per phase)	#Switches (per phase)	Controls	Ref
		AC*	DC					
MVDC distribution network	Half-bridge	6.6	12	1 MVA	16	32	Arm-balancing, AC current	[67]
MV rectifier for motor drives	Half-bridge	6.9	10.5	3.15 MW	22	44	AC and DC current, average capacitor voltage, circulating current, vertical and horizontal voltage balance**	[68]
MVDC distribution network	Not specified	6.6	10	7 MVA	20	Not specified	DC voltage, circulating current, AC line current, horizontal and vertical energy balancing	[69]
Ships with variable speed gas turbine (variable frequency at the AC side)	Half-bridge	4.16	10	25 MW	20	40	DC voltage, inner current	[70]
Power-hardware-in-the-loop facility - Four MMC units	Full-bridge	3.3	6 to 24	1.25 to 5 MW	12 (in each individual MMC)	48	Branch current, AC current, DC short circuit current, and DC voltage controllers, individual cell energy and branch energy balancing	[71]
Flexible MVDC voltage source – two MMC units	Full-bridge	3.3	±5 to ±10	500 kW	16	64	DC voltage and DC short circuit current controller, inner voltage drop compensator	[72]
Inverter stage in an electric ship MVDC system	Half-bridge	220	6	150 kW	8	16	AC voltage controller, sorting algorithm, hierarchical redundancy strategy	[62]

* Voltage level for AC side corresponds to line-to-line root mean square (RMS) voltage
** The aim of vertical balancing is to equally distribute the stored energy between two arms of the same leg. Horizontal balancing aims to equalize stored energy in the legs [68].

In addition to aforementioned submodules, there are other submodule arrangements with higher number of switches and higher complexity, which have been extensively compared in [73]. In general, higher voltage blocking capability, bipolar output voltage and symmetrical voltage levels are desirable for MVDC electric railways, but these characteristics are gained at the cost of higher number of components and consequently, higher cost and conduction losses, and lower reliability. In addition, the control design, mechanical structure of submodules and the protection schemes against internal faults is more complicated.

MMC and VCSs have been combined to form the alternate arm converter (AAC) [74], shown in Fig. 11, in which several series connected IGBTs are in series of each arm of MMC to control the direction of the voltage. Using these director switches, the voltage rating of each arm is approximately half of the voltage rating in a conventional MMC in normal operation. AAC is also able to block DC fault current as well as operating as static synchronous compensator (STATCOM) in DC fault conditions by adding more submodules. Nevertheless, the total number of IGBTs is less than a conventional MMC with full-bridge submodules.

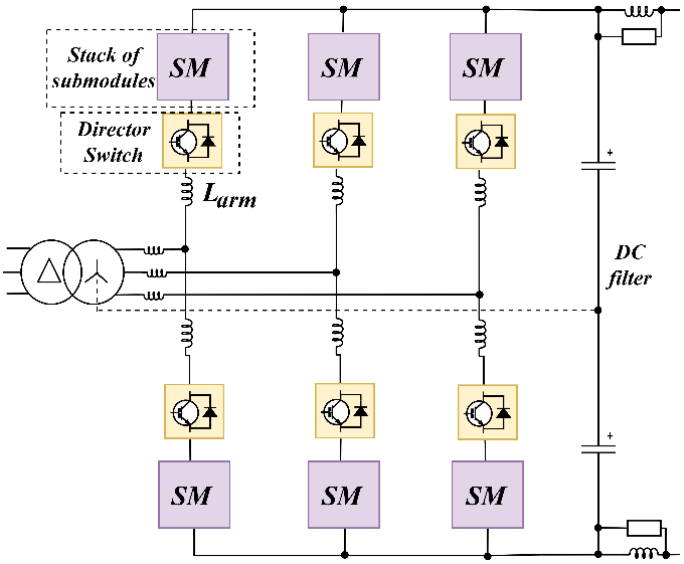


Fig. 11. *Alternate arm converter* [74]

Switching losses and the number of IGBTs of AAC can be optimised when the peak voltage of the AC side is about 27% higher than the voltage of DC terminals, i.e., the DC voltage produced by each arm. In this situation, the converter operates in a "sweet spot" condition because the energy storage devices work at their nominal ratings. In sweet spot conditions, director switches are switched at zero voltage (soft switching), which leads to reduction in their switching losses. However, this comes at the cost of losing the independent control of active and reactive power. Various methods have been proposed to address this issue at the cost of considerable increase in the voltage rating of the converter [73].

AACs benefit from compact structure, lower number of submodules, soft switching feature and low switching losses, reduced number of active and passive elements, and very small or no AC filters. On the other hand, they suffers from series connected switches, higher conduction losses, and limitation on active and reactive power control [73].

3.1.2 *Current source converters*: CSC family can be divided into two categories: load-commutated (LC) or line commutated converters (LCC), and pulse-width modulation (PWM) current source converters. In LCCs, widely used in railway electrification and HVDC systems, the semiconductor switches are commutated with the mains grid frequency (50 or 60 Hz). Conversely, the switching frequency is much higher in the PWM current source converters.

Diode and thyristor bridge rectifiers are the two types of CSCs already used in conventional LVDC railway electrification systems [4]. In order to reduce the DC voltage ripple, improve the total harmonic distortion (THD) at the AC side and reach to higher output voltages and currents, several diode or thyristor bridges can be connected in parallel or series and form 12, 24, 36 and 48 pulse converters, and multiple

winding transformer are needed to introduce the phase shift between the various AC inputs of the bridges [75].

Thyristor rectifiers can regulate the DC output voltage and, hence, increase TPSs spacing. On the other hand, when the firing angle increases, the power factor reduces and the THD at the AC side and the harmonic content of the DC voltage both increase. Nevertheless, the AC side harmonics are within acceptable values defined in IEEE519 standard, and the DC ripples can be mitigated by capacitor filters [76].

The energy from regenerative braking of train can be sent back to the grid using reversible TPSs. To achieve this, a separate thyristor inverter is connected to the rectifier in anti-parallel configuration [77]. Another solution is to connect an active PWM converter to the rectifier. In braking mode, this converter operates as an inverter, while in normal mode, it operates as an active power filter for the rectifier [78].

For both diode and thyristor converters the input power factor cannot be regulated and if reduced by the presence of overlap, that increases with the load. Concerning DC side faults, CSCs can be designed to tolerate DC short circuits. In thyristor-based LCCs, the firing angle can be controlled to limit the DC fault current [79]. Furthermore, in force-commutated CSC topologies, a series connected diode is integrated with each semiconductor switch, enabling it to block the voltage in both directions. Hence, it can block the voltage that supplies the short circuit current. On the other hand, force commutated CSCs must be protected against open circuit faults using emergency current paths [80].

3.1.3 *Double-stage conversion*: Another option for implementing high-power MVDC converters is to use double-stage conversion schemes. In these schemes, the AC input voltage is first converted to an unregulated DC voltage, then the DC voltage

is regulated to the desired value. For instance, the use of single-star bridge cells rectifier as the first stage, and dual active bridge (DAB) converter as the second stage has been described in [81], [82] and the use of diode rectifier connected in series with a boost chopper has been mentioned in [70]. The DAB topology is presented in Fig. 12 for a fully-bidirectional converter, but the second stage can use diodes if the power does not need to be reversed.

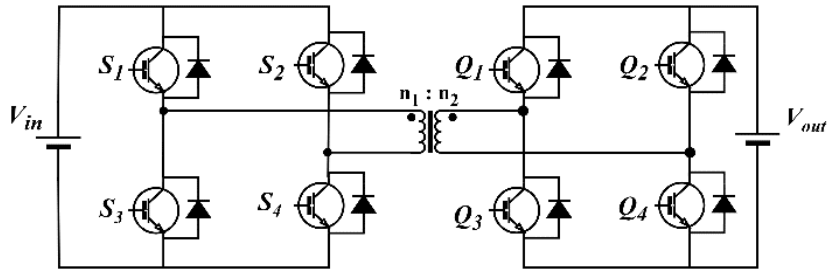


Fig. 12. *DAB converter*

In comparison to using a single high-power AC-DC converter, the double-stage conversion is less efficient and reliable due to the higher number of semiconductor devices. On the other hand, double-stage configurations with high-frequency transformers have a smaller overall size, which could be useful when the cost of land for the TPS is at a premium.

3.1.4 *Discussion on the topologies for the MVDC TPSs:* A direct comparison between converter topologies is always difficult, as current and voltage stresses depend on the topology and often the design can be optimised for each different application. This section attempts at providing an indication of the component count of these topologies assuming that the same switching devices are adopted. The selected devices are chosen with the highest blocking voltage and current available at the time of writing the paper, considering that the typical converter ratings will exceed both in terms of voltage and power. The analysis is based on a reference case where the power output,

the input and output voltages, and the overloading capability are those expected from MVDC systems or are equivalent to existing MVAC systems. Tables 3 and 4 show the selected specifications of the MVDC TPS and the semiconductor devices, respectively used as a reference.

Table 3 Specifications of the MVDC TPS

Specification	**Power rating**	**Voltage at AC grid**	**Nominal voltage of catenary**	**Set point of DC voltage for the converters**	**Maximum voltage of catenary during long term overvoltages**	**Overload capability**
Value	30 MVA	33 kV RMS	25 kV	27.5 kV	38.75 kV	450 %

Table 4 Characteristics of the selected semiconductor devices

Semiconductor device	**Maximum repetitive peak forward and reverse blocking voltage (V_{DRM}, V_{RRM})**	**Maximum value for the average on-state current $I_{T(AV)}$**	**Maximum value for RMS on-state current $I_{T(RMS)}$**	**Maximum collector-emitter voltage V_{CES}**	**Maximum DC collector current I_C**
Dynex DCR3640H85 thyristor	8.5 kV	3.62 kA	5.69 kA	-	-
ABB 5SNA 1000G650300 HiPak IGBT-diode module	-	-	-	6.5 kV	1 kA
Infineon D4600U clamping diodes	-	-	-	4.5 kV	4.45 kA

In the following and with the help of Table 5, the converter topologies are compared against criteria required by the MVDC railway electrification system, showing the compromise between the solutions:

- Power efficiency: The thyristor converters have lower switching losses and higher power efficiency compared to the VSCs. As indicated in [83], the thyristor-based converter designed for the MVDC railway has the power efficiency of above 99% when the DC current is between 30% to 450% of nominal load.
- Initial capital and maintenance costs: The number of required components is an indicator for costs of a converter. For the topologies with series connected devices, the costs for voltage divider components are also added. Moreover, the number of required transformers also affects the overall cost and size of the converter. Table 5 reveals that the thyristor-based converter requires the lowest number of components among other topologies. Furthermore, modular topologies can be easily developed for medium and high voltage levels using identical modules, and this reduces the design complexity and maintenance costs.
- Reliability: In the case of failure in a module, it is possible to operate MMCs and AACs with reduced capacity instead of interrupting the power supply. This is also the case for cascaded converters if an IGBT-Diode module or a stage fails. Moreover, series connection of devices also negatively affects the reliability of thyristor-based converters, two-level VSCs, three-level NPC converters and AACs.

Table 5 Comparing topologies for use in the MVDC TPS

Factor/Topology	**12-pulse rectifier and inverter in anti-parallel configuration**	**Two-level VSC**	**Three-level NPC converter**	**Cascaded two-level VSC**	**Cascaded three-level NPC**	**MMC with full-bridge submodules**	**AAC (full bridge-short overlap period)**
Number of semiconductor devices	168 thyristors	504 IGBT-Diodes	504 IGBT-Diodes/ 108 Clamping Diodes	12 stages (504 IGBT-Diodes)	6 stages (504 IGBT-Diodes/144 Clamping Diodes)	12 submodules (1440 IGBT-Diodes)	218* IGBT-Diodes
Number of series components	9 thyristors in each 6-pulse bridge	12 IGBT-Diodes	6 IGBT-Diodes/9 Clamping Diodes	-	-	-	6 IGBT-Diodes
Number of energy storage elements	1 L**	1 C	2 C	15 C	8 C	90 C/6 L	48 C/6 L
Transformer	1×Three w***	1×Two w	1×Two w	15×Two w	8×Two w	1×Two w	1×Two w
Harmonic distortion of currents at the AC side	↑↑↑↑↑	↑↑↑↑	↑↑↑	↑↑↑	↑↑	↑	↑
Ability of limiting DC short circuit current	Yes	No	No	No	No	Yes	Yes

* Assuming that the AAC converter can block the DC short circuit currents and operates at sweet spot condition

** L = inductor(s), C = Capacitor (s)

*** w = windings

- Power quality and electromagnetic compatibility: Considering DC voltage regulation, all the topologies use DC voltage control loop.

In general, the produced DC voltage by the VSCs has lower ripples in comparison to thyristor-based converters.

Similarly, the harmonic distortion of AC side currents is less in VSCs, so the AC side filters are smaller. The AC current quality is proportional to the number of voltage levels produced by the converter. Hence, the MMCs and AACs have the best performance. Moreover, cascaded topologies can be controlled with phase-shifted carriers, resulting in a higher AC current quality.

The use of high switching frequencies in VSCs also increases the possibility of interference with the track circuit signals. For instance [84], the magnitude of 5.1 kHz component in the DC voltage of a MMC-based MVDC TPS is 7.5 V. A typical range for operating frequency of track circuits is 4.75 kHz to 16.5 kHz. Therefore, the component should be filtered out or the track circuit frequency should be adjusted to higher frequencies to avoid any interference. For thyristor-based converters, conversely, the interference is low.

- Requirements of multi-terminal DC (MTDC) systems: VSCs are more promising solutions than thyristor-based converters for implementing MTDC systems, providing redundant, reliable and flexible operation [85]–[88]. As an example from HVDC systems, the active and reactive power in VSC-based HVDC systems can be controlled independently and rapidly [89], which enables VCS-based HVDC to integrate weak and passive networks to the system [85]. In addition, the VSCs inherently have faster dynamic response [90]. Among VSCs, however, AACs have limitations in independent active and reactive power control, as discussed before.

3.2. Converter topologies for PETTs

PETTs uses MFT instead of line frequency transformer (LFT), which yields to higher power density and lower weight and volume. PETTs also features high energy efficiency, controlled input and output voltages, currents, power flow, and load protection in case of line disturbances or imbalances. At the current state of the art, PETTs have been developed mostly for MVAC electrification systems, where an additional rectifier stage is needed at the input stage. Fig. 13 shows the classical LFT traction transformers compared to PETTs in MVAC and MVDC systems.

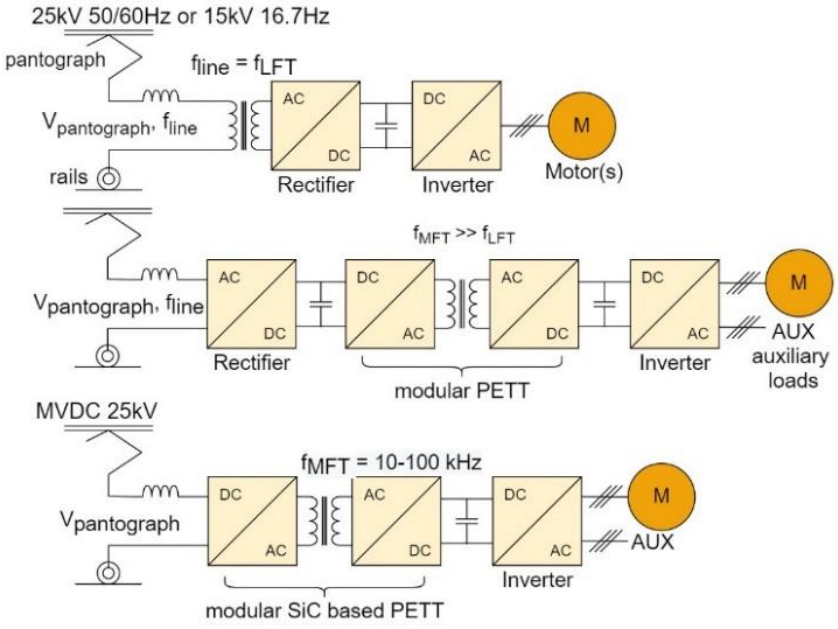


Fig. 13. *Comparison between LFT and PETT in MVAC and MVDC railway electrification systems*

The design of a PETT mainly depends on three key parts: medium-frequency isolation stage, medium-voltage input, and controllability. In order to connect PETTs to medium-voltage power supplies, different configurations have been proposed on the input side and especially the input series output parallel (ISOP) connection.

Based on state-of-the-art, topologies for the PETT can be classified as shown in Fig. 14. Depending on the location of the controlled stage, the traction converter can be either called isolated front-end, with the control stage on the low-voltage side, or isolated back-end converter, with the control stage on the high-voltage side.

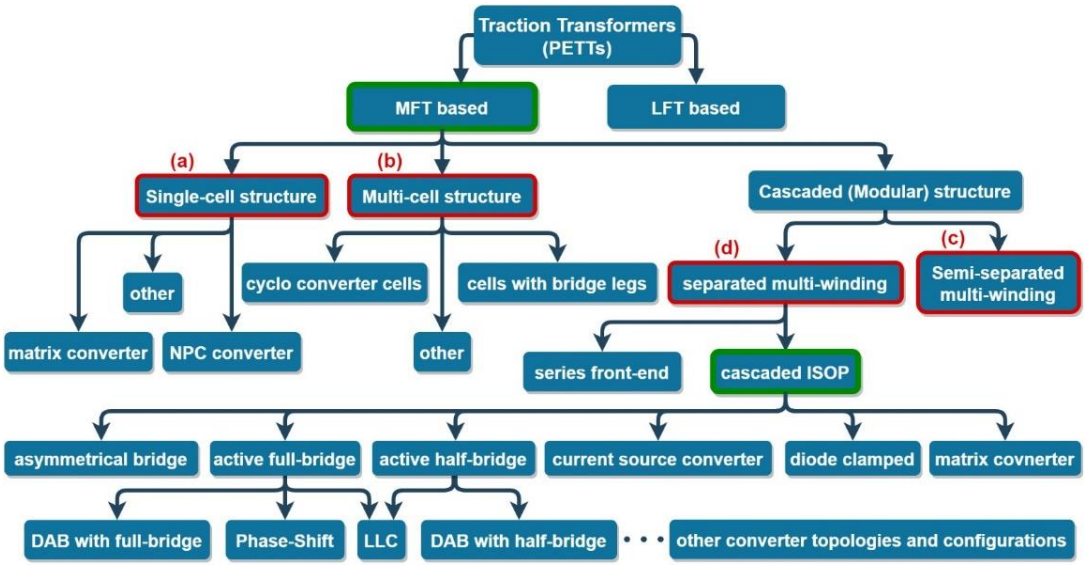


Fig. 14. *Classification of PETTs*

In Fig. 14, the four main MFT topologies are highlighted and each of them is illustrated in Fig. 15. Single-cell traction transformers, shown in Fig. 15 (a), were developed by Weiss [91]. Compared to modular and multilevel systems, they are simpler but with lower reliability. A single cell traction transformer with NPC topology and 10 kV SiC metal oxide semiconductor field-effect transistors (MOSFETs) was recently proposed in [7].

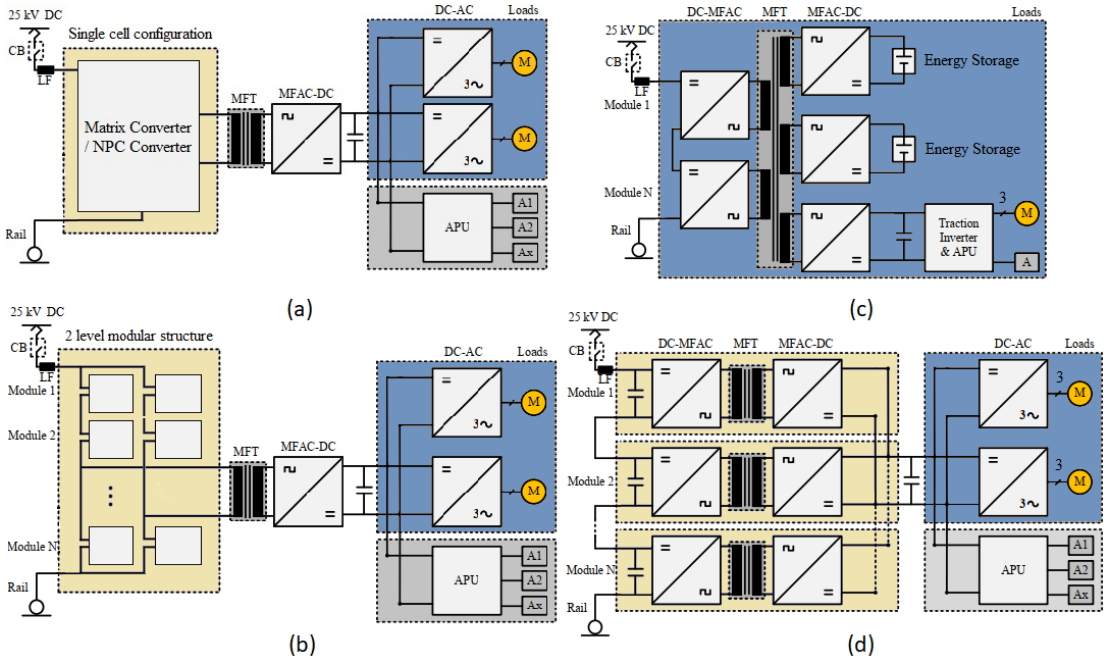


Fig. 15. *The state of the art main PETT topologies (APU: Auxiliary Power Unit, M: Motor): (a) Single cell traction transformer, (b) Multicell topology, (c) Joint multi-winding transformer based cascaded ISOP configuration, (d) Cascaded ISOP with separated multi-winding transformers*

The multi-cell structure proposed in [92], [93] is shown in Fig. 15 (b). MMCs [94] simplify modules by eliminating the necessity of isolated DC supply for each, while keeping a cascaded structure [95]. Siemens developed a full-scale prototype of this topology, achieving high reliability, scalability to higher voltages and capability of dynamic voltage sharing. However, the high number of stages and levels showed increase in costs and losses, and a more complex and difficult control system [96]. To increase the efficiency, the number of cells need to be reduced, for example using high-voltage SiC devices.

The semi-separated multi-winding (SSMW) MFT based topologies, presented in Fig. 15 (c), show feasibility at steady state and in different load conditions, robustness in control, independent output DC links in the secondary and multi-port configuration in the output stage, which facilitate an easier connection of different auxiliary loads and

equipment as well as better bypass features. In addition, SSMW configurations present a matured and fully controllable modular design with balanced power distribution among the modules [96]. ALSTOM developed in 2007 a concept based on this topology, which they called “e-Transformer” – a cascaded eight module propulsion system with a 5 kHz joint multi-winding transformer, obtaining 1.5 MW power and 50% weight reduction compared to classical LFTs [97]. On the other hand, the control of cascaded topologies and the multi-winding MFT is complex, the power density is limited, and joint multi-winding MFT is difficult to manufacture and has weaker fault-handling and reliability capability.

Cascaded ISOP topologies with separated multi-winding (SMW) MFT, shown in Fig. 15 (d), use separated windings (meaning that each DC-DC converter module has its own MFT) to overcome the major disadvantage of the previous topology. This topology can have different variations in the DC-DC converter stage, including active full-bridge converter topology, active half-bridge, asymmetrical active bridge topologies, diode clamped converters, and CSCs [98], [96]. The first example in the industry of a full scale PETT tested on a locomotive was developed by ABB – a 1.2 MW cascaded eight modules traction converter [99],[100]. The SMW MFT is less difficult to produce, it has better fault handling capability and higher reliability as a result of more output stages in parallel. Although this structure needs more devices, which increase the overall costs, the higher initial investment is compensated by the higher efficiency and reliability.

In addition, high-voltage SiC devices can reduce number of modules and, thus, semiconductor devices [98]. Furthermore, inclusion of SiC devices in PETTs can lead to higher power density. As an example, reference [101] analyses the best trade-off among switching frequency, efficiency, filtering elements, noise pollutions and finally

volume and mass. The paper presents an experimental test bench of a resonant single active bridge based 300 kW PETT module prototype for a 9 kV MVDC railway system, investigating two types of 3.3 kV SiC MOSFETs, i.e., 375 A and 750 A Mitsubishi SiC MOSFETs. Currently, this first MVDC PETT is under development as part of FUNDRES project [102]. The two-module small-scale prototype capable of 600 kW power converts 1.8 kV to 1.5 kV, and at nominal power and switching frequency of 15 kHz, the prototype achieves 98.93% efficiency. In addition, experimental results for the two converter modules in ISOP connection have been reported.

In most traction converters developed recently, SMW modular ISOP topologies are favoured for their scalability to higher voltage levels and reliability. Regarding the design of the isolation stage, reference [103] analyses the technical design challenges and trade-offs of MFTs in high-power MVDC power electronic transformers. It also presents a design optimization algorithm, which can generate different feasible MFT designs to obtain maximum power density, based on module requirements, available space, switching frequency, costs and materials. Furthermore, guidelines for choosing the optimal module number are presented. Another recent work [104] examines and classifies MFTs based on core material type, application areas, operating frequency and proposes another design methodology for power electronic transformers using finite element analysis software. However, other existing challenges in PETTs are protection against over-voltages, short circuit induced currents, isolation and thermal management issues [91].

4. Conclusion

This paper has reviewed the proposed technological solutions for medium-voltage DC railways. There are two primary approaches to design the electrification network:

1) using intermediate medium-voltage feeders with low-voltage DC or medium-voltage AC overhead lines; 2) using medium-voltage DC overhead lines.

The paper has also assessed to what extent the topologies presented in the literature address the requirements of railway traction systems.

The investigations of high-power AC-DC converters for the traction power substations and power electronics transformers have shown the advantages and disadvantages of the proposed solutions.

Some outstanding problems have been highlighted in MVDC railways, so Fig. 16 shows the areas in which further research is considered necessary.

Fig. 16. *Research areas in the field of MVDC railways*

While control schemes [33]–[35], stability analysis [31], [32], and corrosion issues [41], [42] in MVDC railways have been investigated in the literature, interaction between the power electronic converters and signalling system, developing suitable protection equipment (e.g., high current MVDC circuit breakers), and economic

analysis need more attention from the researchers. For instance, a cost comparison between MVAC and MVDC railways helps to examine the feasibility and potential benefits of the MVDC railways.

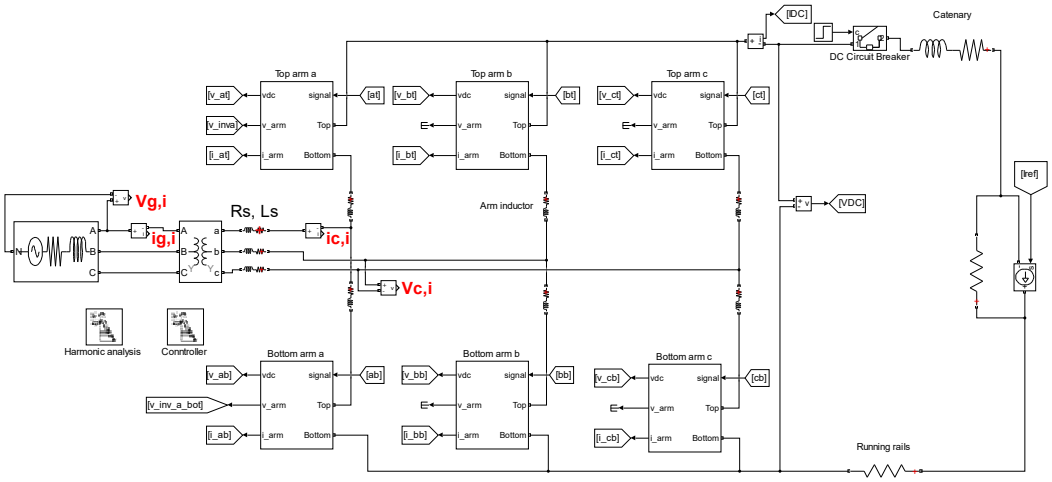
The future direction of research in PETTs should be oriented towards the application of WBG semiconductors, to reduce the number of required devices in a multi-modular system and increase efficiency, without compromising the reliability.

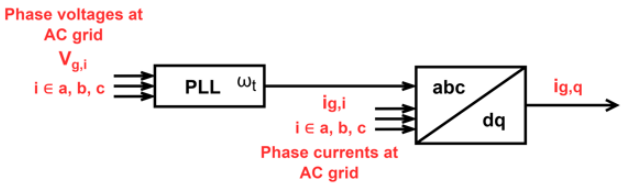
MVDC electrification systems are new to the railway industry. Therefore, there is need to develop new regulations and standards for their installation and operation. In all the mentioned areas, the developed knowledge from other MVDC networks (for example, MVDC distribution networks) can be used as the starting point for the design of future MVDC railway electrification systems.

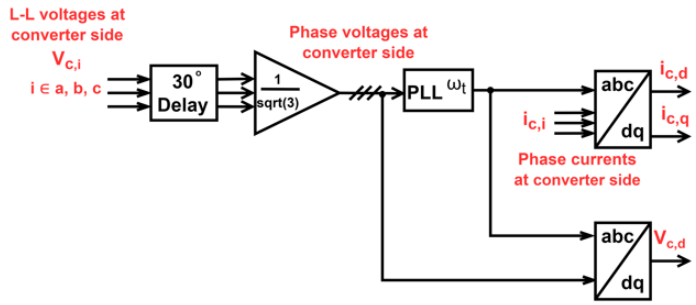
5. Acknowledgments

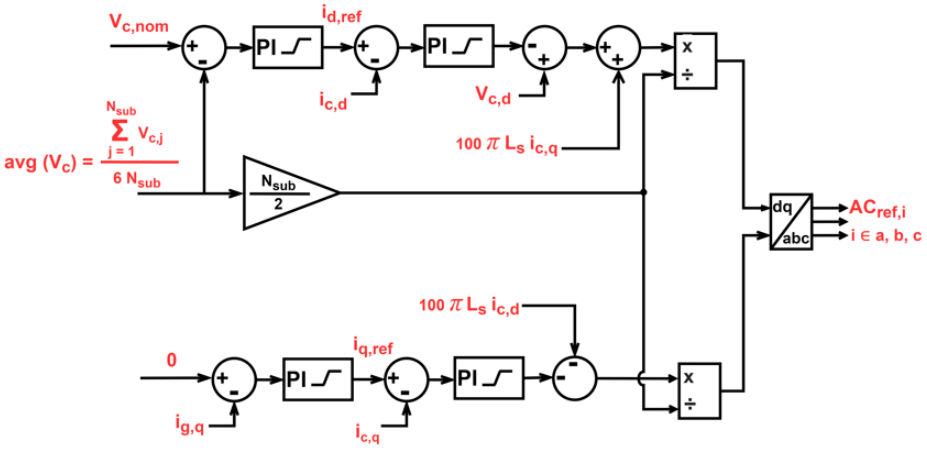
“This project has received funding from the Shift2Rail Joint Undertaking (JU) under grant agreement No 826238. The JU receives support from the European Union’s Horizon 2020 research and innovation programme and the Shift2Rail JU members other than the Union”.

8.2 Appendix B: The overall schematic of the proposed control system and the Proportional−Integral (PI) controller gains used in the MVDC TPS simulations



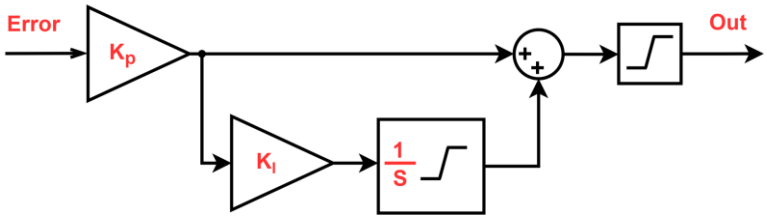






The PI controllers are designed in ideal format. The controller formula is as follows:

$$K_P\left(1 + K_I \frac{1}{S}\right) \quad \text{(B-1)}$$



Parameter	Value
K_{P_VSM}	4 (Ω^{-1})
K_{I_VSM}	50 (s^{-1})
Saturation limits for the outer controller in d axis	± 5000 (A)
K_{P_Q}	0.1 (Ω)
K_{I_Q}	10 (s^{-1})
Saturation limits for the outer controller in q axis	± 1000 (A)
$K_{P\_i_{c,d}}$	5 (Ω)
$K_{I\_i_{c,d}}$	62.96 (s^{-1})
Saturation limits for the inner controller in d axis	± 50000 (V)
$K_{P\_i_{c,q}}$	5 (Ω)
$K_{I\_i_{c,q}}$	62.96 (s^{-1})
Saturation limits for the inner controller in q axis	± 50000 (V)

where the indices VSM and Q denote the coefficients of the outer controllers in d and q axes, respectively.

8.3 Appendix C: Derivation of Equations 3-5 and 3-6

To have DC voltage corresponding to the DC index:

$$n_{top,i} + n_{bot,i} = DC_{index} \qquad i \in a,b,c \ and \ -N_{sub} \leq n_{bot,i} \leq N_{sub} \qquad \text{(C-1)}$$

In addition, the arm voltages should be formed to follow the AC side voltage. In other words, the number of inserted submodules should follow the AC index in each phase.

$$floor\left(\frac{n_{bot,i} - n_{top,i}}{2}\right) = AC_{index,i} \qquad \text{(C-2)}$$

Therefore:

$$2\,AC_{index,i} \leq n_{bot,i} - n_{top,i} < 2\,AC_{index,i} + 1 \qquad \text{(C-3)}$$

Combining C-2 and C-3 yields to:

$$2\,AC_{index,i} \leq 2n_{bot,i} - DC_{index} < 2\,AC_{index,i} + 1 \qquad \text{(C-4)}$$

$$\rightarrow 0.5(2\,AC_{index,i} + DC_{index}) \leq n_{bot,i} < 0.5(2\,AC_{index,i} + 1 + DC_{index}) \qquad \text{(C-5)}$$

Alternatively, C-5 can be written as:

$$n_{bot,i} = floor\left(0.5\left(DC_{index} + 2AC_{index,i} + 1\right)\right) \qquad \text{(C-6)}$$

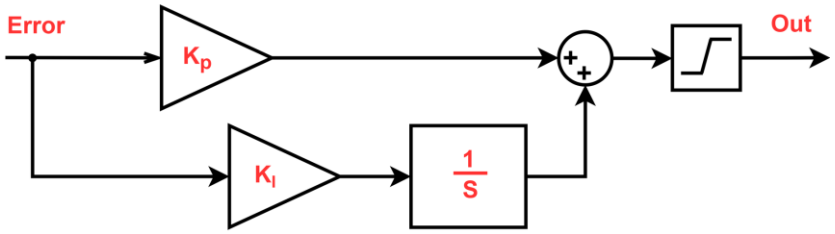
And from C-1:

$$n_{top,i} = DC_{index} - n_{bot,i} \qquad \text{(C-7)}$$

8.4 Appendix D: PI Controller gains used for the short-circuit current controller in the simulations

The PI controller is designed in parallel format. The controller formula is as follows:

$$K_P + K_I \frac{1}{S} \tag{D-1}$$



Parameter	Value
$K_{P\_shortcircuit}$	175 (Ω)
$K_{I\_shortcircuit}$	1 (Ωs^{-1})

8.5 Appendix E: PI Controller gains used for the controllers in the experimental setup

The PI controller blocks [30] are formed in parallel format. The gains are as follows:

- Charging phase:

Parameter	Value
K_{P_VSM}	0.1 (Ω)
K_{I_VSM}	0 (Ωs^{-1})
Saturation limits for the outer controller in d axis	± 1.1 (A)
$K_{P\_i_{c,d}}$	30 (Ω)
$K_{I\_i_{c,d}}$	0 (Ωs^{-1})
Saturation limits for the inner controller in d axis	± 1.5 * $V_{L\text{-}N,peak}$ (V)
$K_{P\_i_{c,q}}$	30 (Ω)
$K_{I\_i_{c,q}}$	0 (Ωs^{-1})
Saturation limits for the inner controller in q axis	± 1.5 * $V_{L\text{-}N,peak}$ (V)

- Normal operation:

Parameter	Value
K_{P_VSM}	0.2 (Ω)
K_{I_VSM}	0.001 (Ωs^{-1})
Saturation limits for the outer controller in d axis	± 4.8 (A)
$K_{P\_i_{c,d}}$	60 (Ω)
$K_{I\_i_{c,d}}$	0 (Ωs^{-1})
Saturation limits for the inner controller in d axis	± 208 (V)
$K_{P\_i_{c,q}}$	60 (Ω)
$K_{I\_i_{c,q}}$	0 (Ωs^{-1})
Saturation limits for the inner controller in q axis	± 208 (V)

- Emulating DC side short-circuit:

Parameter	Value
$K_{P_{shortcircuit},noLoad}$	10 (Ω)
$K_{I_{shortcircuit},noLoad}$	0.1 (Ωs^{-1})
$K_{P_{shortcircuit},Loaded}$	5 (Ω)
$K_{I_{shortcircuit},Loaded}$	0.5 (Ωs^{-1})
Saturation limits for the short-circuit controller	± 100 (V)
Saturation limits for the outer controller in d axis	± 5 (A)

9 References

[1] A. Gómez-Expósito, J. M. Mauricio, and J. M. Maza-Ortega, “VSC-based MVDC railway electrification system,” *IEEE Trans. Power Deliv.*, vol. 29, no. 1, pp. 422–431, 2014, doi: 10.1109/TPWRD.2013.2268692.

[2] D. Serrano-Jiménez, L. Abrahamsson, S. Castaño-Solís, and J. Sanz-Feito, “Electrical railway power supply systems: Current situation and future trends,” *Int. J. Electr. Power Energy Syst.*, vol. 92, pp. 181–192, 2017, doi: 10.1016/j.ijepes.2017.05.008.

[3] M. Brenna, F. Foiadelli, and H. J. Kaleybar, “The evolution of railway power supply systems toward smart microgrids: The concept of the energy hub and integration of distributed energy resources,” *IEEE Electrif. Mag.*, vol. 8, no. 1, pp. 12–23, 2020.

[4] M. Brenna, F. Foiadelli, and D. Zaninelli, *Electrical railway transportation systems*. Wiley, 2018.

[5] X. Huang, L. Qi, and J. Pan, “A new protection scheme for MMC-based MVdc distribution systems with complete converter dault current handling capability,” *IEEE Trans. Ind. Appl.*, vol. 55, no. 5, pp. 4515–4523, 2019, doi: 10.1109/TIA.2019.2917360.

[6] D. Serrano-Jimenez, J. Sanz-Feito, and S. Castano-Solis, “Modeling, simulation and analysis of an advanced mono-voltage DC converter-based electrical railway power supply system for high speed lines,” in *2017 IEEE Vehicle Power and Propulsion Conference (VPPC)*, 2017, pp. 1–5, doi: 10.1109/VPPC.2017.8331002.

[7] A. Verdicchio, P. Ladoux, H. Caron, and C. Courtois, “New medium-voltage DC

railway electrification system," *IEEE Trans. Transp. Electrif.*, vol. 4, no. 2, pp. 591–604, 2018, doi: 10.1109/TTE.2018.2826780.

[8] R. J. Hill, "Electric railway traction. Part 1: Electric traction and DC traction motor drives," *Power Eng. J.*, vol. 8, no. 1, pp. 47–56, 1994, doi: 10.1049/pe:19940105.

[9] K. Segrave, *The electric car in America, 1890-1922: A social history*. McFarland, 2019.

[10] J. L. Sprague, "Frank J. Sprague invents: The constant-speed DC electric motor [History]," *IEEE Power Energy Mag.*, vol. 14, no. 2, pp. 80–96, 2016, doi: 10.1109/MPE.2015.2501085.

[11] R. J. Hill, "Electric railway traction. Part 1. Electric traction and DC traction motor drives," *Power Eng. J.*, vol. 8, no. 1, pp. 47–56, 1994, doi: 10.1049/pe:19940105.

[12] W. D. Middleton, *When the steam railroads electrified*, 2nd ed. Bloomington, Indiana: Indiana University Press, 2002.

[13] U. Behmann and T. Schütte, "Advantages of low frequencies in converter-supplied railway traction power systems," *RTR Rail Technol. Rev.*, vol. 53, pp. 34–37, 2013.

[14] I. Krastev, P. Tricoli, S. Hillmansen, and M. Chen, "Future of electric railways: Advanced electrification systems with static converters for ac railways," *IEEE Electrif. Mag.*, vol. 4, no. 3, pp. 6–14, 2016, doi: 10.1109/MELE.2016.2584998.

[15] R. J. Hill, "Electric railway traction. Part 3. Traction power supplies," *Power Eng. J.*, vol. 8, no. 6, pp. 275–286, 1994, doi: 10.1049/pe:19940604.

[16] P. Leander and S. Ostlund, “A concept for an HVDC traction system,” in *International Conference on Main Line Railway Electrification 1989*, 1989, pp. 169–173.

[17] *Railway applications - Supply voltages of traction systems*. BS EN 50163:2004 + A1:2007, 2007.

[18] ELAND®CABLES, “NR/PS/ELP/00008 19/33kV Graphite Covered MDPE Cable datasheet,” .

[19] C. Stackler, N. Evans, L. Bourserie, F. Wallart, F. Morel, and P. Ladoux, “25 kV–50 Hz railway power supply system emulation for power-hardware-in-the-loop testings,” *IET Electr. Syst. Transp.*, vol. 9, no. 2, pp. 86–92, Jun. 2019, doi: https://doi.org/10.1049/iet-est.2018.5011.

[20] ABB, “Voltage ratings of high power semiconductors,” 5SYA 2051 application note, 2013.

[21] P. S. Jones and C. C. Davidson, “Calculation of power losses for MMC-based VSC HVDC stations,” in *2013 15th European Conference on Power Electronics and Applications (EPE)*, 2013, pp. 1–10, doi: 10.1109/EPE.2013.6631955.

[22] A. Sangwongwanich, A. Abdelhakim, Y. Yang, and K. Zhou, “Chapter 6 - Control of Single-Phase and Three-Phase DC/AC Converters,” F. B. T.-C. of P. E. C. and S. Blaabjerg, Ed. Academic Press, 2018, pp. 153–173.

[23] M. Saeedifard and R. Iravani, “Dynamic performance of a modular multilevel back-to-back HVDC system,” *IEEE Trans. power Deliv.*, vol. 25, no. 4, pp. 2903–2912, 2010.

[24] ABB, “5SNA 1000G650300 HiPak IGBT module,” 5SNA 1000G650300 datasheet, 2018.

[25] ABB, “Applying IGBTs,” 5SYA 2053-04 application note, 2013.

[26] *IEEE Recommended practice and requirements for harmonic control in electric power systems*. IEEE Std 519-2014, 2014.

[27] P. Twomey, “Electricity Specification 217, Issue 3, 33kV Connection up to 90MVA,” Electricity North West Limited, 2020.

[28] I. Krastev, “Advanced power converters for railway traction systems,” PhD thesis, School of Engineering, Department of Electronic, Electrical and Systems Engineering, University of Birmingham, 2019.

[29] I. Krastev and P. Tricoli, “Boost Multilevel Cascade Inverter for hydrogen fuel cell light railway vehicles,” *IEEE Trans. Ind. Electron.*, vol. 69, no. 8, pp. 7837–7847, 2021.

[30] National Instruments, “Guide to Power Electronics Control Application Examples and IP Cores for NI GPIC.” [Online]. Available: https://forums.ni.com/t5/Power-Electronics-Development/Guide-to-Power-Electronics-Control-Application-Examples-and-IP/td-p/3461466.

[31] X. Zhu, H. Hu, H. Tao, Z. He, and R. M. Kennel, “Stability Prediction and Damping Enhancement for MVdc Railway Electrification System,” *IEEE Trans. Ind. Appl.*, vol. 55, no. 6, pp. 7683–7698, 2019, doi: 10.1109/TIA.2019.2916376.

[32] X. Zhu, H. Hu, H. Tao, and Z. He, “Stability analysis of PV plant-tied MVdc railway electrification system,” *IEEE Trans. Transp. Electrif.*, vol. 5, no. 1, pp. 311–323, 2019, doi: 10.1109/TTE.2019.2900857.

[33] X. Yang, H. Hu, Y. Ge, S. Aatif, Z. He, and S. Gao, “An improved droop control strategy for VSC-based MVDC traction power supply system,” *IEEE Trans. Ind. Appl.*, vol. 54, no. 5, pp. 5173–5186, 2018.

[34] S. Aatif, H. Hu, X. Yang, Y. Ge, Z. He, and S. Gao, “Adaptive droop control for better current-sharing in VSC-based MVDC railway electrification system,” *J. Mod. Power Syst. Clean Energy*, vol. 7, no. 4, pp. 962–974, 2019, doi: 10.1007/s40565-018-0487-0.

[35] Y. Dai, L. Zhang, G. Liu, Y. Yang, Q. Chen, and D. Xu, “Multi-VSM based fuzzy adaptive cooperative control strategy for MVDC traction power supply system,” *J. Franklin Inst.*, vol. 358, no. 15, pp. 7559–7585, 2021.

[36] P. Simiyu and I. E. Davidson, “MVDC railway traction power systems; state-of-the art, opportunities, and challenges,” *Energies*, vol. 14, no. 14, p. 4156, 2021.

[37] I. Ferencz, D. Petreuș, and P. Tricoli, “A power electronic traction transformer for a medium voltage DC electric railway system,” in *2021 44th International Spring Seminar on Electronics Technology (ISSE)*, 2021, pp. 1–6.

[38] I. Ferencz, D. Petreus, and P. Tricoli, “Converter topologies for MVDC traction transformers,” in *2020 IEEE 26th International Symposium for Design and Technology in Electronic Packaging (SIITME)*, 2020, pp. 362–367, doi: 10.1109/siitme50350.2020.9292214.

[39] I. Ferencz and D. Petreus, “A Power Electronic Traction Transformer Model for a New Medium Voltage DC Electric Railway,” *Adv. Electr. Comput. Eng.*, vol. 21, no. 3, pp. 99–108, 2021.

[40] I. Ferencz, D. Petreuș, and T. Pătărău, “Small-Scale DC PETT Module Prototype for the Novel 25kV MVDC Electric Railway System,” in *2022 IEEE 16th International Conference on Compatibility, Power Electronics, and Power Engineering (CPE-POWERENG)*, 2022, pp. 1–6.

[41] S. Aatif, X. Yang, H. Hu, and Z. He, “Integration of PV and Battery Storage for

Catenary Voltage Regulation and Stray Current Mitigation in MVDC Railways," *J. Mod. Power Syst. Clean Energy*, vol. 9, no. 3, pp. 585–594, 2020.

[42] S. Aatif, H. Hu, F. Rafiq, and Z. He, "Analysis of rail potential and stray current in MVDC railway electrification system," *Railw. Eng. Sci.*, vol. 29, no. 4, pp. 394–407, 2021.

[43] P. Ladoux, J. M. Blaquiere, H. Caron, D. Iannuzzi, and M. Coppola, "New three-wire supply systems for DC electric railways," *IET Electr. Syst. Transp.*, vol. 5, no. 3, pp. 112–119, 2015, doi: 10.1049/iet-est.2014.0029.

[44] H. Shigeeda, H. Morimoto, K. Ito, T. Fujii, and N. Morishima, "Feeding-loss reduction by higher-voltage DC railway feeding system with DC-to-DC converter," *2018 Int. Power Electron. Conf. (IPEC-Niigata 2018 -ECCE Asia)*, pp. 2540–2546, 2018, doi: 10.23919/IPEC.2018.8507567.

[45] R. Vial, D. Riu, and N. Retière, "Simulating calculations and optimization design of a new HVDC supply power for light rail system," in *IECON 2010 - 36th Annual Conference on IEEE Industrial Electronics Society*, 2010, pp. 2364–2369, doi: 10.1109/IECON.2010.5675339.

[46] A. Hinz, M. Stieneker, and R. W. De Doncker, "Impact and opportunities of medium-voltage DC grids in urban railway systems," in *2016 18th European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)*, 2016, pp. 1–10, doi: 10.1109/EPE.2016.7695410.

[47] L. Abrahamsson, T. Kjellqvist, and S. Ostlund, "High-voltage DC-feeder solution for electric railways," *IET Power Electron.*, vol. 5, no. 9, pp. 1776–1784, 2012, doi: 10.1049/iet-pel.2011.0219.

[48] J. Laury, M. Bollen, L. Abrahamsson, and S. Östlund, "Some benefits of an

HVDC feeder solution for railways," in *NORDAC 2014*, 2014, doi: 10.13140/RG.2.1.3686.4163.

[49] J. Laury, L. Abrahamsson, and S. Östlund, "OPF for an HVDC feeder solution for railway power supply systems," in *13th International Conference on Design and Operation in Railway Engineering (COMPRAIL 2012)*, 2012, doi: 10.13140/RG.2.1.2856.8486.

[50] X. He, J. Peng, P. Han, Z. Liu, S. Gao, and P. Wang, "A novel advanced traction power supply system based on modular multilevel converter," *IEEE Access*, vol. 7, pp. 165018–165028, 2019, doi: 10.1109/ACCESS.2019.2949099.

[51] D. Laousse, C. Brogard, H. Caron, and C. Courtois, "Direct current - A future under which conditions?," Société Nationale ses Chemins de fer Français (SNCF), May 2016.

[52] J. Fabre, J. Blaquière, A. Verdicchio, P. Ladoux, and S. Sanchez, "Characterization in ZVS mode of SiC MOSFET modules for MVDC applications," in *2019 International Conference on Clean Electrical Power (ICCEP)*, 2019, pp. 470–477, doi: 10.1109/ICCEP.2019.8890157.

[53] A. Verdicchio, P. Ladoux, H. Caron, and S. Sanchez, "Future DC railway electrification system - Go for 9 kV," in *2018 IEEE International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles & International Transportation Electrification Conference (ESARS-ITEC)*, 2018, pp. 1–5, doi: 10.1109/ESARS-ITEC.2018.8607304.

[54] H. J. Kaleybar, M. Brenna, and F. Foiadelli, "Compatibility of Present 3 kV DC and 2× 25 kV AC High-Speed Railway Power Supply Systems Towards Future MVDC System," in *2021 12th Power Electronics, Drive Systems, and*

Technologies Conference (PEDSTC), 2021, pp. 1–6.

[55] M. P. Badjor, “Energy effectiveness and electromagnetic compatibility of DC traction power supply systems with 24-kV grid voltage,” *Russ. Electr. Eng.*, vol. 82, no. 8, p. 416, 2011, doi: 10.3103/S1068371211080037.

[56] M. P. Bader and E. V Sachkova, “Adaptation of a traction DC power system for high-speed traffic,” *Russ. Electr. Eng.*, vol. 88, no. 9, pp. 573–578, 2017, doi: 10.3103/S1068371217090024.

[57] P. Simiyu and I. E. Davidson, “Modeling and simulation of MVDC traction power system for high-speed rail transportation,” in *2021 IEEE PES/IAS PowerAfrica*, 2021, pp. 1–5.

[58] G. Asplund, K. Eriksson, and K. Svensson, “DC transmission based on voltage source converters,” in *CIGRE SC14 Colloquium, South Africa*, 1997, pp. 1–7.

[59] G. Asplund, “Application of HVDC Light to power system enhancement,” in *2000 IEEE Power Engineering Society Winter Meeting. Conference Proceedings (Cat. No. 00CH37077)*, 2000, vol. 4, pp. 2498–2503.

[60] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, “A review of three-phase improved power quality AC-DC converters,” *IEEE Trans. Ind. Electron.*, vol. 51, no. 3, pp. 641–660, 2004, doi: 10.1109/TIE.2004.825341.

[61] T. Larsson, A. Petersson, A. Edris, D. Kidd, and F. Aboytes, “Eagle Pass back-to-back tie: a dual purpose application of voltage source converter technology,” in *2001 Power Engineering Society Summer Meeting. Conference Proceedings (Cat. No.01CH37262)*, 2001, vol. 3, pp. 1686–1691 vol.3, doi: 10.1109/PESS.2001.970329.

[62] Y. Chen, Z. Li, S. Zhao, X. Wei, and Y. Kang, “Design and implementation of a modular multilevel converter with hierarchical redundancy ability for electric ship MVDC system,” *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 5, no. 1, pp. 189–202, 2016.

[63] S. Du, A. Dekka, B. Wu, and N. Zargari, *Modular multilevel converters: analysis, control, and applications*. John Wiley & Sons, 2017.

[64] J. Ranneberg, “Transformerless topologies for future stationary AC-railway power supply,” in *2007 European Conference on Power Electronics and Applications*, 2007, pp. 1–11.

[65] V. Gelman, “Insulated-gate bipolar transistor rectifiers: Why they are not used in traction power substations,” *IEEE Veh. Technol. Mag.*, vol. 9, no. 3, pp. 86–93, 2014, doi: 10.1109/MVT.2014.2333762.

[66] S. Milovanović, S. Strobl, P. Ladoux, and D. Dujić, “Hardware-in-the-Loop Modeling of an Actively Fed MVDC Railway Systems of the Future,” *IEEE Access*, vol. 9, pp. 151493–151506, 2021.

[67] M. Hagiwara, R. Maeda, and H. Akagi, “Control and analysis of the Modular Multilevel Cascade Converter based on Double-Star Chopper-Cells (MMCC-DSCC),” *IEEE Trans. Power Electron.*, vol. 26, no. 6, pp. 1649–1658, 2010.

[68] G. J. M. de Sousa, A. d. S. Dias, J. A. Alves, and M. L. Heldwein, “Modeling and control of a modular multilevel converter for medium voltage drives rectifier applications,” in *2015 IEEE 24th International Symposium on Industrial Electronics (ISIE)*, 2015, pp. 1080–1087, doi: 10.1109/ISIE.2015.7281622.

[69] U. Javaid, A. Christe, F. D. Freijedo, and D. Dujic, “Interactions between bandwidth limited CPLs and MMC based MVDC supply,” in *2017 IEEE Energy*

Conversion Congress and Exposition (ECCE), 2017, pp. 2679–2685, doi: 10.1109/ECCE.2017.8096504.

[70] D. Li, "Efficient generation of power in medium voltage direct current systems: variable speed operation and rectifier considerations," Ph.D. dissertation, University of South Carolina, USA, 2013.

[71] M. M. Steurer *et al.*, "Multifunctional megawatt-scale medium voltage DC test bed based on modular multilevel converter technology," *IEEE Trans. Transp. Electrif.*, vol. 2, no. 4, pp. 597–606, 2016, doi: 10.1109/TTE.2016.2582561.

[72] M. Utvić, S. Milovanović, and D. Dujić, "Flexible medium voltage DC source utilizing series connected modular multilevel converters," in *2019 21st European Conference on Power Electronics and Applications (EPE'19 ECCE Europe)*, 2019, pp. 1–9.

[73] A. Nami, J. Liang, F. Dijkhuizen, and G. D. Demetriades, "Modular multilevel converters for HVDC applications: Review on converter cells and functionalities," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 18–36, 2014.

[74] M. M. C. Merlin *et al.*, "The alternate arm converter: A new hybrid multilevel converter with DC-fault blocking capability," *IEEE Trans. Power Deliv.*, vol. 29, no. 1, pp. 310–317, 2014, doi: 10.1109/TPWRD.2013.2282171.

[75] B. Singh, S. Gairola, B. N. Singh, A. Chandra, and K. Al-Haddad, "Multipulse AC–DC converters for improving power quality: A review," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 260–281, 2008, doi: 10.1109/TPEL.2007.911880.

[76] V. Gelman, "Thyristor Controlled Rectifiers (TCR) for traction - Problems and solutions," *2013 3rd Int. Conf. Electr. Power Energy Convers. Syst. EPECS 2013*, vol. 500, pp. 0–5, 2013, doi: 10.1109/EPECS.2013.6713078.

[77] T. Suzuki, “DC power-supply system with inverting substations for traction systems using regenerative brakes,” *IEE Proc. B - Electr. Power Appl.*, vol. 129, no. 1, pp. 18–26, 1982, doi: 10.1049/ip-b.1982.0002.

[78] P. H. Henning, H. D. Fuchs, A. D. le Roux, and H. d. T. Mouton, “A 1.5-MW seven-sell series-stacked converter as an active power filter and regeneration converter for a DC traction substation,” *IEEE Trans. Power Electron.*, vol. 23, no. 5, pp. 2230–2236, 2008, doi: 10.1109/TPEL.2008.2001882.

[79] O. E. Oni, I. E. Davidson, and K. N. I. Mbangula, “A review of LCC-HVDC and VSC-HVDC technologies and applications,” in *2016 IEEE 16th International Conference on Environment and Electrical Engineering (EEEIC)*, 2016, pp. 1–7, doi: 10.1109/EEEIC.2016.7555677.

[80] J. Liang, A. Nami, F. Dijkhuizen, P. Tenca, and J. Sastry, “Current source modular multilevel converter for HVDC and FACTS,” in *2013 15th European Conference on Power Electronics and Applications (EPE)*, 2013, pp. 1–10, doi: 10.1109/EPE.2013.6634735.

[81] R. A. Mastromauro, S. Pugliese, and S. Stasi, “An advanced active rectifier based on the single-star bridge cells modular multilevel cascade converter for more-electric-aircrafts applications,” in *2015 International Conference on Electrical Systems for Aircraft, Railway, Ship Propulsion and Road Vehicles (ESARS)*, 2015, pp. 1–6, doi: 10.1109/ESARS.2015.7101421.

[82] D. Bosich, R. A. Mastromauro, and G. Sulligoi, “AC-DC interface converters for MW-scale MVDC distribution systems: A survey,” in *2017 IEEE Electric Ship Technologies Symposium (ESTS)*, 2017, pp. 44–49, doi: 10.1109/ESTS.2017.8069258.

[83] S. Sharifi, T. Kamel, and P. Tricoli, “Investigating the best topology for Traction Power Substations (TPSs) in a Medium Voltage DC (MVDC) railway electrification system,” *23rd European Conference on Power Electronics and Applications (EPE’21),* Aug-2021.

[84] S. Sharifi and P. Tricoli, “Assessment of performance for MVDC electrification systems,” Technical deliverable D1.2 -Flexible medium voltage DC electric railway systems (MVDC-ERS) project, 2021.

[85] S. Sayed and A. Massoud, “Minimum transmission power loss in multi-terminal HVDC systems: A general methodology for radial and mesh networks,” *Alexandria Eng. J.*, vol. 58, no. 1, pp. 115–125, 2019.

[86] P. Rodriguez and K. Rouzbehi, “Multi-terminal DC grids: challenges and prospects,” *J. Mod. Power Syst. Clean Energy*, vol. 5, no. 4, pp. 515–523, 2017.

[87] D. Van Hertem and M. Ghandhari, “Multi-terminal VSC HVDC for the European supergrid: Obstacles,” *Renew. Sustain. energy Rev.*, vol. 14, no. 9, pp. 3156–3163, 2010.

[88] Y. Zhang, J. Ravishankar, J. Fletcher, R. Li, and M. Han, “Review of modular multilevel converter based multi-terminal HVDC systems for offshore wind power transmission,” *Renew. Sustain. Energy Rev.*, vol. 61, pp. 572–586, 2016, doi: https://doi.org/10.1016/j.rser.2016.01.108.

[89] M. H. Nguyen, T. K. Saha, and M. Eghbal, “Hybrid multi-terminal LCC HVDC with a VSC Converter: A case study of Simplified South East Australian system,” in *2012 IEEE Power and Energy Society General Meeting*, 2012, pp. 1–8.

[90] L. Ding, Y. Lian, and Y. W. Li, “Multilevel current source converters for high

power medium voltage applications," *CES Trans. Electr. Mach. Syst.*, vol. 1, no. 3, pp. 306–314, 2017.

[91] J. E. Huber and J. W. Kolar, "Solid-State Transformers," *IEEE Ind. Electron. Mag.*, vol. 10, no. September, pp. 19–28, 2016, doi: 10.1109/MIE.2016.2588878.

[92] S. Norrga, "A soft-switched bi-directional isolated AC/DC converter for AC-fed railway propulsion applications," *IEE Conf. Publ.*, no. 487, pp. 433–438, 2002, doi: 10.1049/cp:20020156.

[93] T. Kjellqvist, S. Norrga, and S. Ostlund, "Design considerations for a medium frequency transformer in a line side power conversion system," in *2004 IEEE 35th Annual Power Electronics Specialists Conference (IEEE Cat. No. 04CH37551)*, 2004, vol. 1, pp. 704–710.

[94] M. Glinka and R. Marquardt, "A new AC/AC multilevel converter family," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 662–669, 2005.

[95] a Lesnicar and R. Marquardt, "A new modular voltage source inverter topology," *Eur. Power Electron. Conf.*, 2003.

[96] J. Feng, W. Q. Chu, Z. Zhang, and Z. Q. Zhu, "Power electronic transformer-based railway traction systems: Challenges and opportunities," *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 5, no. 3, pp. 1237–1253, 2017, doi: 10.1109/JESTPE.2017.2685464.

[97] J. Taufiq, "Power electronics technologies for railway vehicles," in *2007 Power Conversion Conference-Nagoya*, 2007, pp. 1388–1393.

[98] J. Winter, T. Schirmer, A. Iraklis, A. Lusiewicz, and H. Dittus, "Overview of three-stage power converter topologies for medium frequency-based railway

vehicle traction systems," *IEEE Trans. Veh. Technol.*, vol. PP, no. c, pp. 1–1, 2019, doi: 10.1109/tvt.2019.2895500.

[99] C. Zhao *et al.*, "Power electronic traction transformer-medium voltage prototype," *IEEE Trans. Ind. Electron.*, vol. 61, no. 7, pp. 3257–3268, 2014, doi: 10.1109/TIE.2013.2278960.

[100] C. Zhao *et al.*, "Power Electronic Transformer (PET) converter: Design of a 1.2MW demonstrator for traction applications," *SPEEDAM 2012 - 21st Int. Symp. Power Electron. Electr. Drives, Autom. Motion*, pp. 855–860, 2012, doi: 10.1109/SPEEDAM.2012.6264496.

[101] G. Fortes, P. Ladoux, J. Fabre, and D. Flumian, "Characterization of a 300 kW isolated DCDC converter using 3.3 kV SiC-MOSFETs," in *PCIM Europe digital days 2021; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, 2021, pp. 1–8.

[102] J. Fabre *et al.*, "Characterization and implementation of resonant isolated DC/DC converters for future MVdc railway electrification systems," *IEEE Trans. Transp. Electrif.*, vol. 7, no. 2, pp. 854–869, 2021, doi: 10.1109/TTE.2020.3033659.

[103] M. Mogorovic and D. Dujic, "Sensitivity Analysis of Medium-Frequency Transformer Designs for Solid-State Transformers," *IEEE Trans. Power Electron.*, vol. 34, no. 9, pp. 8356–8367, 2019, doi: 10.1109/TPEL.2018.2883390.

[104] F. Battal, S. Balci, and I. Sefa, "Power electronic transformers: A review," *Meas. J. Int. Meas. Confed.*, vol. 171, no. December 2020, p. 108848, 2021, doi: 10.1016/j.measurement.2020.108848.