CRYOGENIC CHARACTERISTICS OF IGBTs

by

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Abstract

Applications are now starting to emerge for superconducting devices in the areas of electrical power conversion and management, for example superconducting windings for marine propulsion motors, superconducting fault current limiters and superconducting magnet energy storage (SMES). Many of these applications also require power electronics, and it is therefore timely to consider the possibility of locating the power electronics in the cryo-system with the superconducting devices. Although significant work has been undertaken on the cryogenic operation of small devices, little has been published on larger devices, particularly the IGBT. This therefore forms the focus of this study.

To examine the cryogenic performance of the sample devices, a cryo-system consisting of a cold chamber, a helium-filled compressor and vacuum pumps was built. Static, gate charge and switching tests were carried out on three types of IGBT modules, PT (punch-through), NPT (non-punch-through) and IGBT3 respectively, in the temperature range of 50 to 300 K. The switching tests were undertaken at 600V and up to 110 A.

A physically based, compact level-1 model was selected to model the cryogenic performance of the IGBTs. A generic Saber power diode model with reverse recovery was selected to model the diode cryogenic performance. Close correspondence was demonstrated between the models and experimental results over the temperature range of 50- 300 K.

Saber simulation was used to examine the cryogenic performance of a DC-DC step-down converter and a pulse-width modulated inverter leg, in which the temperature-dependent power device models developed in the modelling work were used. The simulation results

showed that standard power electronic circuits using standard devices could work much more efficiently at low temperatures, for example, the efficiency of the DC-DC converter working at 50 kHz being increased from 90.0% at room temperature to 97.0% at 50 K.

Dedicated to Ruohui Yang and my parents!

Acknowledgement

Contents

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List of Abbreviations and Symbols

Abbreviation	Complete forms
AC	Alternating Current
BJT	Bipolar Junction Transistor
DC	Direct Current
EMC	Electromagnetic Compatibility
HTS	High Temperature Superconductor
IGBT	Insulated Gate Bipolar Transistor
kW	kilo Watt
LDMOS	Lateral double-diffused MOSFET
LTS	Low Temperature Superconductor
MISFET	Metal Insulator Semiconductor Field-Effect Transistors
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MRI	Magnetic Resonance Imaging.
MW	Mega Watt
NPT	Non-Punch Through
ppm	parts per million
PT	Punch Through
PWM	Pulse Width Modulation
RF	Radio Frequency
rpm	revolutions per minute
SMES	Superconducting Magnetic Energy Storage
VMOS	V-groove double-diffused MOSFET
VDMOS	Vertical double-diffused MOSFET

Symbol	Description	Unit
A	Total active area of an IGBT	cm^2
A_{CE}	Collector emitter overlap area of an IGBT	cm^2
A_{GC}	Gate collector overlap area of an IGBT	cm^2
B	Mobility ratio μ_n/μ_p	-
BV_n	Breakdown voltage index	-
C_{CE}	Collector- emitter oxide capacitance of an IGBT	F
C_f	Capacitance in the low-pass filter for the buck converter	F
C_{GE}	Gate- emitter capacitance of an IGBT	F
$C_{GC, ACT}$	Actual gate collector capacitance of an IGBT	F
C_{GC}	Gate collector capacitance of an IGBT from the gate charge test	F
C_0	Diode junction capacitance under zero bias	F
C_{OX}	Capacitance per unit area of gate oxide	$F\ cm^{-2}$
C_j	Junction capacitance corresponding to a junction voltage V_j in a diode	F
D	Duty ratio	-
d	Half length of the i-region in an PiN diode	cm
D_a	Ambipolar diffusion coefficient	$cm^2\ s^{-1}$
d_N	N⁻ drift region width in an IGBT	cm

di_r/dt	Reverse current gradient during a diode turn off transient	A/ns
e	Elementary charge, 1.60×10^{-19}	C
E_{on}	Switch-on energy loss	J
E_{off}	Switch -off energy loss	J
f_1	Fundamental frequency	Hz
f_s	Switching frequency in a converter	Hz
f_c	Corner frequency of an low pass filter	Hz
f_{cmax}	Max value for the corner frequency	Hz
g_{ms}	IGBT transconductance	S
i_{CE}	IGBT collector- emitter current	A
I_{CE}	IGBT collector- emitter steady-state current	A
$I_{CE}(0)$	IGBT collector- emitter current value after initial drop during a turn-off transient	A
$I_{CE(ON)}$	IGBT collector- emitter on-state current	A
$I_{CE, sat}$	IGBT saturated collector- emitter current	A
$i_{CE}(t)$	IGBT tail current	A
I_{MOS}	MOS component current in an IGBT	A
I_{PiN}	PiN component current in an IGBT	A
I_d	Diode current	A
I_e	The electron current component in an IGBT	A
$I_{e,lin}$	The linear electron current component in an IGBT	A
$I_{e,sat}$	The saturate electron current component in an IGBT	A
I_F	Diode forward current during on-state	A
I_{FO}	Diode forward current before turn off process	A
I_{GE}	Gate-emitter current	A
I_h	The hole current component in an IGBT	A
i_L	Inductor current	A
I_L	Average value of the inductor current	A
I_{rrm}	Diode peak reverse recovery current	A
I_R	Reverse bias current	μA
I_S	Diode reverse leak current	A
k	Boltzmann constant, $1.3806503 \times 10^{-23}$	J K^{-1}
J_C	Collector current density in an IGBT	A cm^{-2}
J_{PiN}	Current density in the PiN component of an IGBT	A cm^{-2}
J_{MOS}	Current density in the MOS component of an IGBT	A cm^{-2}
K	Parameter for the voltage controlled current source in the diode reverse recovery model	-
K_{plin}	Transconductance in the linear region	A V^{-2}
K_{psat}	Transconductance in the saturation region	A V^{-2}
l	Length of bus bars	cm
L	Inductor used in the diode reverse recovery model	H
L_t	Total stray inductance of two bus bars	H
L_i	Internal inductance of two bus bars	H
L_e	External inductance of two bus bars	H
L_f	Inductance in the low-pass filter for the buck converter	H
L_a	Ambipolar diffusion length	cm
L_p	Minority carrier diffusion length	cm
L_{CH}	The gate channel length for an IGBT or MOSFET	cm

M	Avalanche multiplication coefficient	-
m_a	Depth of amplitude modulation	-
m_f	Depth of frequency modulation	-
n	Electron concentration	cm^{-3}
$n(+d)$	Electron concentration at –d end in the i-region of a PiN diode	cm^{-3}
$n(-d)$	Electron concentration at +d end in the i-region of a PiN diode	cm^{-3}
N_d	Doping concentration in the drift region	cm^{-3}
n_{eff}	Emitter efficiency	%
n_i	Intrinsic carrier concentration	cm^{-3}
p	Hole concentrations	cm^{-3}
Q_{CE}	Collector-emitter charge	C
Q_{GC}	Gate-collector charge	C
Q_{GE}	Gate-emitter charge	C
$Q_{GE(th)}$	Threshold gate-emitter charge	C
Q_{rr}	Diode reverser recovery charge	C
R	Buck converter load	Ω
R_C	Collector resistance	Ω
R_E	Emitter resistance	Ω
R_G	Gate resistance	Ω
R_L	Resistor used in the diode reverse recovery model	Ω
R_{on}	Diode on state resistance	Ω
S	Snappiness factor	-
T	Absolute temperature	K
t	Time	s
t_s	The moment at which the diode reverse current reaches its peak value	s
t_3	Time duration for the diode current dropping from on-state to zero	s
t_4	Time duration for the diode current dropping from zero to the peak reverse current	s
t_5	Time duration for the diode current reverse recovering from the peak reverse current to its 10% value	s
t_{on}	Time duration when the converter switch is on	s
t_{off}	Time duration when the converter switch is off	s
T_S	Converter switching time period	s
t_{rr}	Diode reverse recovery time	s
V_B	Breakdown voltage	V
V_{bi}	Junction built- in potential	V
V_1	Voltage between the collector-gate depletion region	V
V_2	Voltage between the collector-emitter depletion region	V
V_b	Junction barrier potential in a diode	V
V_{CC1}	Voltage across the collector resistor used in the IGBT model	V
V_{CC}	Power supply voltage amplitude	V
V_{CE}	Collector- emitter voltage	V
$V_{control}$	Amplitude of the control signal for PWM	V
V_{dc}	DC input voltage for an converter or inverter leg	V
V_d	Diode voltage	V
V_{diode}	Voltage across the temperature sensor diode	V

V_{EE1}	Voltage across the emitter resistor used in the IGBT model	V
V_F	On-state voltage drop of an IGBT	V
V_{FP}	Overshoot voltage during a PiN diode turn-on transient	V
V_{GC}	Gate-collector voltage	V
V_{GG1}	Voltage across the gate resistor used in the IGBT model	V
V_{GE}	Gate-emitter voltage for an IGBT	V
$V_{GE(th)}$	Gate-emitter threshold voltage	V
V_{GP}	Gate voltage necessary for the device to conduct a full load current	V
V_j	Diode junction voltage	V
v_L	Instantaneous voltage across the inductor in the buck converter	V
V_L	Voltage across the inductor in the diode reverse recovery model	V
V_M	Voltage drop across the i- region of a PiN diode	V
V_m	Maximum reverse blocking voltage of the IGBT N- drift region	V
V_{MOS}	Voltage drop across the MOSFET component of an IGBT	V
V_{N+}	Voltage drop across the N+ region in a PiN diode	V
V_{on}	Diode turn- on voltage, corresponding to a current of 1 A	V
v_{oi}	Instantaneous value for the converter output voltage before the low-pass filter	V
$(V_{oi})_1$	Fundamental frequency amplitude of the converter output voltage	V
V_o	The amplitude of the converter output voltage	V
v_o	Instantaneous value for the converter output voltage	V
V_{OFF}	Collector emitter offset voltage for an IGBT	V
V_{out}	Output voltage signal in the temperature regulation circuit	V
V_{P+}	Voltage drop across the P+ region in an PiN diode	V
V_{PiN}	Voltage across the PiN component of an IGBT	V
V_{Ref}	Reference voltage used in the temperature regulation circuit	V
v_s	Carrier saturation velocity	cm s^{-1}
V_{set}	Temperature demand voltage signal in the temperature regulation circuit	V
V_R	Diode reverse blocking voltage	V
V_{rr}	Reverse recovery peak voltage across a diode	V
V_{TC}	Threshold voltage for the accumulation layer in an IGBT or MOSFET	V
V_T	Gate threshold voltage for an IGBT or MOSFET	V
V_{tri}	Amplitude of the triangular signal for PWM	V
W	Width of the bus bars	cm
W	Gate width for an IGBT or MOSFET	cm
W_{CE}	Collector-emitter depletion width	cm
W_{GC}	Collector-gate depletion depth	cm
x_d	Geometric mean distance between bus bars	cm
Z	Gate depth for an IGBT or MOSFET	cm
Z_L	Impedance of the inverter load	Ω

α_{PNP}	Common-base current gain of a transistor	-
β_{PNP}	Common-emitter current gain of a transistor	-
γ	Carrier injection efficiency	-

ΔV_o	Peak to peak voltage ripple	V
ΔQ	Additional charge on the capacitor in the low pass filter for the bulk converter	C
ΔI_L	Amplitude of the ripple current through the inductor in the low pass filter for the bulk converter	H
ε_0	Vacuum permittivity 8.85×10^{-14}	F cm^{-1}
ε_{Si}	Relative permittivity of silicon	11.90
θ	Transverse field factor	V^{-1}
λ	Channel length modulation parameter	V^{-1}
μ_0	Permeability in vacuum	H cm^{-1}
μ_r	Relative permeability in dielectric	-
μ_n	Electron mobility	cm^2/V-s
μ_{ns}	Surface mobility of the gate channel for an IGBT or MOSFET	cm^2/V-s
μ_p	Hole Mobility	cm^2/V-s
τ	Carrier lifetime	s
τ_a	Minority carrier life time	s
τ_B	Base transit time	s

Chapter 1 Introduction and literature review

1. 1 Introduction

Power electronics involves the conversion of electric power from one frequency, voltage and current level to another, and has become widely used since the 1960s. This technology is now a major part of power engineering: at least 25% of all power generated passes through some form of power electronic system before being utilized [1-1].

However, the room-temperature operation of power electronics is a matter of convenience, not optimisation. Lowering the operating temperature improves the performance and greatly reduces the disruptive effects of thermal energy. The supercooling of power electronics, though inconvenient, is therefore being considered more frequently as a means of boosting performance, especially in applications where a cryocooling system already exists, that is, in superconductor applications. In recent years, rapid advances in high temperature superconductors (HTS) increase the prospects for the development of cryogenic power electronics [1-1].

1. 2 Cryogenic power applications

The interest in applying superconductivity to power applications is motivated by expectations of improved performance in terms of size, weight and efficiency over conventional room-temperature devices. Use of superconducting wire or tape in power generators or large magnets, for example, provides the ability to transport large DC currents with no measurable resistive losses [1-2].

The early low temperature superconductors (LTS) that operated in liquid helium spurred the development of many prototypes for generators, motors, transmission lines, and energy storage magnets. However, all of these demonstrations were compromised by the costly and technologically complicated requirement for liquid helium, and were not easily accepted by utilities or end-users [1-2].

In 1986, the discovery of high temperature superconductors provided new impetus for pursuing cryogenic power applications because of the prospect for higher temperature operation at liquid nitrogen (77 K) temperatures or above. With higher temperatures come not only reduced refrigeration costs but also enhanced reliability [1-3, 4]. There have been many activities in the field of developing high temperature superconductor wires and cables [1-5, 6, 7].

Trends indicate that the availability of high temperature superconductors continues to increase and the cost continues to go down. Therefore they are expected to be utilized in many industrial areas, which include magnetic resonance imaging, rotating machinery, high voltage transmission, superconducting magnetic energy storage, transformers, fault current limiters, space power applications. These applications will be reviewed in the following subsections.

1. 2. 1 Magnetic resonance imaging (MRI)

MRI is based on the principle of nuclear magnetic resonance, a spectroscopic technique used to obtain microscopic chemical and physical information about molecules. MRI has become

an important medical tool for visualizing soft tissues within the human body since the early 1980s [1-8, 9].

Superconductivity came into MRI from the very beginning of this technology in 1984. This is because the early resistive magnets could only achieve a rather low magnetic field around 0.15 Tesla and had poor homogeneity. A high magnetic field, uniform both in time and space, is required and is easy to achieve with a superconducting magnet [1-1, 10].

With HTS, the MRI system could work more efficiently and cheaply. The next generation MRI systems will be made with high temperature superconductors though HTS materials are still expensive [1-11].

1. 2. 2 Rotating machinery

Superconducting rotating machines have looked promising since multifilament niobium–titanium (NbTi) superconductors became available in the mid-1960s. Both DC homopolar and AC synchronous machines were successfully tested from the 1970s to the 1990s. Three different 70-MW generators were demonstrated by the SuperGM project in Japan. However, economic considerations did not make these machines commercially attractive [1-12].

The advantage of high temperature superconductors has provided new impetus to the development of superconducting rotating machines for commercial applications. Currently, large high-torque ship propulsion motors, large generator prototypes, and synchronous condensers are under development and are expected to be commercially available in the next few years. The prospects for improved life cycle cost, smaller size, less weight, and higher

efficiency benefits are providing incentives for the development of these larger rating HTS machines [1-12]. Four superconducting rotating machine programmes are in progress in the US. General Electric is building a 100 MVA superconducting generator under a DoE (the US Department of Energy) contract. American Superconductor has 3 programmes on superconducting machines - a 10 MVAR superconducting synchronous condenser, a 5 MW, 230-rpm ship propulsion motor for Office of Naval Research (ONR) and a 36.5 MW, 120-rpm ship propulsion motor programme also for ONR. All superconducting machines employ high temperature superconductors in the field winding on the rotor and a conventional ambient temperature copper winding in the stator [1-13].

1. 2. 3 High voltage transmission cables

With the rapid growth of electric power demand and environmental concerns in the 1970s, major programs on underground superconducting transmission cables were initiated in the hope of reducing or eliminating the 4% power loss in the conventional power transmission lines. The most ambitious one, also being the one that proceeded furthest, was the 200 m long AC transmission line at Brookhaven National Laboratory on Long Island, New York [1-14]. The full power testing of the prototype system in 1986 confirmed the technical feasibility [1-15]. However, many of the superconducting power transmission cable projects including this one were cancelled for economic reasons.

The discovery of high-temperature superconductivity rekindled interest in superconducting power transmission cables. In February 2000, the first industrial HTS power cable operation in Carrollton, Georgia was announced, which utilized three single-phase, 30-m long cables carrying 1250 A at 12.5 kV [1-16].

Prototype or industrial HTS cable projects were carried out in many industrial countries, until 2003. The applications ranged from 12.5 to 225 kV. Most projects were AC and used the HTS material BSCCO-2223, which has a transition temperature of around 110 K, so liquid nitrogen could be used as the coolant [1-14].

The present price of HTS cable is still well above the target price, $10 per kA-m for the HTS tapes proposed by DoE [1-14]. However, the cost of the cable itself may be insignificant compared with the other cost issues for a particular application. For instance, using HTS cable, the capacity of urban distribution lines could be upgraded without increasing voltage levels and adding new transformers, which is very important to very crowded urban areas [1-14]. Superconducting power transmission cables could have a very significant impact on the power industry.

1. 2. 4 Superconducting Magnet Energy Storage (SMES)

SMES systems use superconducting coils to store electrical energy by keeping a DC current flowing through a lossless superconducting loop in a liquid cryogen tank. Electrical energy is stored in the system by converting the input AC current into DC, and feeding it into the superconducting coil. The withdrawal of energy is accomplished by switching the current through an alternate path, which converts the DC to AC and supplies the grid [1-1].

SMES was initially conceived in the 1970s as a load-levelling device, that is, to store energy in bulk to smooth a utility's daily peak power demand [1-17, 18]. A 30 MJ SMES operated in the power grid in 1982-83 [1-19]. However, the cost of SMES is too high compared with fossil fuel-based peaking generation [1-20].

Due to its rapid response (milliseconds), high power (megawatts) and high efficiency, SMES was identified as a candidate technology to improve transmission stability, frequency control and power quality at power and energy levels of 20-200 MW and 50-500 MJ [1-21]. In the long term, energy storage, SMES in particular, may play an important role in a new deregulated power market with more renewable energy resources [1-20].

1. 2. 5 Power transformers

In a conventional power transformer, load losses represent approximately 80% of total losses. Of the load losses, 80% are I^2R losses and the remaining 20% consists of stray and eddy current losses [1-2]. To date, efforts to reduce load losses have been directed toward the latter. Unlike copper and aluminium, superconductors present no resistance to the flow of DC electricity, with the consequence that I^2R losses become essentially zero, thereby creating the potential for a dramatic reduction in overall losses. In AC operation, the superconductor in an HTS transformer experiences a type of eddy current loss, which is extremely small in comparison to the energy loss in conventional materials. Even with the added cost of refrigeration, HTS transformers in the 10 MVA and higher ranges are projected to be substantially more efficient and less expensive than their conventional counterparts [1-2].

The benefits of smaller weight and size are expected to be major factors in the early introduction of HTS transformers in Japan. In Europe there is growing interest in using compact HTS on-board transformers in high-speed trains [1-2, 22, 23].

1. 2. 6 Fault current limiters

Superconducting fault current limiters normally operate with low impedance and are "invisible" components in the electrical system. In the event of a fault, the limiter inserts impedance into the circuit and limits the fault current [1-2]. A high critical current density, probably at least 10^5 A/cm^2, will likely be required to achieve adequate switching speed and an acceptable superconductor volume [1-4].

The development of high temperature superconductors enables the development of economical fault current limiters. Fault current limiters can be applied in a number of distribution or transmission areas: in the main position to protect the entire bus; in the feeder position to protect an individual circuit on the bus; and in the bus-tie position to protect the unfaulted bus [1-2]

The most extensive FCL program in Japan has been the collaboration between TEPCO (Tokyo Electric Power Corporation) and Toshiba. The long-term goal of this program is the development of a 500 kV limiter with a rated current of 8,000 A. Initial development has been focused on a distribution-level limiter designed for 6.6 kV. Introduction of a transmission-level FCL on the grid is anticipated around 2010. By far the most comprehensive FCL program in Europe is that being conducted by the collaboration between Electricité de France, GEC Alsthom, and Alcatel Alsthom Recherche. The program's main goal is to provide FCLs for the 225 kV grid in France [1-2].

1. 2. 7 Space power applications

Planetary exploration missions and deep space probes require electrical power management and control systems that are capable of efficient and reliable operation in very cold

environments. Presently spacecrafts carry radioisotope heating units to maintain the on-board electrical and electronic systems at near room temperature. Systems capable of operating at cryogenic temperatures will not only contribute to increasing efficiency, and improving the reliability, but also reduce the system size by eliminating or reducing the heating units [1-24, 25]. Cryogenic programs have been carried out with the support from NASA, Department of Defense (DoD) and the Air Force in the US [1-24, 25, 26].

Cryogenic refrigerator and cryogenic integration programs have been reported by the Cryogenic Technologies Group, Space Vehicles Directorate of the Air Force Research Laboratory in the United States. The objective was to develop and demonstrate space cryogenic technologies required to meet future requirements for Air Force and DoD missions. A variety of cryocoolers were pursued to meet various requirements, and several advanced cryogenic integration technologies were developed to meet the reduction in cryogenic system integration penalties and design time [1-26].

Meanwhile, research and development activities on low temperature electronic devices and systems have been carried out from room temperature down to around –190 °C at the NASA Glenn Research Centre. The goal was to develop and demonstrate reliable and efficient power conversion techniques capable of surviving and exploiting the advantages of low temperature environments. The target systems included converters, inverters, controls, digital circuits and special-purpose circuits. Initial development efforts have produced the successful demonstration of low temperature operation and cold-restart of several DC/DC converters (with outputs from 5 to 1000 W) using different design topologies. Some of these circuits employed superconducting inductors [1-25].

Apart from industrial power applications, cryogenics has found applications in scientific areas, such as magnetohydrodynamics and scientific instrumentation based on the physics of the Josephson effect [1-2].

1. 2. 8 Summary of cryogenic power applications

All the cryogenic applications discussed above require a power supply and power conditioning, which may include converters, PWM (Pulse Width Modulation) control, and other power circuitry. Since all these applications are expected to work in a cryogenic environment, there may be system level benefits if all relevant power devices could also work in the same environment.

Compared with the conventional power system, cryogenic power systems can offer impressive mass, volume and fuel savings, which is very important to space applications [1-27, 28, 29]. The system analysis of a typical power system for a ground based radar application suggested that it was possible to develop a near-term demonstration of a cryogenic radar power system that could offer 50 percent savings in mass and volume, and more than 65 percent savings in fuel consumption in comparison with the conventional power system [1-28]. The evaluation of a 1.5 MW cryogenic power conditioning system for an electric propulsion spacecraft indicated that the system efficiency with the cryogenic MOSFET conversion can be improved from 90.9% to 92.7% [1-27]. With the development of high temperature superconductor technology, the efficiency of cryogenic power systems could be further improved.

The possible benefits of using cryogenic power electronics supplied the motivation to characterise and assess the operation of power devices and power conversion circuits in a cryogenic environment.

1. 3 Review of cryogenic semiconductor physics

The effect of temperature on semiconductor materials and therefore on the performance of power devices have been studied for a long time.

The temperature dependence of semiconductor properties had been noticed and analysed since the very beginning of semiconductor research [1-30, 31, 32 and 33]. However, the low temperature characteristics of power devices was not thought important until the development of field-effect transistors (MOSFET, JFET, MESFET, MODFET) since standard bipolar transistors performed poorly at low temperatures [1-3].

The temperature dependence of carrier lifetime was firstly studied by Shockley, Read and Hall in the 1950s [1-34, 35]. Further studies on the effect of the low temperatures on carrier lifetime were carried out and detailed models were developed to follow the new experimental results [1-36, 37]. An empirical model was recommended in [1-38], which took into account the widest amount of data available at that time.

A complete analytical model of carrier concentration was presented in the 1950s [1-33]. The reduction of carrier concentration at low temperatures was referred to as 'carrier freezeout'. However, this model is very complicated. Based on new experimental results, a more practical model was presented in 1990 [1-34].

The slight increase of silicon bandgap with the reduction of temperature has been an important topic of study since the 1950s. The recent model of silicon band gap variation proposed in 1979 has been shown valid over a wide temperature range [1-35]. This model has been found to be accurate for the most recently available electric data on the band-gap energy of silicon with high precision between 2 and 300 K [1-36].

The temperature characteristics of the carrier mobility were first studied in the 1950s [1-39, 40]. The bulk mobility temperature dependence was developed in the 1970s [1-41]. With the development of MOSFET, the temperature effect on the inversion layer and accumulation layer mobilities was developed [1-42, 43, 44]. All these models are empirical.

1. 4 Review of cryogenic power electronics

The motivation for low temperature electronics is the improved performance compared with room temperature electronics. This motivation was encouraged by the cryogenic research activities on MOSFETs in the 1970s [1-45, 46]. The research work showed that the cryogenic environment could offer some advantages, like lower forward voltage drop in majority carrier devices, higher switching speeds, reduced package volume and other merits [1-1].

This section will give a review of the cryogenic characteristics of the main power devices, including the power diode, bipolar transistor, MOSFET and IGBT, which are all made from silicon. The cryogenic research of germanium power devices is followed. Finally cryogenic power converter research activities are reviewed.

1. 4. 1 PiN diode cryogenic characteristics

The PiN diode is one of the very first semiconductor devices developed for power circuit applications. It consists of an intrinsic layer sandwiched between a pn junction, which has a very low concentration, generally n-type, in the order of 10^{13} cm^{-3}. The thickness of the intrinsic layer ranges from 10 to 500 μm depending on the rated breakdown voltage. The wide intrinsic region is flooded with minority carriers during forward conduction, so its resistance becomes very small allowing a high current density. Almost all silicon diodes with a blocking voltage over 200 V are PiN diodes [1-1, 47].

Early experiments noticed an increase of diode forward voltage, a decrease of breakdown voltage, and a slight decrease of junction capacitance as temperature reduces from 300 K to 77 K. Furthermore the authors concluded that diode doping must be carefully chosen to minimise the effects of freezeout on the diode series resistance [1-48].

Detailed measurements and modelling work on PiN diodes were carried out to characterise and optimise diode low temperature performance. Analyses and measurements proved that there is an order of magnitude reduction in the intrinsic region stored charge from 300 K down to 77 K. This results in a reduced switching loss at 77 K. An analytical model including end region recombination with bandgap narrowing was presented to explain diode low temperature performance in [1-49].

1. 4. 2 Power bipolar junction transistor (BJT) cryogenic characteristics

A power BJT is shown in Figure 1-1. It can be an n-p-n or p-n-p structure with a very highly doped emitter region, a thin middle base region and a step lightly-heavily doped collector

region. The main current is controlled through the base terminal. While power BJTs provide a very low voltage drop, the base current drive is continuously required for normal operation. The relatively low current gain of power bipolar devices and the requirement for complex high current drive circuits has resulted in the devices being superseded by MOSFETs and IGBTs [1-1].
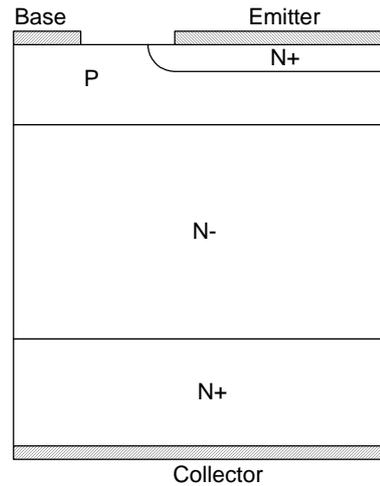
Figure 1-1 Structure of a typical half-cell of a power BJT [1-1]

Measurements performed on commercial bipolar junction transistors at 77 K show a large reduction in current gain, a slight increase in forward voltage drop, an increase in collector-emitter breakdown voltage, and an order of magnitude reduction in the turn-off time. In addition, numerical simulations indicated that an increased emitter current crowding occurs at 77 K. All these variations were attributed to energy narrowing and carrier freezeout [1-1, 50 and 51]. Research efforts have been exerted to avoid these degradations. The re-optimisation of the emitter, base and collector dopings and an increase of the emitter area can offer improved performance at low temperatures [1-51, 52]. A polysilicon emitter contact has been proved more efficient at lower temperatures than a metal contact to avoid the degradation of current gain [1-50, 53].

1. 4. 3 Power MOSFET cryogenic characteristics

The power MOSFET is one of the most important devices for very large-scale integrated circuits and power electronics. The principle of surface field-effect transistors was first proposed in the early 1930s [1-54]. In 1960, the MOSFET was first proposed and fabricated using a thermally oxidized silicon structure [1-55]. Many different structures have been developed. Three of most common structures– LDMOS, VMOS and VDMOS, are shown in Figure 1-2. LDMOS is often used in large-scale integrated circuit and VDMOS is preferred when high frequency and high voltage performance are needed. To a large extent, VMOS has been superseded by VDMOS for the critical requirements in controlling etching processes. The review of power MOSFETs will concentrate on VDMOSFET.
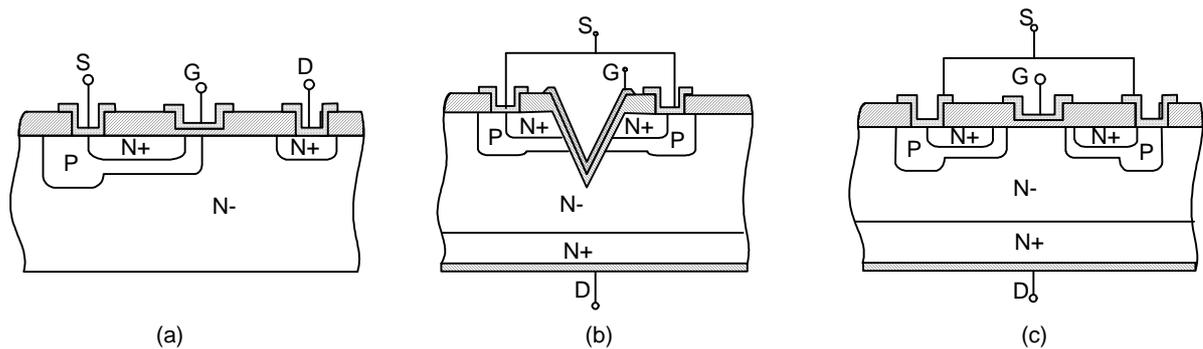
Figure 1-2 Cross sections of three typical MOSFETs
(a) Lateral double-diffused MOSFET (LDMOS); (b) V-groove double-diffused MOSFET (VMOS); (c) Vertical double-diffused MOSFET (VDMOS) [1-56]

 In a MOSFET, a control signal is applied to a gate electrode that is separated from the semiconductor device surface by an intervening insulator (normally silicon dioxide). There is no significant current flow during either on-state or off-state in the gate circuit. The high input impedance is a primary feature of power MOSFETs, which greatly simplifies the gate drive circuitry [1-47].

The possible advantages of operating MOSFETs at low temperatures began to be explored in the 1970s when it became clear that higher current density and lower power loss at low temperatures would result in devices packaged in small, readily-cooled volumes [1-57, 58]. More experimental work and numerical modelling resulted in a better understanding of the temperature dependence of inversion, accumulation and bulk mobilities [1-42, 44, 59 and 60]. The breakdown voltage and on-resistance were found to decrease whereas the threshold voltage and transconductance were found to increase at low temperatures [1-61, 62, 63, 64 and 65]. The analyses showed that a 77 K optimal VDMOSFET had a reduced polysilicon gate length as compared with a 300 K optimal device [1-64].

1. 4. 4 Power IGBT cryogenic characteristics

The basic difference between an IGBT and a MOSFET is the addition of a P+ substrate beneath the N drift region, as shown in Figure 1-3. This structural difference offers a high-current handling capability. This means that the IGBT combines the advantages of a bipolar device and a MOSFET. However, the IGBT has the disadvantages of a comparatively large current tail, which limits its applications at high frequencies. The IGBT technology is certainly the choice of device for breakdown voltages above 1000 V, while the MOSFET is for voltages below 250 V and frequencies above 100 kHz, as shown in Figure 1-4. Between 250 to 1000V, there are many technical papers available from manufacturers, some preferring MOSFETs, some IGBTs. Choosing between IGBTs and MOSFETs is very application-specific and cost, size, speed and thermal requirements should all be considered [1-67].

The IGBT technology is still being developed. Besides traditional technologies, PT (Punch-Through) and NPT (Non-Punch-Through), a new technology called IGBT 3 (trench field-stop technology) was reported and gradually commercialised in recent years [1-68]. More details about IGBTs will be reviewed in Chapter 2.
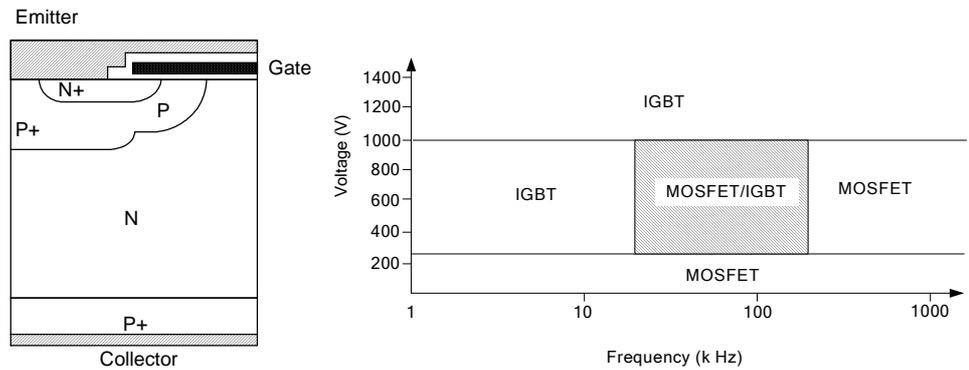
Figure 1-3 Structure of an IGBT [1-66] Figure 1-4 MOSFET and IGBT application range [1-67]

Cryogenic explorations of PT and NPT IGBTs have been reported. At low temperatures, the gate threshold voltages were found to increase, similar to the temperature characteristics of power MOSFETs [1-55]. Most devices showed reduced forward voltage drops at reduced temperatures and reached minimum values around 100 K. The increase of forward voltage drops below 100 K was caused by carrier freeze-out. The switching processes were found to be shorter at reduced temperatures because of the variation of carrier lifetimes [1-69, 70, 71, 72 and 73].

The maximum blocking voltages of IGBTs were found to decrease at low temperatures. For example, a 1300 V NPT IGBT could block only 900 V at 5 K [1-73]. This effect must be considered for cryogenic applications.

The experimental work showed that all the tested PT IGBTs lost their switchability below a certain temperature, above which the switchability returned. In contrast the NPT IGBTs remained switchable even at 5 K. This might be caused by carrier freezeout [1-73].

The cryogenic characteristics of the new technology, IGBT 3, have not been reported. There may be some differences from the PT and NPT devices.

1. 4. 5 Germanium devices

Applications of power devices below liquid nitrogen temperature (77 K) were also explored. Different materials have been used at extremely low temperatures.

Cryogenic research on germanium semiconductor devices was supported by NASA and other collaborators. At first Ge power diodes were examined at low temperatures. Commercial Ge power diodes were found to be capable of satisfactory operations down to around 20 K, and the forward voltage was considerably lower than that of the Si power diode. However, the reverse breakdown voltage was lower than desired. The breakdown voltage of re-optimised Ge diodes was found to be acceptable [1-74]. On the basis of these results for cryogenic Ge diodes, other Ge devices for cryogenic operations were developed. Ge BJTs were reported in [1-75] and showed better DC characteristics at 20 K. Ge JFETs and MISFETs (Metal Insulator Semiconductor Field-Effect Transistors) were also reported to even lower temperature– 4 K. Ge IGBTs for operations down to 20 K were reported to be under development [1-76, 77].

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1. 4. 6 Cryogenic power converters

The motivation for low temperature power electronics is improved performance compared to room temperature electronics. The increased speed, improved efficiency and reliability are key elements to implement cryogenic power converters.

Ultra high efficiency (>99%) power conversions were reported to be possible by combining cryogenic power MOSFETs and high current inductors made with high temperature superconductors [1-78, 79]. Some applications were foreseen, such as high power inverters, switch-mode amplifiers and multi-kilowatt RF (radio frequency) generators [1-79, 80, 81]. Since a significant improvement in high-frequency switching efficiency could be obtained by operating power MOSFETs at cryogenic temperatures, reduced system volume, improved conversion efficiency, and reduced cost were foreseen by using liquid-nitrogen cooled power converters [1-65, 82].

Since the middle 1990s, cryogenic power converters were anticipated to play an important role in space missions. Different converter technologies using silicon power MOSFETs were tested at cryogenic temperatures: buck converter [1-83], PWM boost converter [1-84, 85], full-bridge DC/DC converter [1-86], three-level buck converter [1-87, 88] and commercial low power DC/DC converter modules [1-89, 90, 91]. High-speed PWM control chips for DC/DC converters were studied in [1-92, 93]. The DC/DC converters for cryogenic and space applications were positively evaluated in [1-25, 94, 95]. Based on the results of this research, a large number of cryogenic converter-related patents have been registered since 2000 [1-96, 97 and 98].

1. 4. 7 Summary of cryogenic power electronics

Many semiconductor devices and circuits can operate at temperatures down to the cryogenic range. However, the devices that show improved performance at cryogenic temperatures are nearly always field-effect transistors (MOSFET, JFET and MESFET). Standard bipolar junction transistors perform poorly at very low temperatures due to a large reduction in current gain and on-state current density.

In general, the power dissipation in devices reduces as operating temperature is reduced from room temperature to 77 K. In majority carrier devices, like Schottky barrier diode, power MOSFET and power JFET, this is mainly caused by a reduction in on-state voltage drop due to an increase in carrier mobilities. In minority carrier devices, like the PiN diode, power BJT, IGBT and thyristor, this is mainly caused by a reduction in the switching losses because of: (a) a dominance of end-region recombination current; (b) a reduction of carrier lifetime; and (c) an increase in carrier mobilities [1-1]. The breakdown voltage in devices normally decreases gradually as temperature is reduced down to the cryogenic range.

With the characterisation of cryogenic power devices, research efforts have been exerted on cryogenic power electronic systems, that is, power converters. Different converter technologies using silicon power MOSFETs were tested at cryogenic temperatures and commercial applications were positively anticipated.

As a new and promising technology, power IGBTs are not fully characterised at low temperatures. It can be predicted that power IGBTs will play an important role in cryogenic power electronics from the published research results.

1. 5 Summary of literature review

From the literature review, it can be seen that cryogenic semiconductor physics is well developed, which provides a foundation for cryogenic power electronics.

The silicon power devices including power diodes, bipolar transistors, MOSFETs are well characterised for applications at low temperatures. The silicon IGBT is not yet fully characterised and related applications are still under laboratory development. Compared with room temperature operation, cryogenic power electronics can offer increased efficiency, power density or higher switching frequency.

To survive in a hostile environment like deep space, germanium devices including diodes, BJTs, JFETs and MISFETs have been characterised and re-optimised for applications at low temperatures. Below 30 K, germanium devices show much better characteristics than silicon ones. The lowest temperature tested for germanium devices is 4 K. Germanium IGBTs for cryogenic operation are reportedly under development, but no results have yet been published.

Cryogenic power conversion can be applied advantageously at high power levels (>10 kW), especially where a cryogenic environment is available as in magnetic resonance imaging systems and in deep space. The main possible advantages of cryogenic power conversion are size, weight and cost reductions. The feasibility of designing completely cryogenic power electronic systems for airplanes, ships, aircraft and power utility systems is being studied all over the world [1-79].

1. 6 Scope of the thesis

From the literature review, the cryogenic physics of silicon is well developed, but the Si IGBT is not fully characterised at low temperatures. To advance cryogenic applications of silicon IGBTs, cryogenic characterisation, modelling and simulation of silicon IGBTs are presented in this thesis.

Chapter 2 describes the power diode and IGBT characteristics in the normal temperature range. To understand the cryogenic characteristics of a power device, it is necessary first to appreciate its normal characteristics.

Chapter 3 introduces the cryogenic experimental work on three types of IGBT modules. An experimental system based on a cryostat is described. The static and switching test results of typical IGBTs and diodes from 50 K to 300 K are reported and analysed.

Chapter 4 explains the modelling work on the cryogenic characteristics of IGBTs. A physically based, compact device model is selected to model the cryogenic performance of the three tested IGBTs. A generic Saber power diode model with reverse recovery is selected to model the diode performance at low temperatures. The experimental work described in Chapter 3 is used to parameterise the models.

Chapter 5 describes the simulation work in Saber to examine the cryogenic performance of a DC-DC buck converter and a pulse-width modulated inverter leg. The converter and inverter leg consist of the temperature-dependent IGBT and diode models, which are obtained from the modelling work in Chapter 4.

Chapter 6 draws conclusions on the cryogenic work on IGBTs. The priorities for further

research on cryogenic power electronics, especially on IGBTs are summarised.

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Chapter 2 Basic characteristics of the PiN diode and IGBT

2. 1 Introduction

Before examining the cryogenic behaviour of power devices, it is useful to review their characteristics in the normal operating temperature range. This chapter concentrates on the PiN power diode and the IGBT. First, the basic structure and operating mechanism is explained, followed by a review of the terminal characteristics (static and switching) and the temperature sensitivity of the characteristics over the normal temperature range of 25 to approximately 150˚C.

2. 2 PiN power diode

Power semiconductor devices, even diodes, are more complicated in structure and operation than their low-power counterparts. The added complexity arises from the modifications made to accommodate the high voltage and current requirements [2-1].

2. 2. 1 Basic structure

In the case of the power diode or PiN diode, the intrinsic N- region is the prime structural feature not found in low-power diodes, as shown in Figure 2-1. The N- region has a very low concentration, generally in the range of 10^{13} ~10^{14} cm^{-3} and its thickness ($2d$) ranges from 10 to 500 μm depending on the rated breakdown voltage level [2-1, 2]. The outside P+ and N+ layers are usually highly doped, in the order of 10^{19} cm^{-3}. The cross-sectional area of the diode varies according to the rated current. For diodes that can carry several thousand amperes, the area can be several square centimetres [2-1].
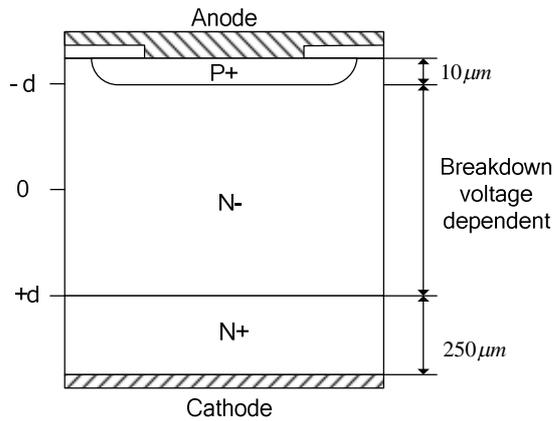
Figure 2-1 Structure of a typical PiN diode [2-1]

2. 2. 2 Static characteristics

The injection of minority carriers plays a major role in determining the forward conduction characteristics: low-level and high-level, as shown in Figure 2-2. At low current levels, the current rises exponentially with the applied voltage, however, at high current levels, the output characteristics deviate from the exponential behaviour: the current increases linearly with the forward bias voltage [2-1, 3]. At high current levels, the N- intrinsic region is flooded with minority carriers and its resistance R_{on} becomes very small, allowing a very high current density [2-4]. The forward bias characteristics of a power diode can be modelled approximately as an ideal diode in series with an on-state voltage source and a resistor R_{on}, as illustrated in Figure 2-2.

Under reverse bias conditions, only a small leakage current I_S flows until the breakdown voltage V_B is reached. The breakdown of a power diode should be avoided since the excessive power dissipation is likely to damage the device.
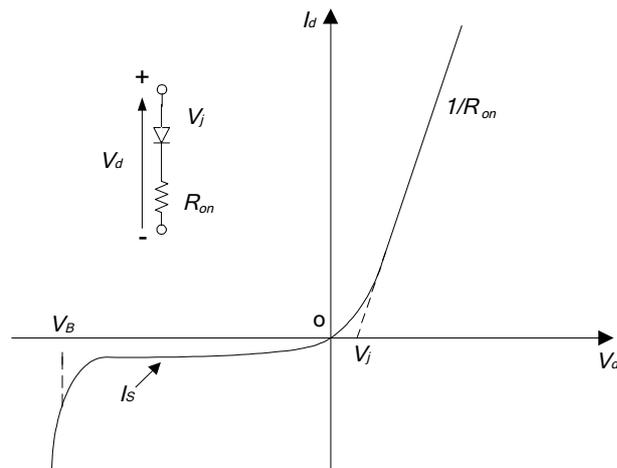
Figure 2-2 I-V characteristics of a PiN diode [2-1]

2. 2 .3 Switching characteristics

Typical current and voltage waveforms are sketched in Figure 2-3 for the turn-on and turn-off transients. The forward voltage drop across a PiN diode initially exceeds its steady state value at the same current level when it is turned on with a high di/dt. This phenomenon is called forward voltage overshoot or forward recovery, and arises from the existence of the highly resistive i-region. Under steady-state current conduction, the i-region resistance is dramatically reduced by the injected minority carriers, however, during turn-on under high di/dt conditions, the current rises at a faster rate than the diffusion of the minority carriers. Therefore, a high voltage drop develops across the i-region for a short time until the minority carrier distribution reaches equilibrium conditions. Under very high di/dts, forward voltage overshoots can be in excess of 30 V [2-3].
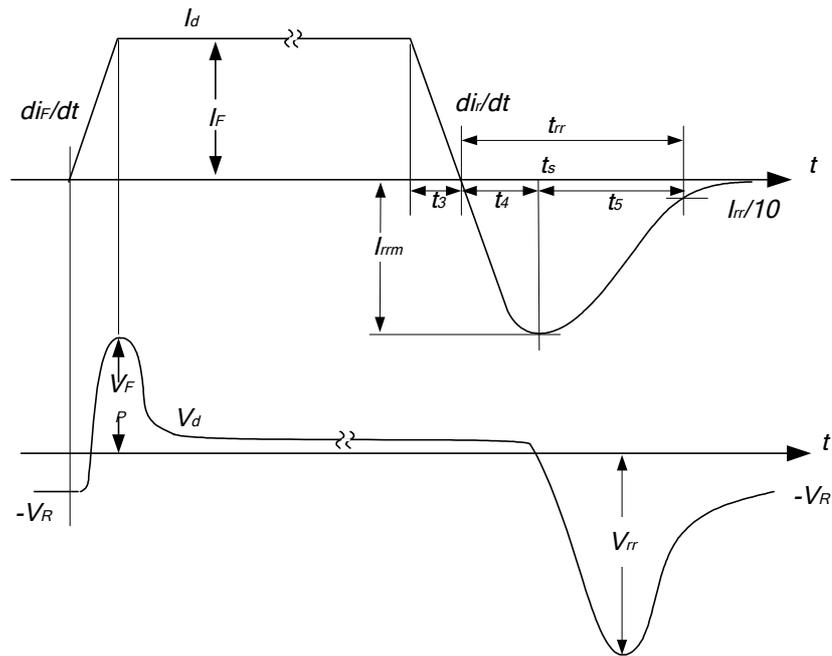
Figure 2-3 Sketched current and voltage waveforms during turn-on
and turn-off transients [2-1]

A reverse recovery process occurs when the diode is switched from its on state to its reverse blocking state. During this transition the minority carriers stored in the i-region during forward conduction must be removed. As shown in Figure 2-3, a large reverse current pulse exists during the turn-off process. The time interval $t_{rr} = t_4 + t_5$ is often termed the reverse recovery time. The peak reverse current I_{rrm} can be comparable with the forward current I_F. To ameliorate the reverse recovery transient, the semiconductor is often doped in such a way that the minority carrier lifetime is reduced. A snappiness factor S is used to describe the reverse recovery current waveform where S is given by:

$$S = t_5 / t_4 \tag{2-1}$$

A very snappy reverse recovery, high value of S, is often undesirable as it can trigger violent parasitic oscillations and produce EMC (Electromagnetic Compatibility) problems.

The severity of the reverse recovery transient depends on the speed with which the diode is turned off. Diode datasheets often give detailed plots of t_{rr} and reverse recovery charge Q_{rr} as functions of the reverse current gradient, di_r/dt [2-1].

In typical power electronic switching circuits, the reverse current flows through the transistor that is turning on, increasing the turn on losses and possibly degrading the transistor's reliability. Many research efforts on PiN diodes have focused on improving the reverse recovery characteristics [2-3].

2. 2. 4 Trade-off between the switching speed and the forward voltage drop

The trade-offs between the static and dynamic characteristics of the diode may be seen in the following equations, taken from [2-3], which describe the basic conduction mechanism of the device.

The voltage drop across the N- region V_M can be expressed by

$$V_M = \frac{3kT}{e}\left(\frac{d}{L_a}\right)^2 \qquad\qquad \text{for } d \leq L_a; \qquad\qquad (2\text{-}2)$$

$$V_M = \frac{3\pi kT}{8e}\exp\left(\frac{d}{L_a}\right) \qquad\qquad \text{for } d \geq L_a; \qquad\qquad (2\text{-}3)$$

where e is the electron charge, 1.60×10^{-19} C;

T is temperature, K;

k is the Boltzmann constant, 1.38×10^{-23} J K^{-1};

d is the half length of the i- region, cm;

L_a is the ambipolar diffusion length (cm), given by

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$$L_a = \sqrt{D_a \tau_a} \qquad\qquad (2\text{-}4)$$

where τ_a is the minority carrier life time, s.

D_a is the ambipolar diffusion coefficient, $\text{cm}^2\ \text{s}^{-1}$, which is given by [2-4]

$$D_a = \frac{(n+p)D_n D_p}{(nD_n + pD_p)} \qquad\qquad (2\text{-}5)$$

where n and p are the electron and hole concentrations, cm^{-3};

D_n and D_p are the electron and hole diffusion constants, $\text{cm}^2\ \text{s}^{-1}$, which are related with carrier mobility.

From (2-2) and (2-3), the voltage drop V_M increases when the value of L_a decreases. From (2-4), the value of L_a decreases when the minority lifetime τ_a is reduced to improve the reverse recovery characteristics. Therefore the amelioration of the reverse recovery characteristics by lifetime reduction is accompanied by a degradation in the forward conduction characteristics.

A trade-off between the switching speed and the forward voltage drop is undertaken during power diode design. This trade-off is dependent on a number of factors such as the N-base width, the recombination center position in the energy gap, the distribution of the deep-level impurities, and the doping profile in the i-region. This trade-off exists not only in the power diode, but also in all the bipolar power devices, including the power IGBT.

2. 2. 5 Temperature effects

The normal operating temperature range for power diodes is - 40 to around 150 °C and over this range there are significant variations in some of the characteristics, and these are reviewed in this section.

(a) On-state characteristics

Several conflicting effects combine to give the overall variation in characteristics with temperature. The total voltage drop across the end P+ and N+ regions is given by [2-4]

$$V_{P+} + V_{N+} = \frac{kT}{e} \ln\left[\frac{n(+d)n(-d)}{n_i^2}\right]$$
(2-6)

where $n(-d)$ and $n(+d)$ are the electron concentrations at the $-d$ and $+d$ ends in the mid-region respectively, cm^{-3}.

n_i is the intrinsic concentration, cm^{-3}.

Since n_i is a rapidly rising function of temperature, the sum of V_{P+} and V_{N+} decreases at high temperatures. The decrease of carrier mobility will result in the reduction in the value of diffusion coefficient, D_a, and is expected to result in an increase of the voltage drop across the i-region. However, carrier lifetime normally increases with temperature and this may offset some effect of the reduced mobility. The net result is normally that at low current densities V_F decreases with increasing temperature whereas at high current densities it increases [2-5, 6]. In the approximate model of the device, this may be represented by a decrease in the knee voltage and an increase of the resistance R_{on}. This effect is shown in Figure 2-4.
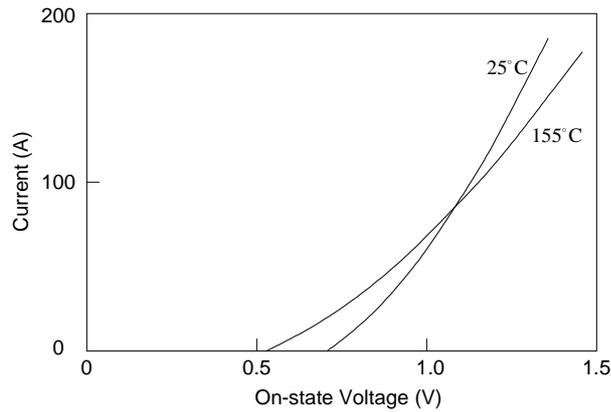
Figure 2-4 Temperature effect on the forward characteristics of a 2.5 kV diode [2-6]

(b) Reverse bias characteristics

The temperature coefficient for avalanche breakdown is positive. This is because the increased thermal energy of the atoms at higher temperature results in an increased vibration amplitude, reducing the mean distance between collisions. For a given electric field, a lower average carrier speed leads to a less effective impact ionisation. This results in a slight increase in avalanche breakdown voltage at high temperatures.

Figure 2-5 indicates the reverse leakage current increases with increased junction temperature [2-5]. This effect can become dominant at high temperatures, especially for high voltage devices.
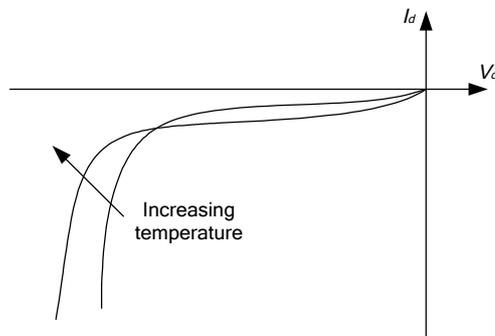
Figure 2-5 Temperature effect on the reverse bias characteristics of a power diode [2-5]

(c) Switching characteristics

The carrier lifetime, at both high and low injected concentrations for p- and n- type silicon, increases in the temperature range of 0-200 °C [2-7]. This effect results in a more severe reverse recovery process at high temperature, and can result in a significant increase in switching losses. An example of the temperature effect on the diode reverse recovery characteristics is given in Table 2-1 for a typical 1200 V, 30 A device.

Parameter	Symbol	Values			Unit
		min.	Typ.	max.	
Reverse recovery time V_R=800V, I_F=30A, di_r/dt = 850A/µs, T_j=25°C V_R=800V, I_F=30A, di_r/dt = 850A/µs, T_j=125°C V_R=800V, I_F=30A, di_r/dt = 850A/µs, T_j=150°C	t_{rr}	 - - -	 243 355 380	 - - -	ns
Peak reverse current V_R=800V, I_F=30A, di_r/dt = 850A/µs, T_j=25°C V_R=800V, I_F=30A, di_r/dt = 850A/µs, T_j=125°C V_R=800V, I_F=30A, di_r/dt = 850A/µs, T_j=150°C	I_{rrm}	 - - -	 23.7 28.3 29.5	 - - -	A
Reverse recovery charge V_R=800V, I_F=30A, di_r/dt = 850A/µs, T_j=25°C V_R=800V, I_F=30A, di_r/dt = 850A/µs, T_j=125°C V_R=800V, I_F=30A, di_r/dt = 850A/µs, T_j=150°C	Q_{rr}	 - - -	 2630 4700 5200	 - - -	nC
Reverse snappiness factor V_R=800V, I_F=30A, di_r/dt = 850A/µs, T_j=25°C V_R=800V, I_F=30A, di_r/dt = 850A/µs, T_j=125°C V_R=800V, I_F=30A, di_r/dt = 850A/µs, T_j=150°C	S	 - - -	 6 7.4 7.5	 - - -	

Table 2-1 Temperature effect on the reverse recovery characteristics of a 1200V, 30 A diode [2-8]

2. 3 Power IGBTs

The concept of power IGBTs is based on the combination of bipolar current conduction with MOS gated current control within the same semiconductor region. Due to this structural feature, power IGBTs exhibit superior on-state characteristics, reasonable speed, excellent safe operating area and have simple, low power drive requirements. For these reasons, power IGBTs have become the most widely used power devices in the medium power and medium frequency range.

2. 3. 1 Basic structure and operation

A sketched cross section of an n-channel IGBT is shown in Figure 2-6 (a). At first sight an IGBT is just a MOSFET plus a lower p-n junction (J1). However, this structural variation provides the IGBT with very different characteristics.

The IGBT equivalent circuit is shown in the right side of Figure 2-6 (b). Under normal conditions, the parasitic thyristor does not conduct and the IGBT may be regarded as a cascaded connection of a MOSFET and a bipolar transistor, with the MOSFET providing the base current for the bipolar device.

(a)   (b)
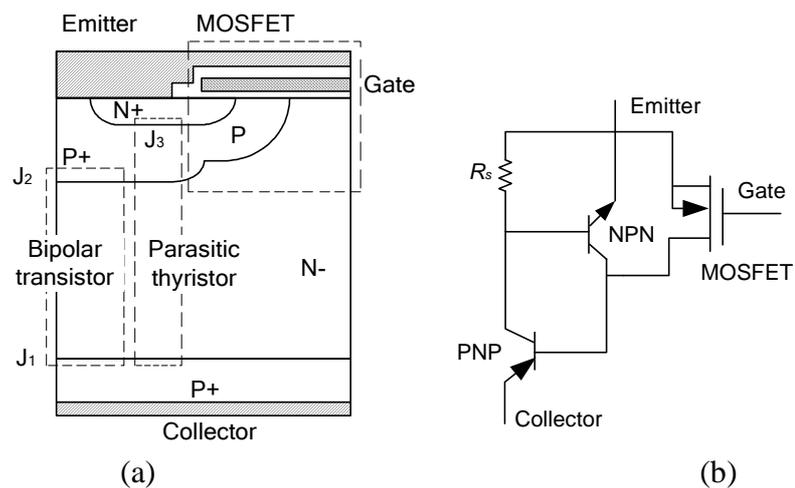
Figure 2-6 IGBT structure and equivalent circuit [2-3]
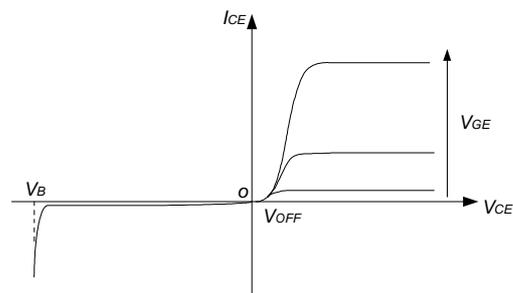
Figure 2-7 Output characteristics of an IGBT

The output characteristics of the IGBT are shown in Figure 2-7. If a sufficient positive gate bias exists when the device is in its forward blocking mode, it can be switched into the

forward conducting state, and electrons flow from the N^+ emitter to the N^- drift region. This provides the base drive current for the vertical PNP transistor in the IGBT structure. Since the emitter junction (J_1) for this bipolar transistor is forward biased, the P^+ region injects holes into the N- base region. When the positive bias on the collector terminal of the IGBT is increased, the injected hole concentration increases until it exceeds the background doping level of the N^- drift region. In this regime of operation, the device characteristics are similar to those of a forward biased PiN diode. Consequently, the power IGBT is superior to the power MOSFET in the medium frequency range, being able to operate at high current densities even when designed to support high blocking voltages [2-3].

However, if the inversion layer conductivity is reduced by application of a gate bias close to the threshold voltage, a significant voltage drop occurs across the channel region. When this voltage drop becomes comparable to the difference between the gate bias and the threshold voltage, the channel becomes pinched-off. At this point, the electron current saturates. Since this limits the base drive current for the PNP transistor, the hole current flowing through this path is also limited.

Removal of the gate bias cuts off the supply of electrons to the N^- drift region and initiates the turn-off process. Due to the presence of the high concentration of minority carriers injected into the N^- drift region during forward conduction, the turn-off does not occur abruptly. At first, a sudden current drop is observed and then the collector current decays gradually with a characteristic time constant determined by the minority carrier lifetime [2-3]. This phenomenon is called the IGBT tail current.

In the design of an IGBT device, it is necessary to make a trade-off between the conduction and switching loss. The conduction loss could be greatly reduced by increasing the hole injection efficiency of the collector, however, the decay time for the tail current will increase and the switching loss is also likely to increase. This trade-off is typically made assuming a junction temperature in the region of 100 °C.

The parasitic thyristor may be activated under some abnormal conditions like very high rate of rise of collector-emitter voltage at turn off or too large a value of R_s. This phenomenon is called latch up. Once the thyristor has been activated, the gate can no longer control the flow of current through the device. The details are described in [2-3].

2. 3. 2 Typical IGBTs

(a) Traditional technologies– PT and NPT IGBTs

The two traditional technologies – PT (punch-through) and NPT (non-punch-through) IGBTs, are also referred to as asymmetrical and symmetrical IGBTs respectively. These two basic types of IGBT, shown in Figure 2-8, differ widely with regard to their fabrication technology, structural details, carrier profiles, carrier lifetimes and transport mechanisms. These physical differences correspond to different output characteristics, behavioural patterns and other device properties.
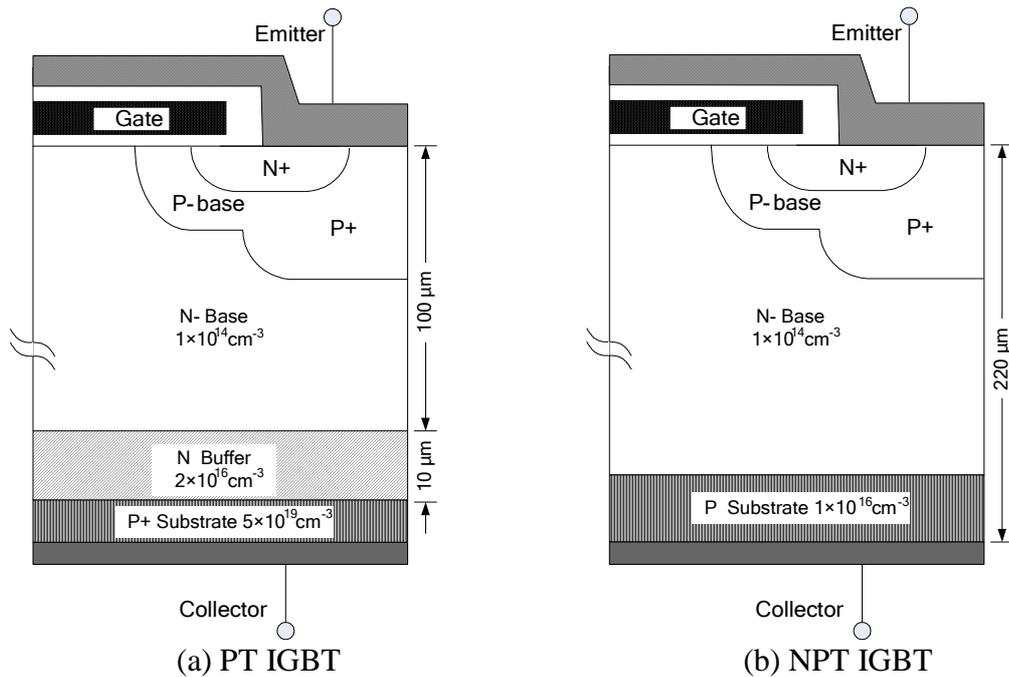
Figure 2-8 Two traditional IGBT structures [2-9]

PT- IGBT fabrication utilizes the technology of growing a thick epitaxial layer of uniform resistivity (1×10^{14} cm^{-3}) and thickness (100 μm) on a P$^+$ substrate (5×10^{19} cm^{-3}) where the numeric values given are typical of a 1200 V device. The thick epitaxial layer forms the N$^-$ base. The N buffer is sandwiched between the P$^+$ substrate N$^-$ base. The buffer layer has two functions. First, the thickness of the N$^-$ base required to support a given breakdown voltage is decreased since the depletion layer expansion at high applied voltage is accommodated in a small thickness of this buffer layer, avoiding failure by punchthrough. Second, the holes injected recombine in the buffer layer. This slightly offsets the injection efficiency of the collector. Therefore the buffer layer reduces the tail current and shortens the fall time of the IGBT. By this mechanism, the trade-off between conduction and switching loss is improved.

In contrast, The NPT-IGBT is manufactured using diffusion steps on the basis of thin wafer technology. The starting Si wafer is an N-type <100> orientation wafer of thickness 220 μm and concentration 1×10^{14} cm^{-3} for a 1200 V device. On the back of the wafer, boron

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implantation is performed, followed by a long and high-temperature drive-in cycle. This produces a p-type collector at a concentration of 10^{16} cm^{-3} instead of a P$^+$ collector. The process of manufacturing the NPT-IGBT is less expensive that that of the PT-IGBT.

Due to the existence of a high concentration gradient across the P$^+$ collector/N buffer/N$^-$ base, the current flow is more aided by diffusion in a PT IGBT than in a NPT IGBT. Furthermore, in the PT device the electrical field has a smaller N$^-$ base thickness to spread over, so the PT device is more fragile than the NPT case [2-9].

(b) New Technology– IGBT3

Some drawbacks exist in both the PT and NPT IGBTs. The PT IGBT has a high carrier concentration in the P$^+$ substrate resulting in an undesired high turn off current and losses. In contrast, the NPT IGBT has the desirable low carrier concentration in the P$^+$ substrate, but the n-layer has to be rather thick due to its triangular electrical field in the blocking condition. This thick n-layer results in higher static and dynamic losses [2-10].

Two techniques have been developed to enhance the on state and switching characteristics of the new device- IGBT3. First, sinking the gate into the surface of the wafer to form a set of trenches produces an increased carrier concentration in the emitter region and allows the on-state voltage to be reduced. The second technique involves introducing an additional, weakly doped n-type field-stop layer next to the p-emitter on the bottom of the wafer, the doping of the field stop layer being typically in the region 10^{15} to 10^{16} cm^{-3}. This allows the wafer thickness to be reduced by around 30% for the same forward blocking voltage. For example, a 1200 V IGBT3 can be made with a wafer thickness of 120 μm instead of 175 μm for a

NPT device. The on-state voltage is therefore reduced, and due to the reduction in stored carriers, the switching speed may be increased [2-11, 12]. The new device, shown in Figure 2-9, incorporates both of these enhancements.

Since the IGBT3 is much thinner than the earlier devices, the processing of the device presents several challenges requiring sophisticated wafer handling [2-11]. The trench is etched by a fluorine-based, reactive ion etching process in the gate area. The corners of the trench are rounded. The gate oxide is grown thermally over the sidewalls and the base of the trench surface, and is followed by filling the trench by Polysilicon deposition. The buffer layer is implanted on the backside of the wafer [2-9].
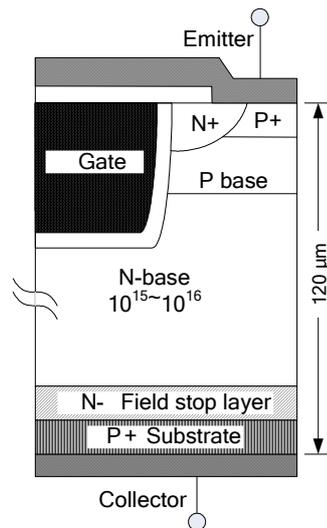
Figure 2-9 Structure of a IGBT3 [2-9]

The field-stop layer in a typical IGBT3 has a doping of 10^{15}~10^{16}, which is totally different from the buffer layer in a typical PT IGBT. In PT IGBTs, the buffer layer is not only responsible for stopping the electrical field, but also for reducing the enormous p emitter efficiency, and therefore has a doping of more than 10^{16}~10^{17} cm^{-3} at thickness of 10 μm or more [2-10]. The comparison of these three IGBTs is described in Table 2-2.

Layers	PT –IGBT	NPT- IGBT	IGBT3
p-emitter	Very high efficiency	Low efficiency	Low efficiency
n⁻ -layer	Thin	Medium	Thin
Additional n-layer	Buffer layer - highly doped; to reduce the very high emitter efficiency; to stop the electrical field	No	Field-stop layer- weakly doped; to stop only the electrical field;
Carrier lifetime	Low	High	High

Table 2-2 Comparison of three IGBTs [2-10]

2. 3. 3 Static blocking capability

The reverse and forward blocking capabilities of PT and NPT IGBTs will be discussed in this section. The electric field distributions under forward and reverse blocking conditions will be described to analyse the differences of these two devices.

(a) Reverse blocking capability

The junction J_1 in Figure 2-6 is reverse biased during reverse blocking and its depletion layer extends primarily into the N⁻ drift region. The reverse blocking voltage is determined by an open-base-transistor formed between the P⁺ collector, N⁻ drift region and the P- base region. This structure is prone to punch-through breakdown if the N⁻ drift region is too lightly doped or too narrow. It is essential to design optimally the resistivity and thickness of the N⁻ drift region. Generally the N⁻ drift region is chosen so that its thickness is equal to the depletion width at maximum operating voltage plus one diffusion length, that is [2-3]

$$d_N = \sqrt{\frac{2\varepsilon_{Si}V_m}{eN_d}} + L_p \qquad (2\text{-}7)$$

where d_N is the N⁻ drift region width, cm;

V_m is the maximum reverse blocking voltage, V;

L_p is the minority carrier diffusion length, cm.

However, the added p–n⁻ junction J_1 of the IGBT is not normally designed to block a significant voltage. Most IGBTs do not have reverse blocking capability in practice [2-13].

(b) Forward blocking capability

To operate the IGBT in the forward blocking mode, the gate must be shorted to the emitter or reverse biased. When a positive collector voltage is applied, the P- base/ N⁻ drift region junction J_2 in Figure 2-6 becomes reverse biased. A depletion layer extends from this junction on both sides.

Like the power MOSFET, the gate cell must be designed to make sure that the depletion layer of the junction J_2 in the P- base does not punch-through to the N⁺ emitter region. The spacing between the DMOS cells also affects the forward blocking capability. However, a large-size cell may increase the source resistance R_s and increase the risk of triggering the parasitic thyristor.

Figure 2-10 shows the electrical field distribution for the PT and NPT IGBTs under both forward and reverse blocking conditions. These two devices have 'asymmetrical' and 'symmetrical' electrical field distributions respectively. In the PT IGBT, the reverse breakdown voltage is less than the forward breakdown voltage. The NPT IGBT has equal forward and reverse breakdown voltages [2-3, 9].
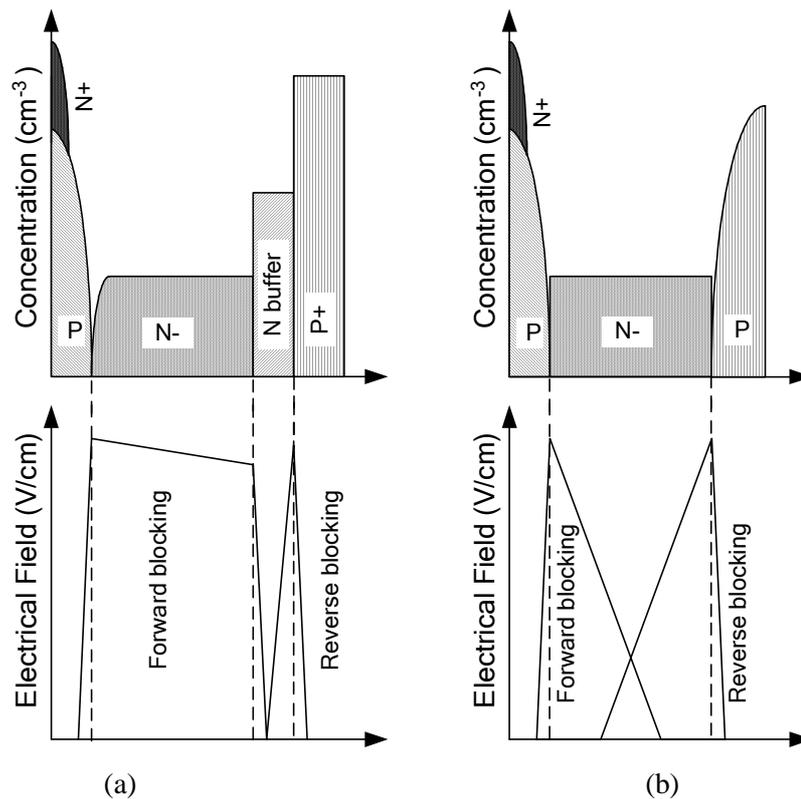
Figure 2-10 Doping profiles and electric field distributions in (a) PT and (b) NPT IGBTs under forward and reverse blocking conditions [2-5]

2. 3. 4 Forward conduction characteristics

At its simplest level, an IGBT can be treated as a MOSFET in series with a diode to understand the device forward characteristics, and can also be treated as a MOSFET driving a bipolar transistor to study its behaviour in more detail. These two models will be explained in this section.

(a) PiN diode/MOSFET model

The PiN diode/MOSFET model is shown in Figure 2-11. In this model, the collector current is assumed equal to the current through the diode and the MOSFET:

$$I_{CE} = I_{MOS} = I_{PiN} \tag{2-8}$$

where I_{CE}, I_{MOS} and I_{PiN} are the collector current, the currents through the diode and the MOSFET respectively, A.
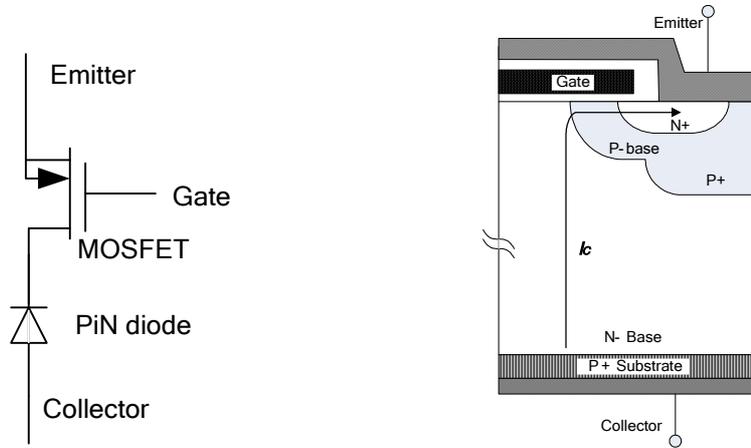
Figure 2-11 PiN diode/MOSFET model [2-3]

The voltage drop across the PiN diode component V_{PiN} is related to its forward conduction current density [2-3]

$$J_{PiN} = \frac{2eD_a n_i}{d} F\left(\frac{d}{L_a}\right) e^{eV_{PiN}/2kT} \tag{2-9}$$

where J_{PiN} is the current density through the PiN diode component, A cm^{-2};

V_{PiN} is the voltage drop across the PiN diode component, V.

The function $F(d/L_a) = \dfrac{d/L_a \tanh(d/L_a)}{\sqrt{1 - 0.25 \tanh^4(d/L_a)}} \exp\left(-\dfrac{eV_M}{2kT}\right)$ (2-10)

where V_M is the voltage drop across the i- region in the PiN diode component, V.

Since the current density in the PiN diode is assumed equal to the collector current density J_C, equation (2-9) may be re-arranged to give:

$$V_{PiN} = \frac{2kT}{e} \ln\left(\frac{J_C d}{2eD_a n_i F(d/L_a)}\right) \tag{2-11}$$

where J_C is the collector current density, A cm^{-2};

The MOSFET current is given by

$$I_{MOS} = J_{MOS}WZ \approx J_C WZ \tag{2-12}$$

where J_{MOS} is the MOSFET current density, A cm^{-2}; W and Z are the width and depth of the

gate channel respectively, cm;

According to MOSFET theory, the current through the MOSFET can be expressed as [2-3]

$$I_{MOS} = \frac{\mu_{ns}C_{OX}Z}{2L_{CH}}[2(V_{GE} - V_T)V_{MOS} - V_{MOS}^2] \tag{2-13}$$

where V_{MOS} is the voltage drop across the MOSFET component, V;

μ_{ns} is the surface mobility of the channel, cm^2/V-s ;

C_{OX} is the capacitance per unit area of the gate oxide, F cm^{-2};

L_{CH} is the length of the gate channel, cm;

V_{GE} and V_T are the gate-emitter voltage and its threshold value respectively, V.

In the linear region, the voltage drop across the MOSFET component is very small.

Therefore $V_{MOS} \ll V_G - V_T$, and equation (2-13) becomes

$$I_{MOS} = \frac{\mu_{ns}C_{OX}Z}{L_{CH}}(V_{GE} - V_T)V_{MOS} \tag{2-14}$$

The voltage drop across the MOSFET section is then given by

$$V_{MOS} = \frac{I_{CE}L_{CH}}{\mu_{ns}C_{OX}Z(V_{GE} - V_T)} \tag{2-15}$$

The forward voltage drop across the IGBT is the sum of the voltage drop across the

MOSFET and the PiN diode component:

$$V_F = \frac{2kT}{e}\ln\left(\frac{I_{CE}d}{2eWZD_a n_i F(d/L_a)}\right) + \frac{I_{CE}L_{CH}}{\mu_{ns}C_{OX}Z(V_{GE} - V_T)} \tag{2-16}$$

where V_F is the on-state voltage drop of the IGBT, V.
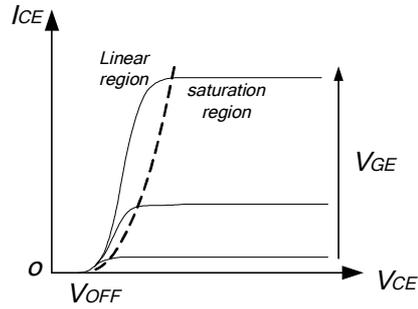
Figure 2-12 IGBT forward conduction characteristics

From equation (2-16), the forward conduction characteristics can be computed as a function of the gate bias voltage. Typical forward characteristics will take the form shown in Figure 2-12. The "knee voltage" below which very little current flows, is because of the lack of injection from the collector junction [2-3].

The PiN diode/MOSFET model can be used to understand the behaviour of the forward conduction characteristics. It is convenient to use this model to consider the temperature effect on the forward conduction characteristics. The major shortcoming is that it omits the hole current component flowing into the P-base region, which is included in the model based on a MOSFET driving a bipolar transistor.

 (b) Bipolar transistor/MOSFET model

An IGBT can also regarded as a MOSFET driving a bipolar transistor, as shown in Figure 2-13, where the electron current (I_e) flows through the MOSFET channel and the hole current (I_h) flows through the bipolar transistor section. These currents are related via the current gain of the wide-base transistor:

$$I_h = \left(\frac{\alpha_{PNP}}{1 - \alpha_{PNP}} \right) I_e \qquad (2\text{-}17)$$

where α_{PNP} is the current gain of the transistor.

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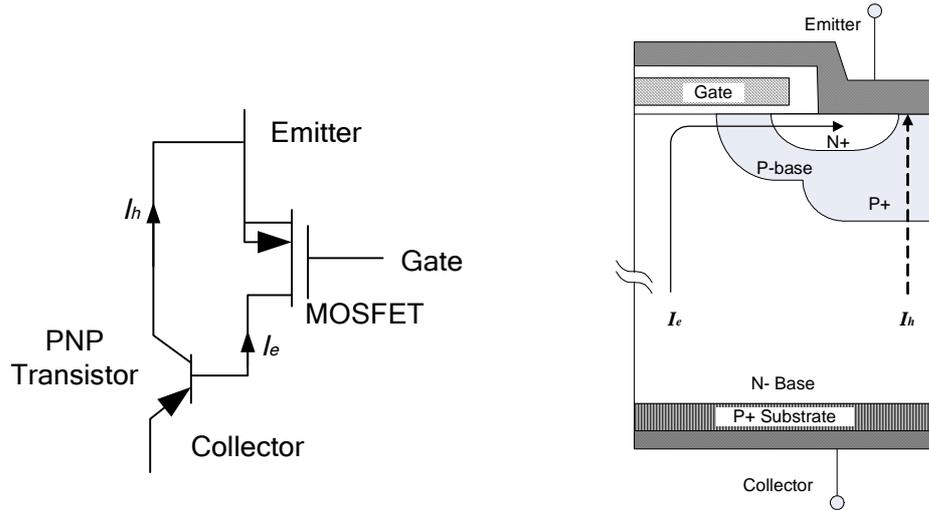
Figure 2-13 The equivalent circuit and current distribution for the bipolar transistor/MOSFET model of an IGBT

The collector current is the sum of these components:

$$I_{CE} = I_h + I_e = \frac{1}{1-\alpha_{PNP}} I_e \tag{2-18}$$

The voltage drop in the N-drift region can still be approximated as that for a PiN diode with a current flowing through it as (2-16). Therefore the on-state voltage drop of the IGBT is given by

$$V_F = \frac{2kT}{e} \ln\left(\frac{I_{CE}d}{2eWZD_a n_i F(d/L_a)}\right) + \frac{(1-\alpha_{PNP})I_{CE}L_{CH}}{\mu_{ns}C_{OX}Z(V_{GE}-V_T)} \tag{2-19}$$

This voltage is smaller than that from (2-16) because all the collector current no longer flows through the MOSFET channel [2-3].

In the saturation region, the electron current is given by

$$I_{e,sat} = \frac{\mu_{ns}C_{OX}Z}{2L_{CH}}(V_{GE}-V_T)^2 \tag{2-20}$$

where $I_{e,sat}$ is the saturate electron current component, A.

From (2-18), the saturated current is then

$$I_{CE,sat} = \frac{1}{1-\alpha_{PNP}} I_{e,sat} = \frac{1}{1-\alpha_{PNP}} \frac{\mu_{ns} C_{OX} Z}{2L_{CH}} (V_{GE} - V_T)^2 \qquad (2\text{-}21)$$

where $I_{CE,\,sat}$ is the saturated collector- emitter current, A.

From this equation, the transconductance of the IGBT in the active region can be obtained by differentiation with respect to V_{GE}:

$$g_{ms} = \frac{1}{1-\alpha_{PNP}} \frac{\mu_{ns} C_{OX} Z}{L_{CH}} (V_{GE} - V_T) \qquad (2\text{-}22)$$

where g_{ms} is the transconductance of the IGBT, S.

The transconductance of the IGBT is larger than for a power MOSFET with same aspect ratio (Z/L_{CH}). It depends on the gain of the wide-base bipolar transistor inherent in the IGBT structure. Since the current gain α_{PNP} of the PNP transistor is typically around 0.5, the transconductance of the IGBT is typically a factor of 2 times larger than that for a MOSFET with the same channel aspect ratio.

2. 3. 5 Switching characteristics

When the gate voltage falls below the threshold voltage, the channel inversion layer will no longer exist, and the collector current will drop abruptly because the channel current component (I_e) is suddenly discontinued. After this occurs, the collector current continues to flow since the hole current does not cease abruptly. As the minority carrier density in the N-drift region decays due to recombination, it leads to a gradual reduction in the collector current. This current flow is referred to as the current tail, shown in Figure 2-14. The turn off time is here defined as the duration from the moment of the initial sudden drop in current to the instant when the current is 1% of the on-state current.
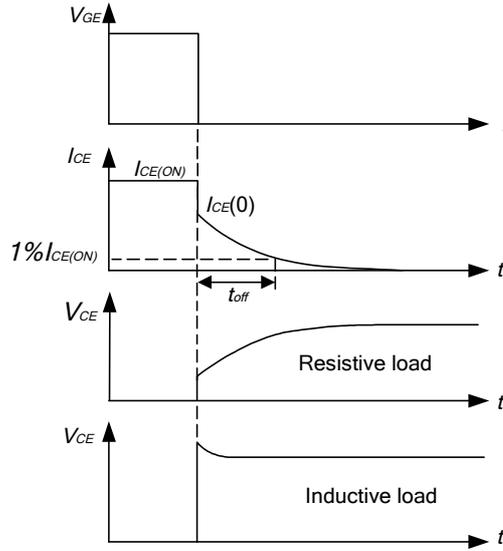
Figure 2-14 Sketched turn-off waveforms for an IGBT [2-3]

From equation (2-18), the current level just after the gate voltage is removed at the start of the tail, $I_{CE}(0)$ can be obtained from

$$\beta_{PNP} = \frac{I_{CE(ON)} - I_{CE}(0)}{I_{CE(ON)}}$$ (2-23)

where β_{PNP} is the common-emitter current gain of the P base-N⁻ drift- P⁺ collector transistor

inside the IGBT, $= \frac{\alpha_{PNP}}{1 - \alpha_{PNP}}$. (2-24)

After the initial sudden drop, the collector current decays exponentially at a rate determined by the lifetime of minority carriers. The tail current waveforms may be represented by [2-14, 15]

$$i_{CE}(t) = I_{CE}(0) \exp\left(\frac{-t}{\beta_{PNP}\tau_B}\right)$$ (2-25)

where τ_B is the base transit time and is given by

$$\tau_B = \frac{[\gamma(b+1) - 1][1 - \sec h(d_N / L_a)]\tau_a}{2\gamma - [\gamma(b+1) - 1][1 - \sec h(d_N / L_a)]}$$ (2-26)

Here, γ is the injection efficiency, and b is the mobility ratio (μ_n / μ_p) [2-2].

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In the case of symmetrical high voltage devices with fast switching speed, the diffusion length L_a is small compared with the base width d_N and the injection efficiency γ is close to unity [2-4]. The parameter τ_B becomes

$$\tau_B = \frac{b\tau_a[1 - \sec h(d_N / L_a)]}{2 - b[1 - \sec h(d_N / L_a)]} \qquad (2\text{-}27)$$

From (2-27), it can be concluded that the current tail will decay at a rate proportional to the free carrier lifetime. This is consistent with the observed reduction in the turn-off time with increasing electron radiation dose [2-4].

2. 3. 6 Temperature effects

One of the important characteristics of the IGBT is its excellent high temperature forward conduction characteristics. This feature makes the device attractive for high temperature operations. Devices have been operated successfully with heat sink temperatures approaching 200 °C. However, to take advantage of this feature, the latching current density must be raised to maintain fully gate-controlled operation at high temperatures [2-3].

(a) On-state characteristics

The forward conduction characteristics of a 600 V NPT IGBT measured at elevated temperatures are shown in Figure 2-15. The detailed measurements were published in [2-16]. The on-state characteristics can be viewed as consisting of two segments: a diode drop portion followed by a resistive MOSFET portion as described in section 2.3.4 (a). The diode voltage decreases when the temperature is increased, which compensates for the increase in channel resistance. This results in a comparatively small change in overall on-state voltage with temperature; the voltage falls at low current levels due to the dominance of the diode voltage, whereas at high currents, the overall voltage increases since the MOSFET voltage becomes more dominant, shown in Figure 2-16. In contrast, for the power MOSFET, the on-

state resistance increases steeply with temperature, resulting in the need to derate the current handling capability more severely than for the IGBT.
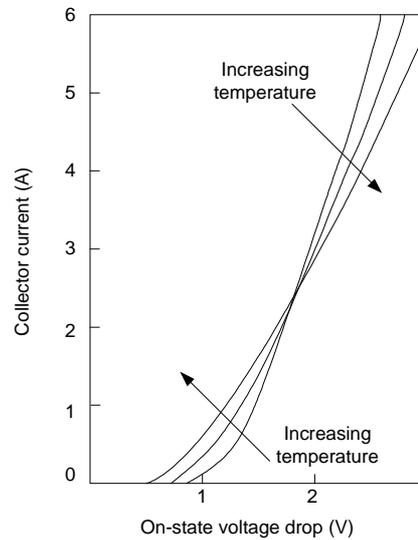
Figure 2-15 Typical variation of the on-state characteristics at elevated temperatures [2-3]
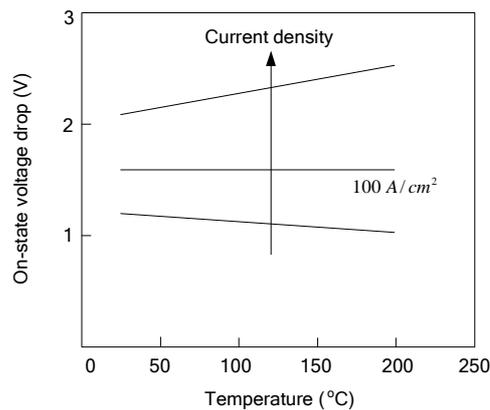
Figure 2-16 Variation of on-state voltage drop of a 600 V NPT IGBT
at elevated temperatures [2-3]

The small positive temperature coefficient of the forward drop at higher current levels observed in IGBTs is beneficial in ensuring homogeneous current distribution within chips, and for achieving good current sharing when paralleling devices [2-3].

(b) Forward blocking characteristics

As in the case of other semiconductor devices, the collector forward blocking leakage current in the IGBT increases with increasing temperature. The leakage current arises from a

combination of the space charge generation current in the depletion region and the diffusion current. The space charge generation current is dominant at room temperature while the diffusion current becomes dominant at high temperature. A measurement of the leakage current in the temperature range of 100 to 200 °C is given in [2-16] for a typical device. The leakage current can be observed to rise gradually with increasing anode potential until breakdown. The occurrence of avalanche breakdown is confirmed by an increase in the blocking voltage capability with increasing temperature. The authors noted that the leakage current exceeded 1 mA only when the temperature was raised to 200 °C [2-16].

(c) Switching characteristics

The IGBT turn-off time is dominated by the current tail. The minority carrier lifetime increases at higher temperatures, which not only slows down the recombination process, but increases the PNP transistor gain. The latter effect produces a smaller initial current drop at turn off. The temperature effect on the turn-off current is shown in Figure 2-17. Both these phenomena cause an increase in the turn-off time with increasing temperatures.

A typical example of the measured change in turn-off time with temperature is provided in Figure 2-18 for an NPT IGBT. In this case, the turn-off time shows an approximately linear change with temperature, with a 50 percent increase between room temperature and 200 °C. Compared with the NPT device, the PT device shows a relatively small change in turn off time with temperature. This is believed to be due to the recombination of the carriers in the buffer layer, which has a higher concentration than the N-drift region for the NPT device [2-3].
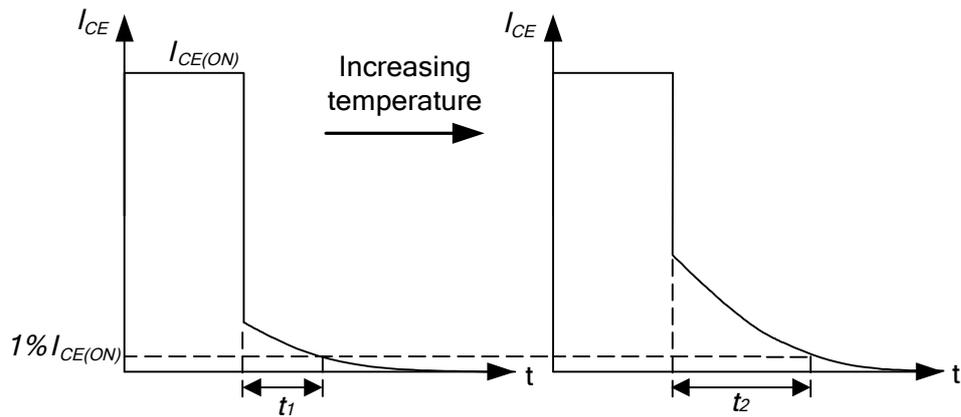
Figure 2-17 Variation in turn-off waveforms at an increased temperature [2-3]
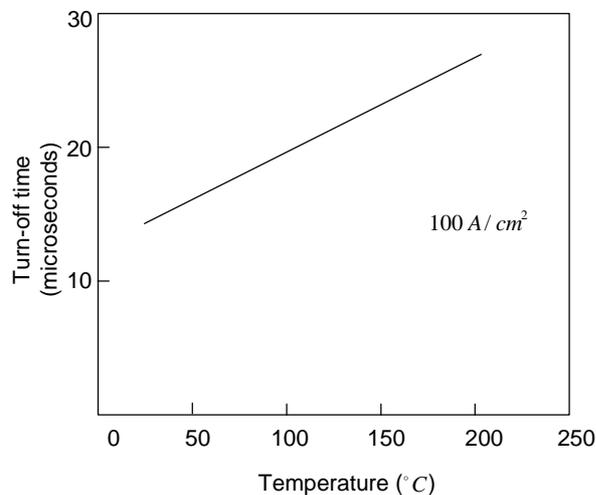
Figure 2-18 Increase in turn-off time with temperature for a NPT IGBT [2-3]

2. 4 Summary

The operation of the power diode and IGBT both rely on minority carrier diffusion. This feature makes them similar in some ways, especially the high temperature effects. At high temperatures, the diode exhibits a lower knee voltage, higher incremental resistance and higher reverse avalanche levels. Similar effects are found in IGBTs. At high temperatures, the reverse recovery process of the power diode becomes more pronounced, so does the tail process of the IGBT.

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The operation of power devices generally degrades at high temperature, such as the diode and IGBT switching characteristics explained in this chapter. The cryogenic environment may allow power devices to operate more efficiently. The cryogenic characteristics and performance of IGBTs will be carried out in the following chapters.

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Chapter 3 Characterisation of IGBT devices at cryogenic temperatures

3. 1 Introduction

This chapter describes an experimental investigation into the characteristics of three typical types of IGBT modules at temperatures ranging from room temperature to cryogenic levels. The devices selected represent three generations of IGBT technology namely, PT (Punch-Through), NPT (Non-Punch-Through) and IGBT3.

Three sets of tests have been carried out on the IGBTs: static tests, gate charge tests, and switching tests. The tests on the static and reverse recovery characteristics of the diodes within the tested modules were also carried out.

The tests were undertaken using a purpose built cryosystem comprising a temperature controlled cold head and vacuum chamber. The section 3.2 describes the design and operation of the cold chamber. The following sections describe the tests undertaken on the devices and the results.

3. 2 Test system

The test system is shown in Figure 3-1. It is built around a COOLPOWER 120 T (12) cold head from Leybold Vacuum GmbH. The cold head is in a stainless steel vacuum chamber and connected to a compressor (20) by a pair of flexlines (14). High-purity, high-pressure helium gas is compressed in the compressor and its pressure is then released in a controlled way in the cold head to generate low temperatures. A safety valve protects the cold head against excessively high helium pressure. The cold head can be cooled down to 20 K within approximately 40 minutes.

The tested sample is mounted on the cold head. A vacuum jacket surrounds the cold head and sample to prevent condensation of water vapour and heating by convection. The vacuum is provided by a two-stage pumping system: a turbo molecular pump Turbotronik NT10 (17) backed by a rotary vane pump Trivac D4B (19). The vacuum level is monitored by a vacuum gauge ITR 90 (15). The dry nitrogen supply (8) is used to release the vacuum after the experimental work to avoid condensation of water vapour.

The cold chamber has two feedthroughs for connection to the sample devices: one four-pin power feedthrough (11) for high power connections, and another 12-pin instrumentation feedthrough (13) for signal connections. The instruments (1, 2, 5, 6, and 7) are for the switching tests. A photo of the test system is shown in Appendix 1.

A sensor diode and a heater coil built in the cold head, together with a temperature control circuit (4) are employed to control the heater power supply (3), and thereby regulate the cold head temperature.

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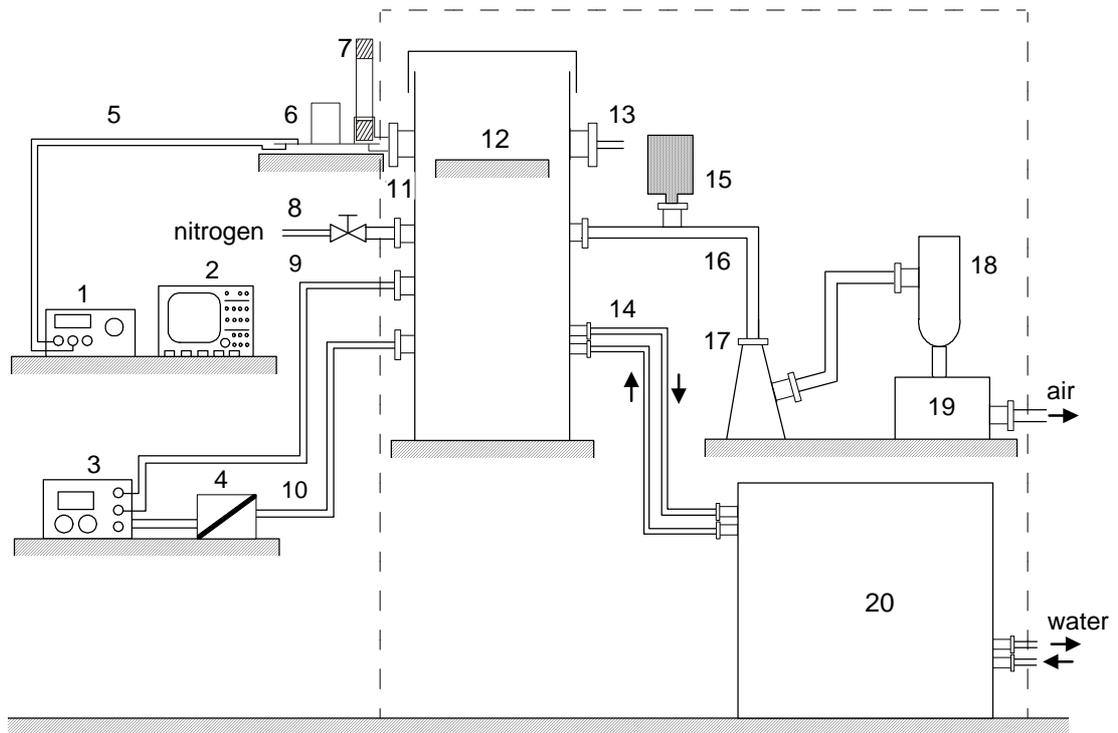
Figure 3-1 Test system arrangement (The devices inside the dash box are from
Leybold GmbH)

1 Main power supply;
2 Oscilloscope;
3 Heater power supply;
4 Temperature control circuit;
5 Power connections;
6 DC capacitors, load and gate circuit;
7 Current transformer,
8 Nitrogen valve and hose;
9 Heater leads;
10 Sensor diode leads;
11 Power Feedthrough;
12 Cold head in a lid-opened chamber;
13 Instrumentation feedthrough;
14 Helium flexline and the safety valve;
15 Vacuum gauge;
16 Vacuum hose;
17 Molecular pump;
18 Fine vacuum adsorption trap;
19 Rotary vane pump;
20 Compressor;

3. 2. 1 Cold chamber
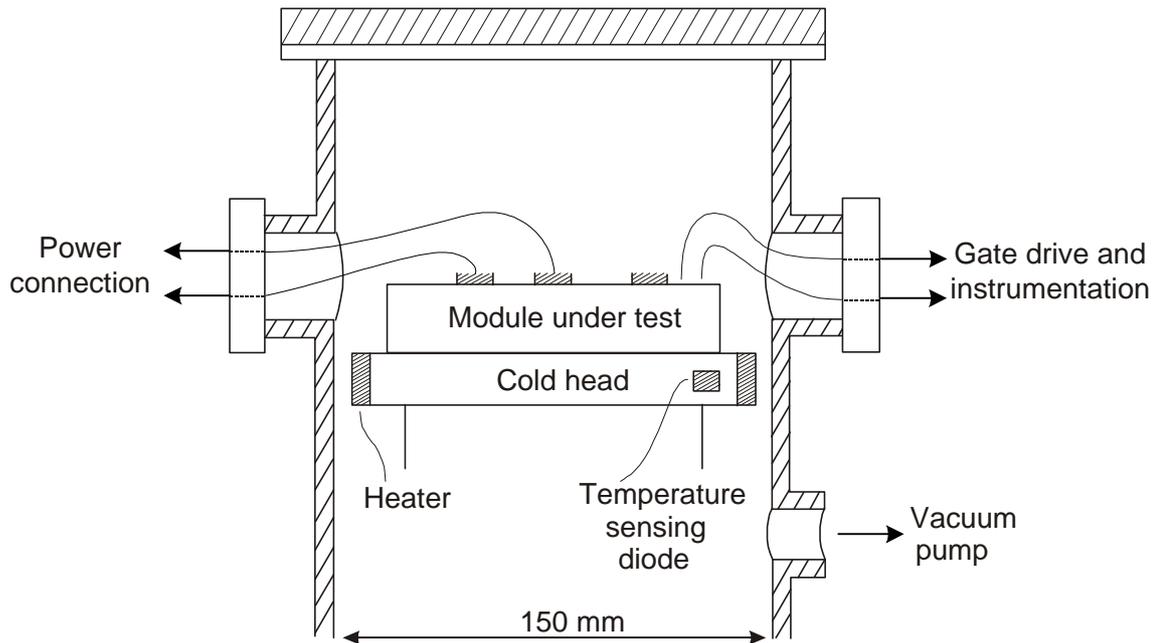
Figure 3-2 Cold chamber cross- section diagram

The Figure 3-2 shows the cross-section diagram of the cold chamber. The cold head diameter is 120 mm, allowing power modules with a 110×60 mm footprint to be accommodated comfortably. This refrigeration unit has a cooling capacity of 120W at 80K, providing the capability to operate power devices continuously at low temperature as well as undertaking single-shot tests. A photo of the cold chamber holding a device is shown in Appendix 2.

During test, the pressure in the chamber is kept at around 10^{-4} mbar. At this vacuum level voltages in the region of 600 V can be safely used in the cold chamber.

3. 2. 2 Temperature regulation

The sensor diode and heater, as shown in Figure 3.2, are key elements to regulate the cold head temperature. The sensor diode technical information is shown in Table 3-1. The cold head temperature value can be obtained by measuring the voltage across the diode, V_{diode},

when the diode current is 10 μA, and using the diode calibration curve. The heater is a coil

with a resistance of 12 Ω and a power rating of 160 W.

Item name	Silicon Diode Type D Ref. NO. 200 19 70
Manufacturer	Leybold Vacuum GmbH
Temperature range	1.4 - 330 K
Accuracy	$\pm$ 1 K, T $\in$ [2, 100] K $\pm$ 1 % $\times$ V_{diode}, T $\in$ [100, 330] K
Resistance	$V_{diode} \times 10^5$ Ω
Recommended excitation	10 μA $\pm$ 0.05 %

Table 3-1 Sensor diode specifications
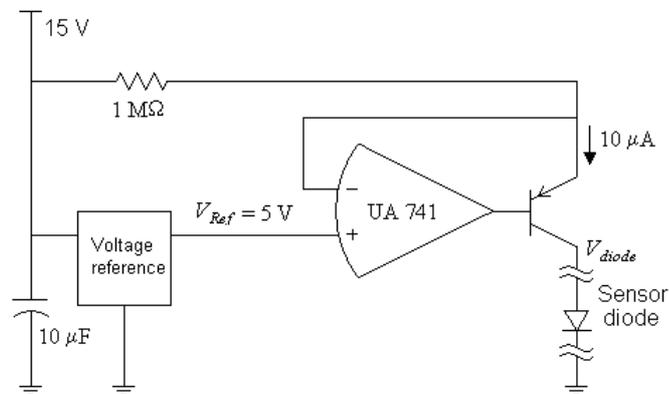
(a) Temperature measurement circuit
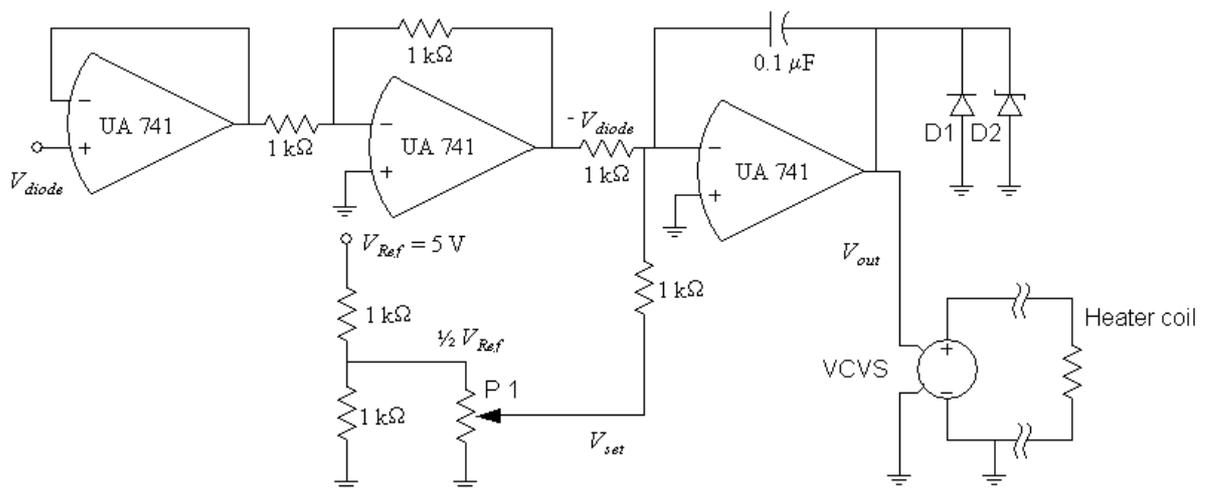
(b) Temperature control circuit
Figure 3-3 Temperature measurement and control circuits

The circuit shown in Figure 3-3(a) supplies a 10 μA current for the sensor diode. The difference between the 15 V supply and the 5 V reference is impressed across the 1 MΩ resistor, establishing a 10 μA current. The PNP transistor forms a constant current drive to the sensor diode.

The circuit shown in Figure 3-3(b) forms a simple negative feedback loop and integral controller, which supplies a controlled voltage across the heater coil to regulate the cold head temperature. The actual temperature-related signal, V_{diode}, is an input and becomes $-V_{diode}$ after a voltage follower and inverter. The temperature demand signal V_{set} is set by a potentiometer P1, which can be adjusted between 0 V and approximately $V_R/2$. The superimposed voltage signal of $-V_{diode}$ and V_{set} is processed by an integral controller, comprising a resistor, an op-amp and a capacitor. The output voltage V_{out} is employed to control the heater power supply. If the actual temperature is higher than demanded, the output of the controller tends to be negative but is clamped at approximately 0 V by the diode D1, and there is no supply to the heater. If the actual temperature is lower than demanded, the output of the controller is positive and power is delivered to the heater to raise the cold head temperature. D2 is a 7.5 V zener diode that limits the maximum heater power to approximately 150 W.

During the tests, the cold head was left for around 20 minutes at each temperature to equalize the temperature of the cold head and the tested sample. The warming-up and cooling-down processes were both measured and the same results were obtained.

3. 3 Sample IGBTs and diodes

The three tested IGBTs represent 3 generations of IGBT technology. Two IGBTs with traditional technologies, PT and NPT, are from Dynex Semiconductor Ltd. The third one with the latest IGBT3 technology is from Infineon Technologies AG, but packaged by Dynex. The IGBT3 device has a soft punch through structure and a trench gate. The electrical connections for the tested modules are shown in Figure 3-4. Each module contains a half bridge circuit, consisting of two IGBTs and two anti-parallel diodes. The details of the tested devices are given in Table 3-2.
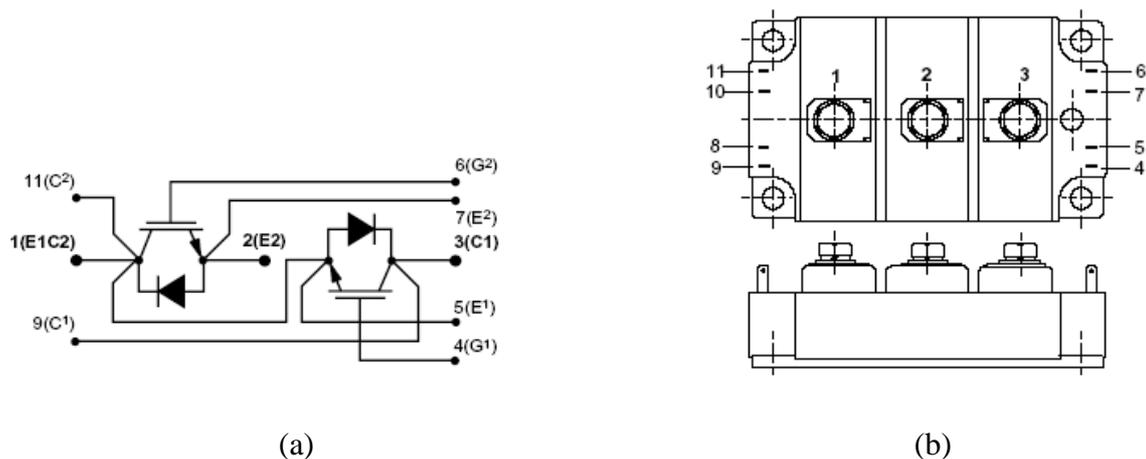
(a)   (b)
Figure 3-4 Electrical connection for the tested modules
(a) circuit diagram; (b) package profile

Device	Type	Manufacturer	Voltage rating /V	Current rating (70°C) /A
GP350MHB06S	PT	Dynex	600	350
DIM200MHS17-A000	NPT	Dynex	1700	200
SIGC186T170R3	IGBT3	Infineon	1700	150

Table 3-2 IGBT specifications (from the corresponding datasheets)

For the PT and NPT modules, there are two IGBT dies in each IGBT and diode arm to provide a high current capacity. As for the IGBT3 module, there is a single die in each arm. That is why the IGBT3 rated current is lower.

In order to operate the devices successfully at cryogenic temperatures it was found to be necessary to use modules that were not filled with the usual protective gel. This is because the normal gel appeared to degrade below 200 K, resulting in electrical discharges occurring around the edges of the die, which produced device failure. Gel free modules were specially made for cryogenic tests by Dynex semiconductor Ltd.

Apart from the three modules, special samples, each comprising two IGBT chips and two diode chips, were provided by Dynex semiconductor Ltd to carry out the breakdown characteristics test.

3. 4 Measurement of static characteristics

A programmable high power curve tracer, Tektronix 371 B, was used to examine the static characteristics of the devices, including the on-state voltage and collector-emitter breakdown voltage. This instrument can be applied to make high power measurement of semiconductor devices: up to 3000 Volts, 400 Amps and 3000 Watts. Its technical information is shown in Table 3-3.

	High Voltage Mode				High Current (pulsed) Mode	
Peak Power	30 mW	300 mW	3 W	30 W	300 W	3 kW
Collector Peak Current	0.4 mA ±20%	4 mA ±20%	4 mA ±20%	40 mA ±20%	40 A	400 A
Maximum Peak Voltage	300 V + 15% − 0%	300 V + 15% − 0%	3 kV + 10% − 0%	3 kV + 10% − 0%	30 V + 10% − 5%	30 V + 10% − 5%

Table 3-3 Curve tracer information

For the on-state characteristics test, the curve tracer was set in the high current mode, the device collector and emitter were connected to the curve tracer through the power

feedthrough; the step generator was set according to the desired gate voltages and the gate pins were connected to the curve tracer through the instrumentation feedthrough.

For the forward blocking characteristics test, the curve tracer was set in the high voltage mode, the device collector and emitter were connected to the curve tracer through the power connection feedthrough; the gate and emitter pins were shorted together.

3. 4. 1 On-state characteristics

(a) Rated current region

The gate-emitter voltage was varied from 5 V to 15 V, in steps of 2 V and the collector-emitter voltage from 0 V to 10 V. With this setting, the on-state characteristics up to a current level of 150 A, close to the maximum continuous current rating, were tested from room temperature down to 50 K in steps of 25 K.

The on-state results at room temperature for the three tested devices are shown in the left side of Figure 3-5. From the test results, the on-state voltages corresponding to a current level of 100A and gate voltage of 15 V were extracted. The total voltage drop V_{CE} is divided into two parts: the knee voltage, and the remaining voltage, corresponding to the voltages across the series-connected rectifier and MOSFET components in the simple IGBT model.

The on-state voltage drop variation with temperature is shown in the right side of Figure 3-5 for the three tested devices. The results show that the voltage drops of three devices fall at low temperatures and have minimum values at approximately 100 K. The increase in the on-state voltage at very low temperatures was attributed to freeze-out effects. There is a small

reduction in the on-state voltage of the 600 V PT IGBT, from 1.40 V at room temperature to 1.30 V at 100 K. As for the two 1700 V devices, the on-state voltage of the IGBT3 device at room temperature, 1.7 V, is as expected significantly lower than the corresponding value for the NPT device, 2.1 V. Both voltages fall at lower temperature, however, the on-state voltage of the NPT device is seen to have a greater sensitivity to temperature. These two 1700 V devices have very similar on-state voltages for temperatures in the region of 100 K, the values being around 1.5 V.
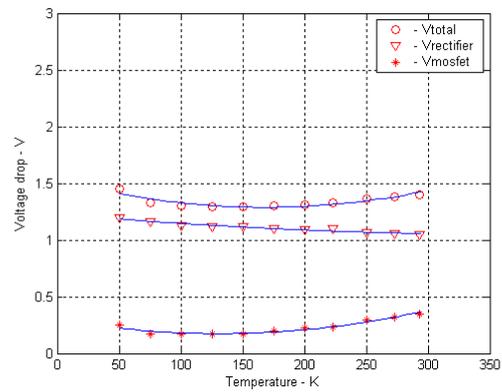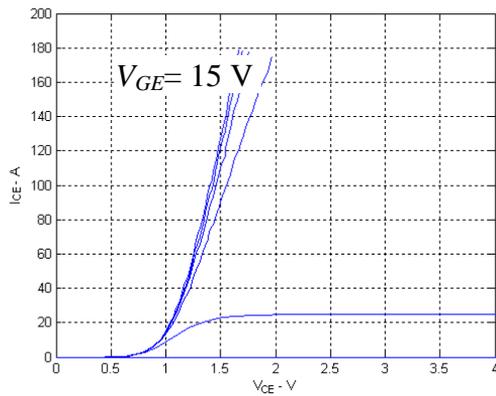
(a) 600 V PT IGBT
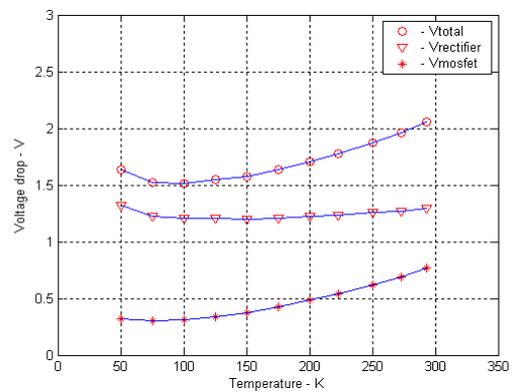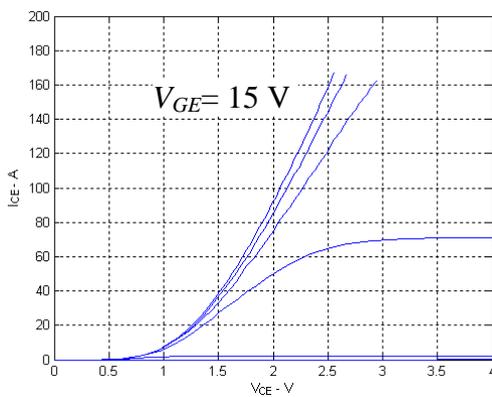
(b) 1700 V NPT IGBT
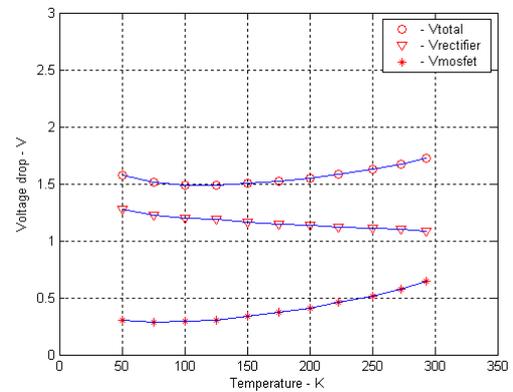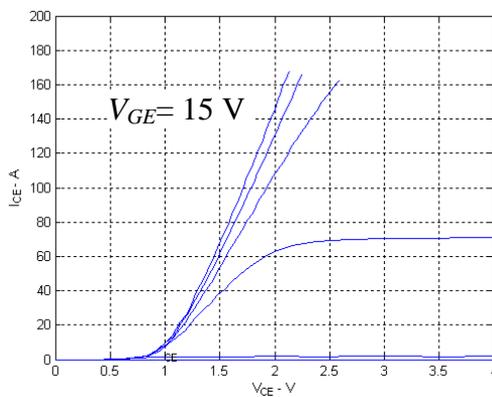
(c) 1700 V IGBT3

Figure 3-5 On-state voltage drops at 100A from 50 K to 300 K
Left: samples at room temperature; V_{GE} =5, 7, 9, 11, 13, 15 V;
Right: on-state voltage drop variation at low temperatures, V_{GE}=15 V

The MOSFET component of on-state voltage in the three devices reduces very significantly,

by a factor of approximately two at 100 K. However, the variations of the rectifier

component of the voltage drops are different: the rectifier component of voltage in the NPT

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device varies very little, whereas the values for the PT and IGBT3 devices increase approximately linearly by around 20% as the temperature falls from 300 K to 50 K.

(b) The subthreshold region

The gate-emitter voltage was set from 5 V to 8 V in steps of 0.5 V and the collector-emitter voltages ranged from 0 V to 5 V. With this setting, the on-state characteristics in the subthreshold region were tested from room temperature down to 50 K. Figure 3-6 shows the results at room temperature and 100 K for all three IGBTs. It can be seen that temperature strongly influences the IGBT performance in the subthreshold region.

From the on-state results in the subthreshold region, the DC transfer characteristics I_{CE} against V_{GE} are extracted for $V_{CE} = 1.2$ V, as shown in Figure 3-7.
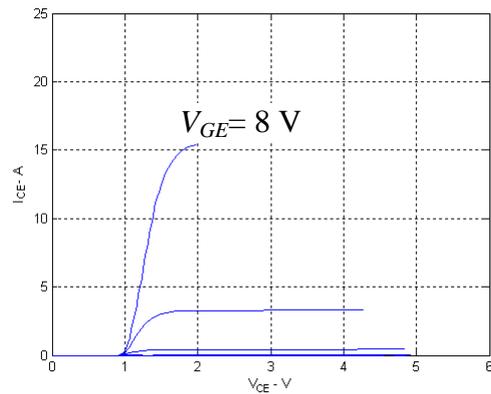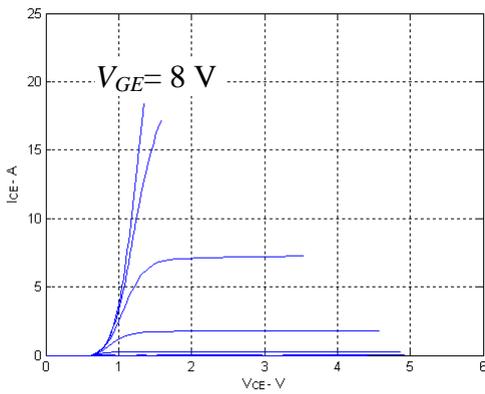
(a) 600 V PT IGBT. Left: room temperature, right: 100 K
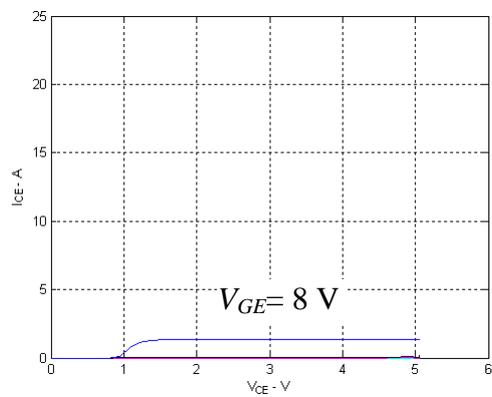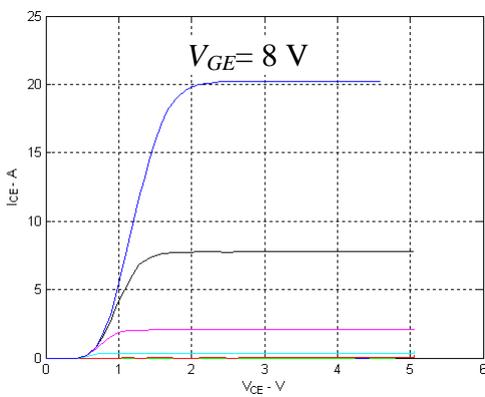
(b) 1700 V NPT IGBT. Left: room temperature, right: 100 K
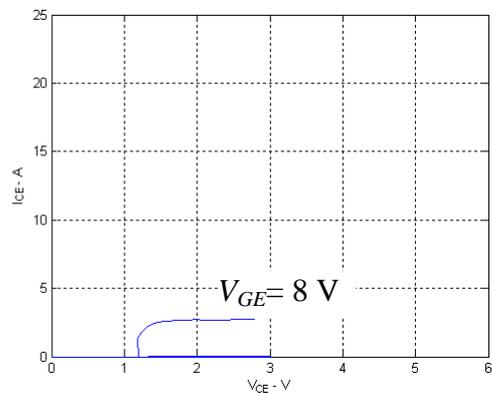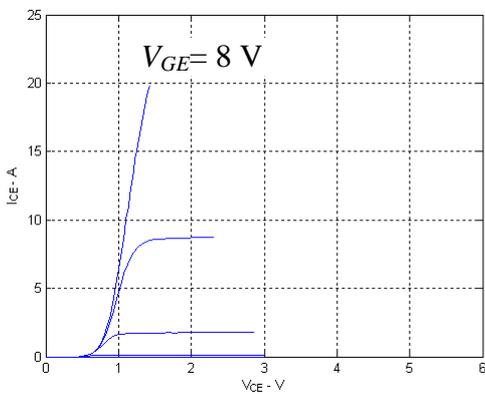
(c) 1700 V IGBT3. Left: room temperature, right: 100 K
Figure 3-6 On-state characteristics in the subthreshold region
V_{GE}: from 5 V to 8 V in steps of 0.5 V
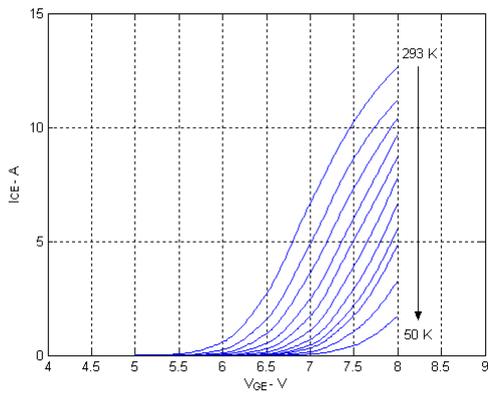
(a) 600 V PT IGBT   (b) 1700 V NPT IGBT
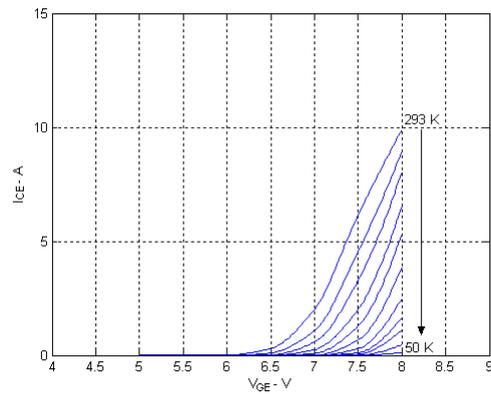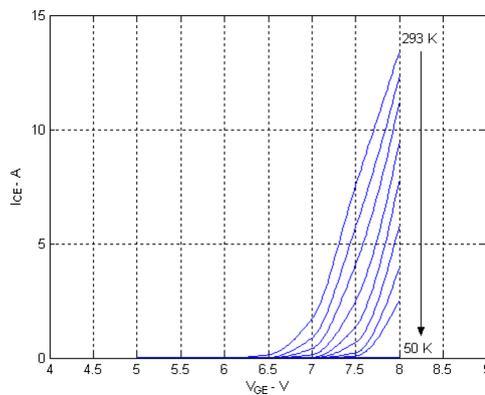
(c) 1700 V IGBT3

Figure 3-7 DC transfer characteristics at V_{CE}=1.2 V

The gate-emitter threshold voltage is assumed to correspond to a collector current of 10 mA. The values of the threshold voltage were extracted from the measurements and plotted in Figure 3-8 for the three tested devices. As temperature increases, the threshold voltages for all three devices were found to decrease at the rate of approximately 7 mV/K. This rate is close to the power MOSFET threshold voltage variation rate in the normal temperature region, 6 mV/K [3-13].
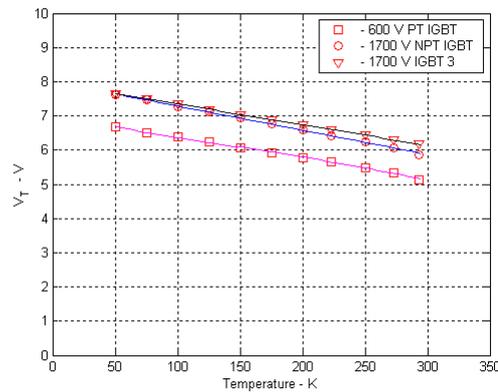
Figure 3-8 Threshold voltage variations from 50 K to room temperature

3. 4. 2 Forward blocking characteristics

The measurements of the forward blocking characteristics of the three devices at room temperature are shown in the left side of Figure 3-9. The breakdown voltages are marked with '∇', and correspond to the points where the leakage current begins to increase sharply. Such measurements were carried out from room temperature down to 50 K in steps of 25 K.

The variation in the forward breakdown levels with temperature is shown in the right side of Figure 3-9. The breakdown voltages of the PT and NPT IGBT decrease gradually with temperature reducing from 900 V to 600 V for the PT device and from 2000 V to 1400 V for the NPT device, approximately 30% reduction. However, the breakdown voltage of the IGBT3 reduces from 1900 V at room temperature to 700V at 50 K, approximately 60% reduction. From room temperature to 200 K, the IGBT3 device exhibits a similar variation in breakdown voltage to the other two devices, but a very dramatic reduction occurs below 200 K. A similar variation in breakdown voltage has been observed from experimental investigation in other IGBT devices that also possess a field stop layer, including devices that do not have a trench gate structure. It is therefore thought that the field stop layer is

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responsible for the sharp drop in breakdown voltage in the IGBT3 device at low temperatures.
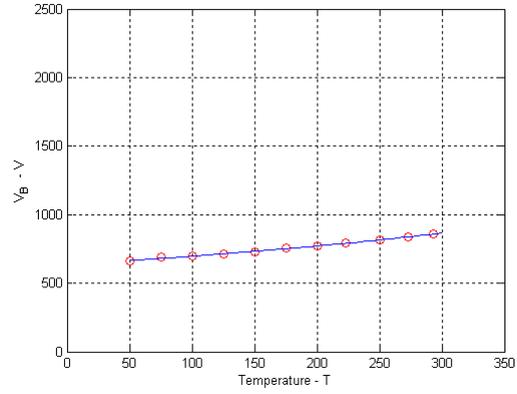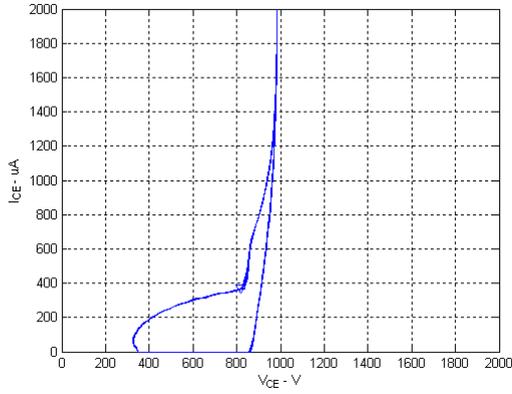
(a) 600 V PT IGBT
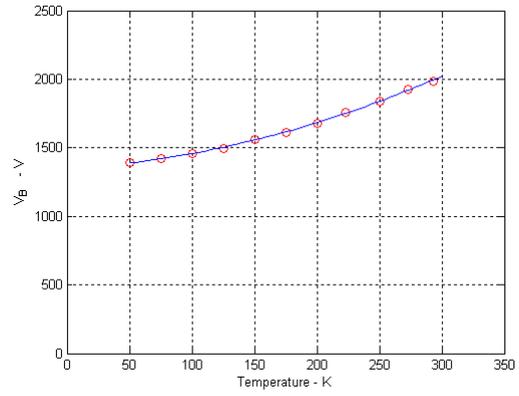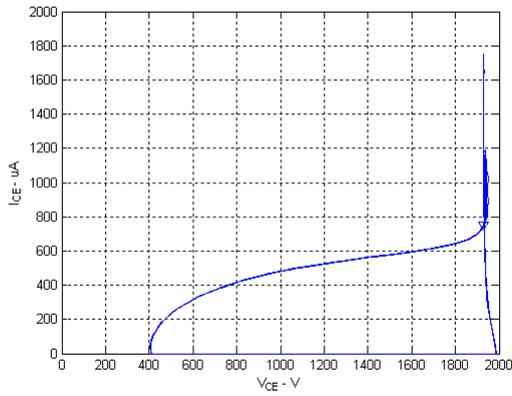
(b) 1700 V NPT IGBT
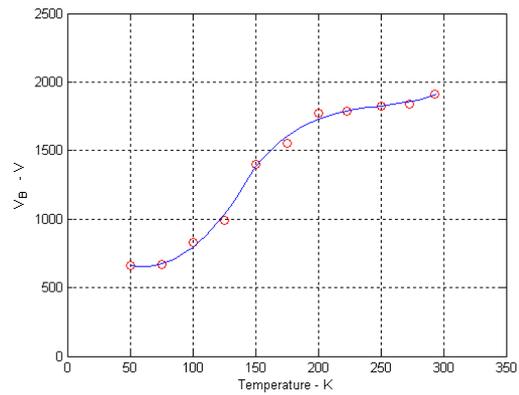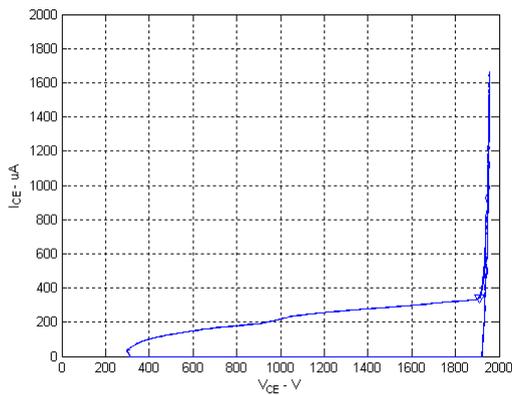
(c) 1700 V IGBT3

Figure 3-9 Measurements and temperature dependence of forward breakdown voltage
(the breakdown points are marked with '∇')
Left: measurements at room temperature;
Right: breakdown voltage variation with temperature

3. 5 Gate parameters

The gate resistance R_G and the parasitic capacitances between gate and emitter, C_{GE}, and gate and collector, C_{GC}, shown in Figure 3-10, are key elements in determining the switching behaviour of an IGBT. The variation of these elements with temperature is examined in this section using standard test methods.
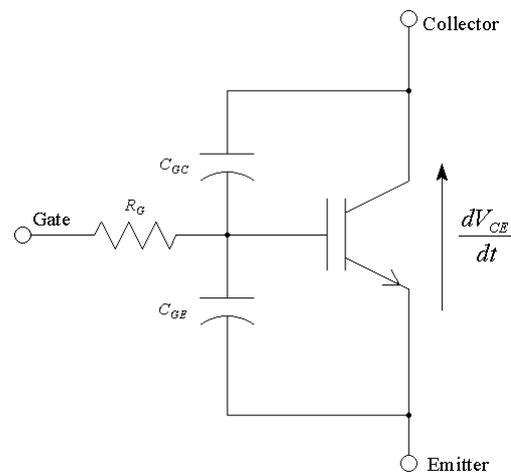
Figure 3-10 IGBT gate resistance and parasitic capacitances

3. 5. 1 Gate resistance

The two IGBT modules from Dynex Semiconductors Ltd, the 600 V PT IGBT and the 1700 V NPT IGBT, use a silicon resistor in series with each gate. However, the module containing the Infineon device uses a surface mounted thick film resistor. Two special samples, each comprising several gate resistors on a base plate, were provided by Dynex Semiconductor Ltd allowing tests to be made on the gate resistors.

The samples were mounted on the cold head and the resistance was measured by a digital multimeter outside the cold chamber. Figure 3-11 shows the variation of the two resistances with temperature.

The silicon resistance shows a dramatic reduction, from 6.2 Ω at room temperature to 0.6 Ω at 50 K, approximately 90 % drop. The resistance of the gate resistor in the IGBT3 module increases linearly from 50 K to 300 K. The variation is quite small compared with the silicon resistance, around 20 %, from 4.9 Ω at room temperature to 4.0 Ω at 50 K.
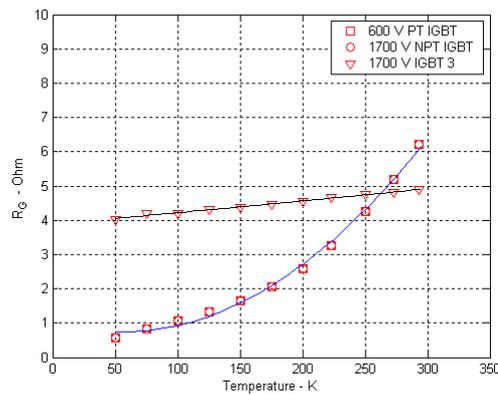
Figure 3-11 Temperature characteristics of gate resistors

According to power MOSFET theory, the gate resistance has great influence on the turn-on transient. Both the turn-on delay time and the transit time required for the current to rise from zero to full current level are related with the gate resistance. The larger the resistance, the longer the delay time and the transit time [3-13]. Therefore the turn-on transient at low temperatures is likely to be influenced by the reduction of the gate resistance.

3. 5. 2 Gate capacitance

(a) Gate charge test theory

Figure 3-12 is the test circuit schematic for testing an n-channel device. Polarities are simply reversed for a p-channel device. A pulsed constant current source is employed to drive the device under test. A resistive load is used to explain the gate charge test theory. The gate charge is the integration of the pulse current with respect to time. The experimental gate test circuit is a practical embodiment of Figure 3-12, which is given in Appendix 3.
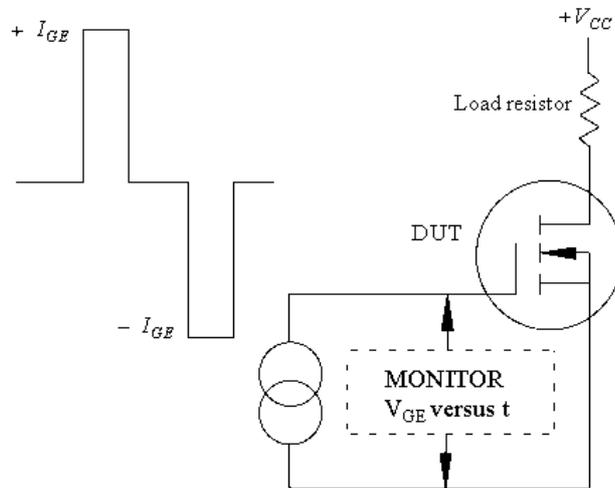
Figure 3-12 Gate charge test diagram, $Q_{GE} = I_{GE} \times t$ [3-14]

Figure 3-13 (a) shows the idealized gate charge waveforms during a typical turn-on transient. For purposes of illustration, the nonlinearity of the parasitic capacitances is not considered, so the collector current and voltage waveforms change in a linear manner.

$Q_{GE\ (th)}$ is the charge that must be supplied to reach the gate-source threshold voltage. It establishes a linear locus through the origin of a $Q = f\ (V_{GE})$ graph that is invariant with I_{CE} and $V_{CC.}$ The gate-emitter capacitance is calculated as

$$C_{GE} = \frac{Q_{GE(th)}}{V_{GE(th)}} = \frac{I_{GE} \times (t_1 - t_0)}{V_{GE(th)}} \tag{3-1}$$

V_{GP} is the gate voltage necessary to for the device to conduct the full load current.
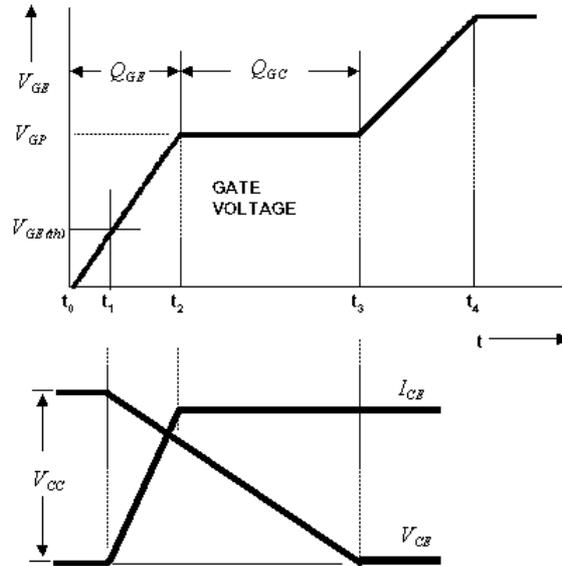
(a) Idealized gate charge waveforms [3-13, 14]
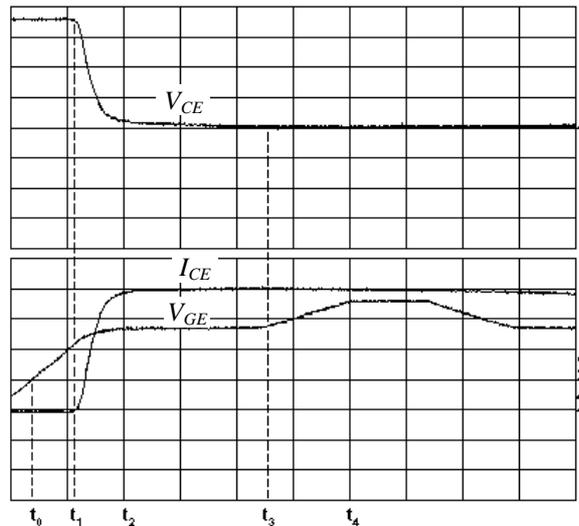
(b) Practical gate charge waveforms
1- V_{CE} 100 V/div; 3- V_{GE} 5 V/div; 4 - I_{CE} 50 A/div
Figure 3-13 Gate charge waveforms

Q_{GC} is the charge supplied to the collector from the gate to change the collector voltage under constant collector current. It is variant with V_{CC} and may be considered invariant with I_{CE}. It is related to an effective gate-collector capacitance as follows [3-14],

$$C_{GC} = \frac{Q_{GC}}{V_{CC}} = \frac{I_{GE} \times (t_3 - t_2)}{V_{CC}} \qquad (3\text{-}2)$$

Figure 3-13 (b) shows the practical gate charge waveforms. The practical gate-emitter voltage V_{GE} and collector current I_{CE} waveforms are the same as the idealized ones. However, the fall of the collector voltage V_{CE} slows down once $V_{CE} < V_{GE}$. This is caused by the nonlinearity of the gate-collector capacitance, which increases sharply as the collector voltage falls below the gate voltage forming an accumulation layer at the surface of the n⁻ drift region [3-13]. According to (3-1) and (3-2), the discrepancy between the idealized and ideal collector voltages does not affect the gate charge test results.

(b) Gate charge test results

To make the transition time from off to on-state or vice versa to be in the order of 50 µs, a pulse current generator with an output capacity of 4.25 mA was built to drive the tested IGBTs.

To measure the charge $Q_{GE\,(th)}$ and calculate C_{GE}, the collector current was set at 100 mA for all the three tested devices. The off-state collector voltage was selected as 350 V for the 600 V device and 600 V for the two 1700 V devices, the load resistor was selected as 3.5 k Ω and 6 kΩ respectively. From the test results, $Q_{GE\,(th)}$ was obtained. Using equation (3-1), the capacitance C_{GE} was calculated.

To measure the gate voltage V_{GP} at the continuous rated collector current level, the operation current was selected as 200 A. The off-state collector voltage was selected as 350 V for the 600 V device and 600 V for the two 1700 V devices, therefore the load was selected as 1.7 Ω and 3.0 Ω respectively. From the test results, the charge Q_{GC} was obtained. Using (3-2), the capacitance C_{GC} was calculated.

Figure 3-14 shows the gate capacitance variations against temperature. It can be seen that both the gate-emitter capacitances and the gate-collector capacitances, change very little over the temperature range from 50 K to 300 K. The variation of the gate-emitter capacitances is less than 5%, and that of gate-collector capacitances is less than 10%.
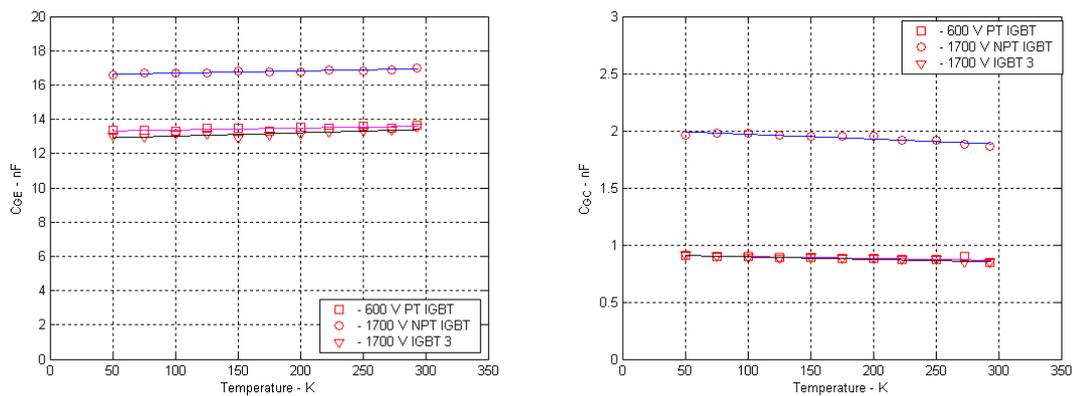
Figure 3-14 Gate capacitance variation against temperature
Left: gate-emitter capacitance; right: gate-collector capacitance

3. 6 Switching characteristics

Based on a double-pulse test circuit, the switching characteristics of the three IGBTs were tested at a current level of approximately 100 A from 50 K to 300 K in steps of 25 K. The turn-off characteristics will be analysed later in this section. The turn-on process is related to the reverse recovery characteristics of the free-wheel diodes, which will be analysed in 3. 7.

3. 6. 1 Switching test circuit

Figure 3-15 shows the electrical circuit for the switching tests. The lower IGBT and the upper diode are used in the switching test, and the gate and emitter of the upper IGBT are clamped together to disable the device. A ±15 V rectangle signal is used as the gate drive for the lower IGBT. Single-shot switching tests are used in which the lower IGBT is switched on

and off twice, allowing measurements to be made of the turn-on and turn-off inductive switching waveforms. The device voltage is measured using a high performance differential amplifier DA1850A from LeCroy, allowing the on-state voltage to be monitored accurately. The current is monitored immediately outside the chamber using a 20 MHz Pearson current transformer model 110. All the signals are recorded by a LeCroy digital oscilloscope LT354.

The electrical connection for the switching tests is shown in Figure 3-16. Low inductance, planar bus bars are used to bring the power connections out of the chamber. The DC link capacitors and the load inductor are also located outside the chamber. More details about this circuit will be introduced in the following sections. The DC power supply voltages are 300 V for the 600 V device and 600 V for the 1700 V devices.
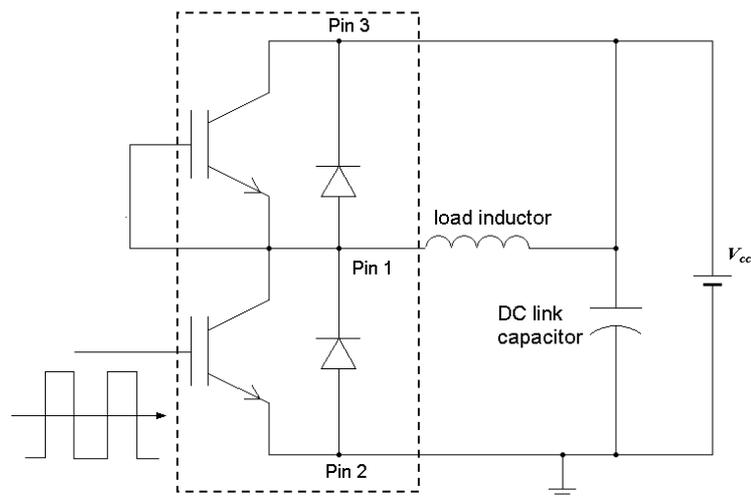
Figure 3-15 Switching test circuit
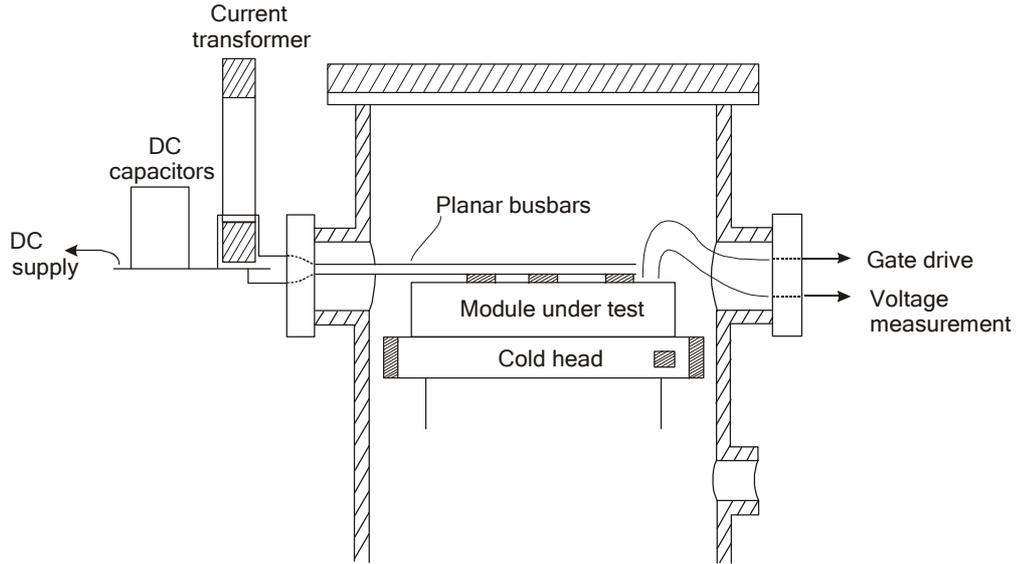
Figure 3-16 Electrical connection for switching tests

(a) Bus bars

To reduce the stray inductance in the circuit, two planar bus bars are used to connect the test module to the outside circuit. Considering the shape and size of the cold chamber, the planar bus bars shown in Figure 3-17 were used. The bus bars consist of 0.38 mm copper strip insulated by two layers of Kapton tape, the total insulation thickness between the bus bars being approximately 0.15 mm. The upper and lower bus bars are connected to pin 2 and pin 3 on the test module.

To calculate the stray inductance, each bus bar was assumed to be a 130 mm (l) long and 30 (w) mm wide rectangular copper sheet. The internal inductance of two bus bars can be estimated as [3-15]

$$L_i = \frac{\mu_0 \mu_r}{8\pi} l \tag{3-3}$$

According to [3-16], the geometric mean distance between the two bus bars can be calculated

$$x_d = 0.22313 \times w \tag{3-4}$$

The external inductance of two bus bars is given by [3-16]

$$L_e = 0.002l \left\{ \log_e \left(\frac{l}{x_d} + \sqrt{1 + \frac{l^2}{x_d^2}} \right) - \sqrt{1 + \frac{x_d^2}{l^2}} + \frac{x_d}{l} \right\} \qquad (3\text{-}5)$$

The total stray inductance is therefore:

$$L_t = L_i + L_e \qquad (3\text{-}6)$$

For this case, the whole stray inductance was approximately 80 nH. This figure was confirmed by measurements of the switching transients. A sample turn-off switching result is shown in Figure 3-18. In this case, the voltage overshoot at turn-off is approximately 60 V, and the di /dt is –0.68 A/ns, confirming that the stray inductance is around 88 nH.
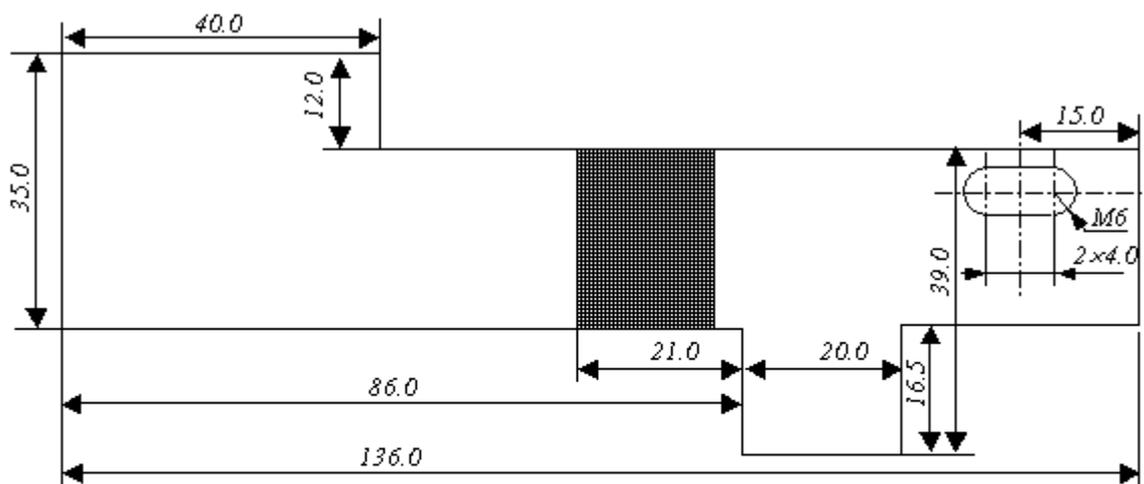
(a) The upper bus bar
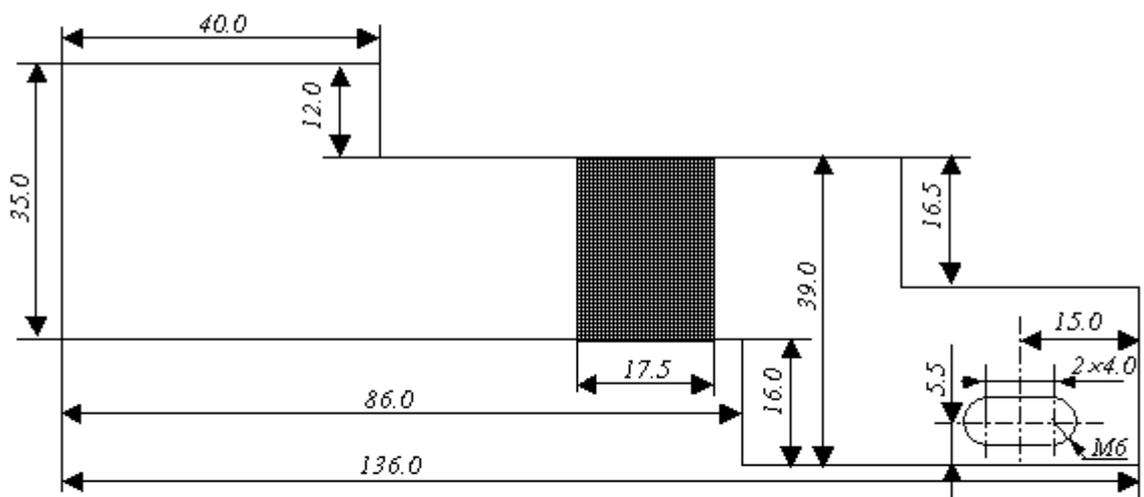
(b) The lower bus bar
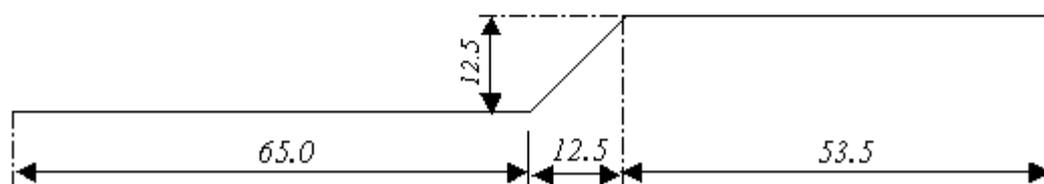
(c) The bus bar bending (front view)

Figure 3-17 Diagram of bus bars –all dimensions are in mm
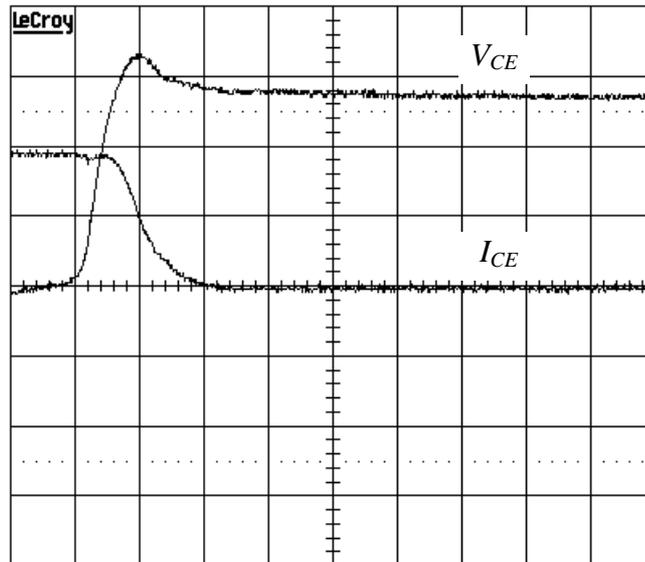
Figure 3-18 A sample of switching test results
Time: 0.2 µs/div, I_{CE}: 50 A/div, V_{CE}: 100 V/div

(b) Load inductor

To ensure that the stray inductance within the module does not cause errors in the measured on-state voltage, the load inductor must be made sufficiently large to limit the di/dt during IGBT conduction. A load inductor of 200 µH was selected, giving a rate of rise of on-state current of 3 A/µs with a 600 V supply. An IGBT conduction time of 33 µs would therefore be required for the load current to rise from 0 to 100 A. To avoid saturation effects, an air cored inductor was used, the winding consisting of eight parallel strands of 0.71 mm diameter copper wire wound on a wooden bobbin.

(c) Gate circuit and DC link capacitors

The gate drive circuit used was supplied by Dynex Semiconductor Ltd. Its circuit diagram is shown in Appendix 4. Using this gate circuit a double-pulse ± 15 V gate signal can be generated to drive the tested devices. A sample result of a double-pulse test is shown in Figure 3-20. The turn-on and turn-off processes of the second pulse are studied.
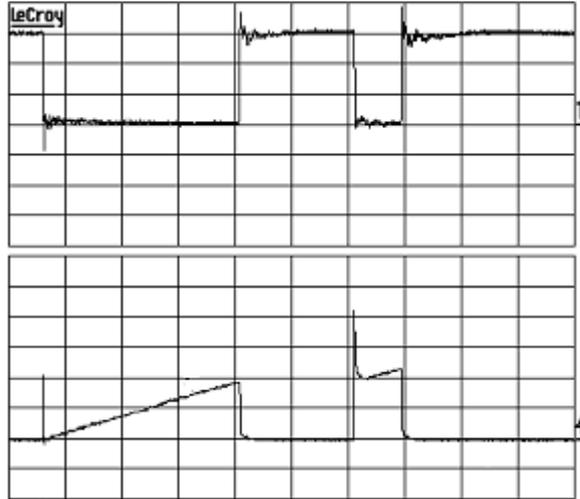
Figure 3-19 Sample results for switching measurements on an IGBT
Upper trace V_{CE}, 200 V/div, lower trace I_{CE}, 50 A/div, 10 µs/div.

The DC link capacitors are selected to maintain a stable DC voltage and supply enough charge for the single-shot tests. To limit the ripple voltage on the DC link capacitors to be less than 5% of the DC supply voltage requires a capacitor value of:

$$C = \frac{\Delta Q}{\Delta V} = \frac{I \times \Delta t}{5\% \times V_{cc}} = \frac{100 \times 10}{5\% \times 600} \mu F \approx 33.33 \mu F \qquad (3\text{-}7)$$

Four 10 µF, 630 V DC capacitors from BC components were selected as DC link capacitors.

(d) Buffer circuit

Since a low current power supply was used for the DC link, 600 V × 1.7 A, a buffer circuit consisting of a L-C filter was used to limit the peak current pulse that was drawn from the supply, as shown in Figure 3-20.
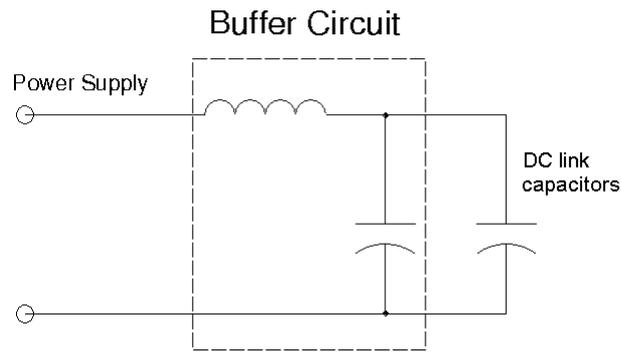
Figure 3-20 Buffer circuit

One 8.6 μH inductor and two series connected 450 V, 1200 μF capacitors were selected as components for buffer circuit.

3. 6. 2 Switching test results

The details of the device turn-off currents and voltages at room temperature 293K and at 100 K for the three IGBTs are shown in Figure 3-21, 22 and 23. The most obvious feature of the results is that there is a substantial reduction in the duration of the turn off tail current in all devices at low temperatures. The 600 V PT device shows much shorter tails and lower switching losses, than the NPT and IGBT3 devices. Moreover, the reduction of the wafer thickness and therefore of the charge stored in the IGBT3 device leads to shorter current tails and lower turn-off losses than in the NPT device.
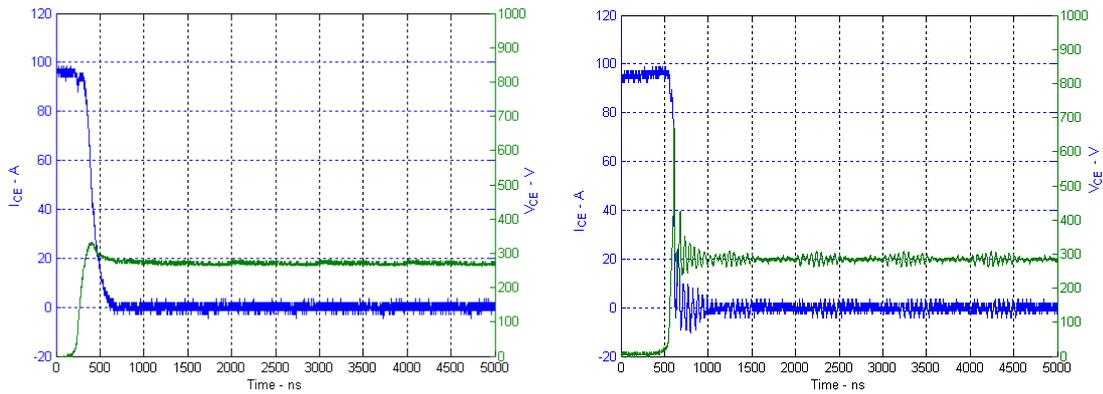
(a)   (b)

Figure 3-21 PT IGBT turn-off current, (a) room temperature and (b) 100 K
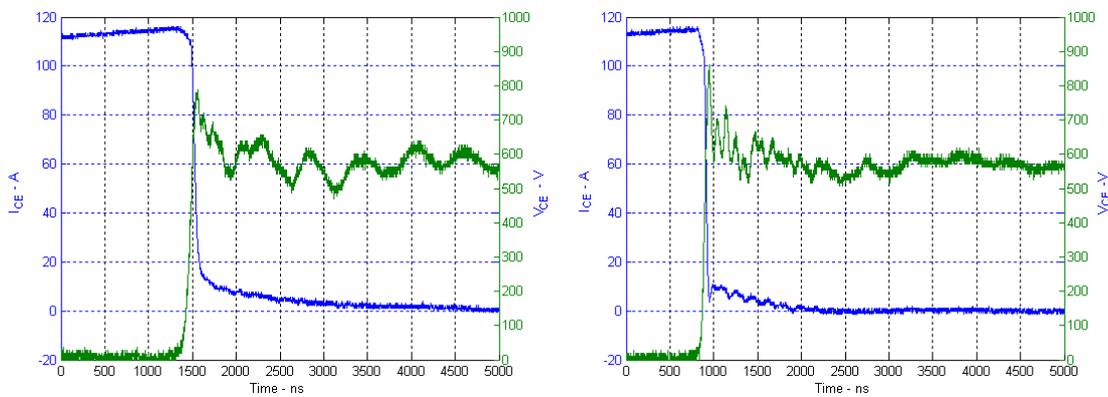
(a)   (b)

Figure 3-22 NPT IGBT turn-off current, (a) room temperature and (b) 100 K
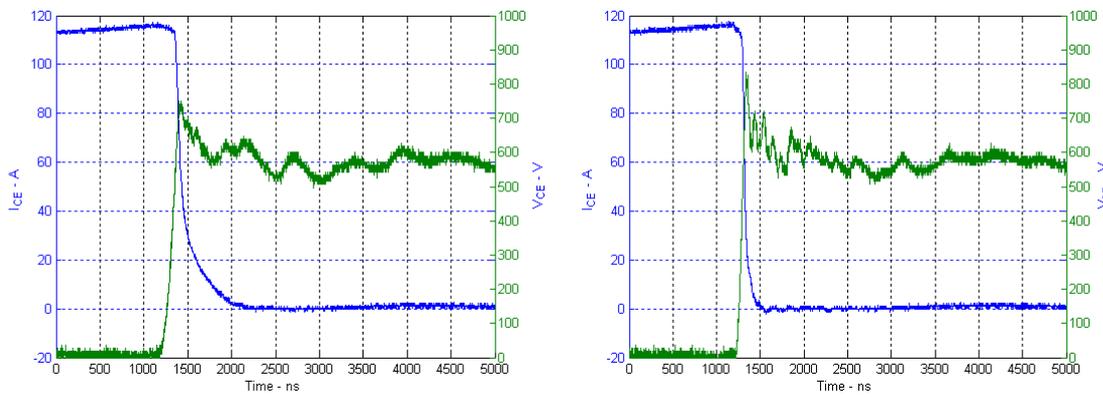
(a)   (b)

Figure 3-23 IGBT3 turn-off current, (a) room temperature and (b) 100 K

The total turn-off time may be divided into two parts: the first is the current fall time, and the second is the tail time. The former part corresponds to the sudden drop in the turn-off current, and is related to the gate resistances and the capacitances of the IGBT chips, and the

latter part corresponds to the gradual current decrease after the sudden drop, and is mainly determined by the IGBT structure, stored carriers and carrier lifetime as described in section 2.3.5. The end of the current tail is normally taken to be the point at which the current falls to 1% of the on-state level.

The di/dt for the initial current drop and turn-off times are shown in Figure 3-24 for all three devices over the temperature range down to 50 K. The turn off time is divided into two components, the duration of the initial rapid drop and the subsequent tail time. All the three devices have much greater di/dt at low temperatures partly due to the decrease of the gate time constant $R_G C_{GC}$. At room temperature the current drop for the PT device is quite gentle, but becomes very steep at low temperatures. The two 1700 V devices show a similar variation of di/dt at low temperatures.

The results show that the turn-off times of these three devices reduce significantly from room temperature down to 150 K by a factor of between two and three. Below 150 K, the turn off times become less sensitive to temperature. However, the turn-off transients are quite different in these three devices. In the lower voltage component the variation in the initial fall time appears to be the dominant effect, reducing by a factor of almost six as the temperature falls to 50 K. In the higher voltage devices the initial fall time is a very minor part and the tail time dominates.

The comparison of the turn-off losses is shown in Figure 3-25. The losses were calculated using a LeCroy oscilloscope to multiply the instantaneous voltage and current then integrate over the switching transient.

All the three devices have dramatically lower switching losses at reduced temperatures. The total switching loss is the sum of the turn-on and turn-off losses. At cryogenic temperatures, the switching losses are reduced by a factor of approximately three compared with the values at room temperature.

With shorter tails, all the devices have lower turn-off switching losses at low temperatures. The turn-off loss of the 600 V PT device decreases gradually with reduced temperatures to approximately 1/3 of its room temperature value at 75 K. The turn-off loss of the IGBT3 device is around 20% less than the NPT device's at room temperature and the difference increases as the temperature is reduced. In the region 100 K to 150 K the turn-off losses in the IGBT3 device are around 30-40% lower than those in the NPT device.

The turn-on loss is related to the diode reverse recovery process. The turn-on loss for the 600 V PT device is very small compared with the turn-off loss. The turn-on switching losses for the two 1700 V devices are larger than their turn-off losses at each temperature and decrease gradually with decreased temperatures, which is related with the reverse recovery variation and will be described in section 3.7.
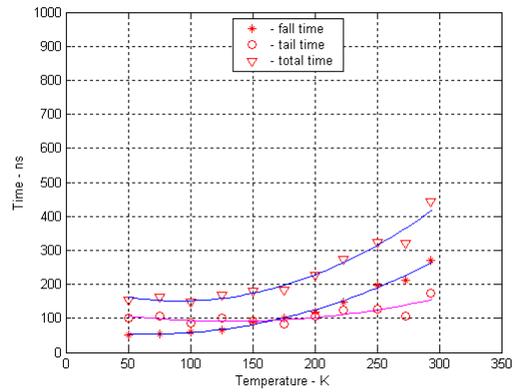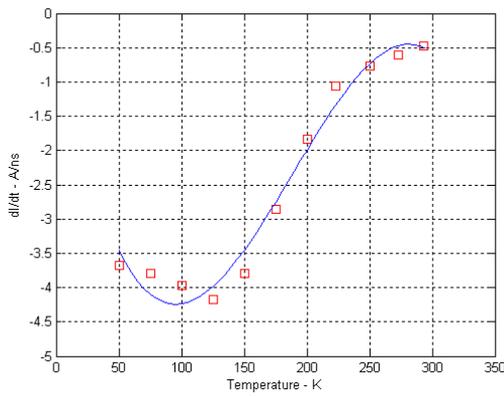
(a) 600 V PT device at 300 V and 100 A
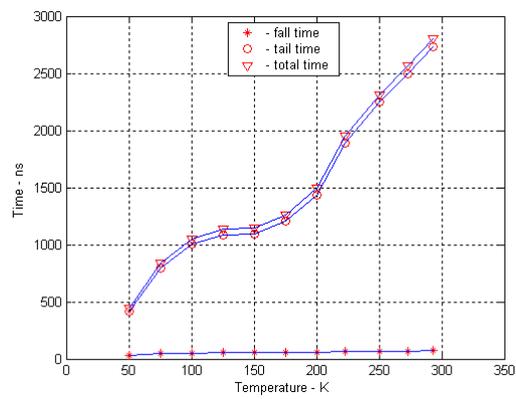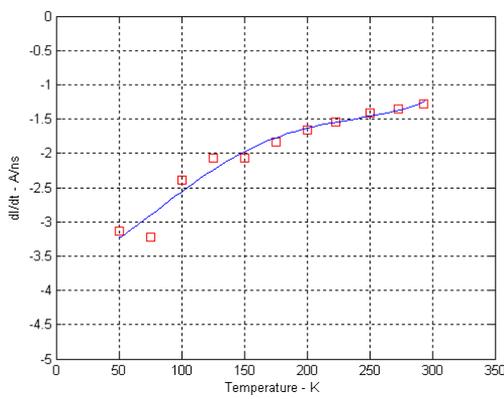
(b) 1700 V NPT device at 600V and 110 A
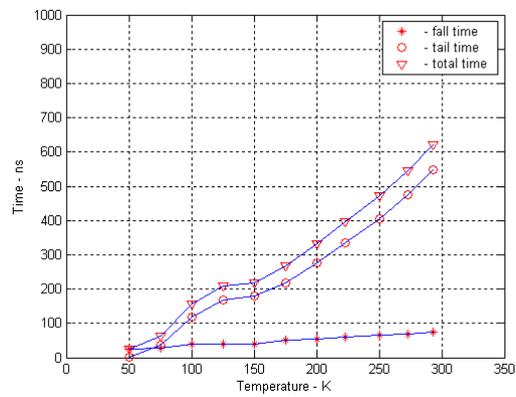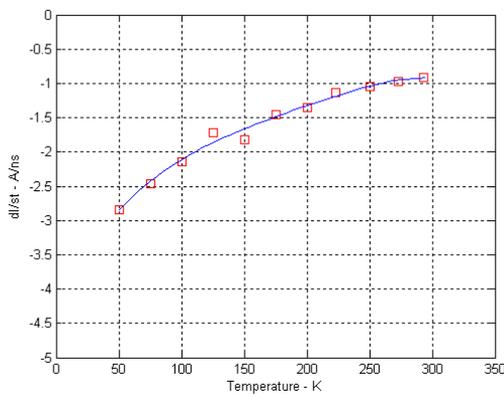
(c) 1700 V IGBT3 device at 600Vand 110 A
Figure 3-24 Turn-off di/dt (left) and turn-off times (right) from 50 K to 300 K
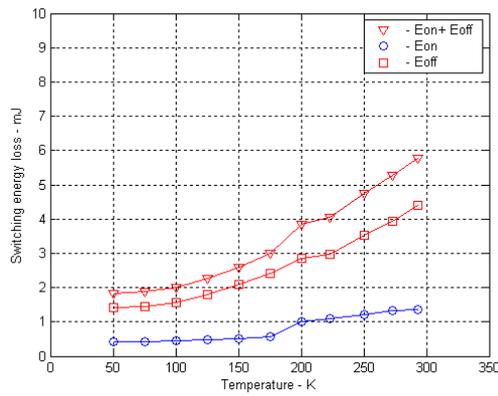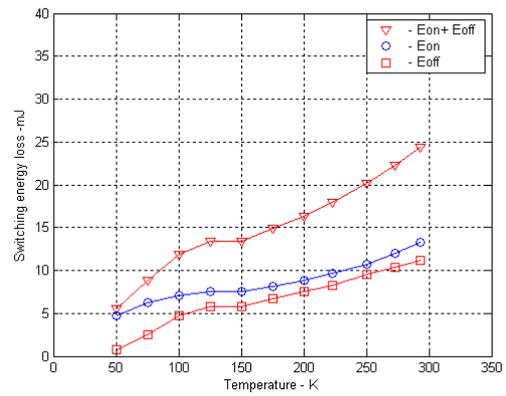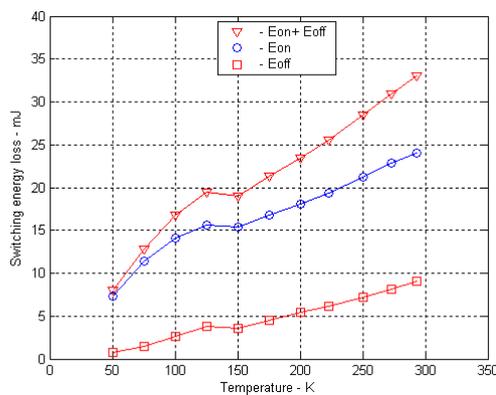
Figure 3-25 Switching energy losses from 50 K to 300 K
(a) PT device at 300 V and 100 A;
(b) NPT and (c) IGBT3 devices at 600Vand 110 A

3. 7 Diode characteristics

The most important diode features are the static characteristics, including on-state and breakdown, and the reverse recovery characteristics. The diode static characteristics were measured using a curve tracer: the high current mode for on-state tests and the high voltage mode for reverse breakdown tests. The reverse recovery characteristics were obtained from the double-pulse switching test. The diode in the 1700 V Dynex module was tested extensively. The other diodes were tested and similar results were obtained.

3. 7. 1 Diode static characteristics

Sketched typical diode on-state characteristics are shown in Figure 3-26. As discussed in section 2.2.2, four parameters are often used to express the diode static characteristics and are defined with respect to Figure 3-26:

Two parameters were obtained from the on-state test:

➢ V_{on}: turn-on voltage, corresponding to 1 A forward current.

➢ R_{on}: on-state incremental resistance. This value is the reciprocal of the curve gradient and may change at different current levels.

The other two parameters can be obtained from the reverse breakdown test:

➢ I_S: reverse leakage current.

➢ V_B: breakdown voltage.
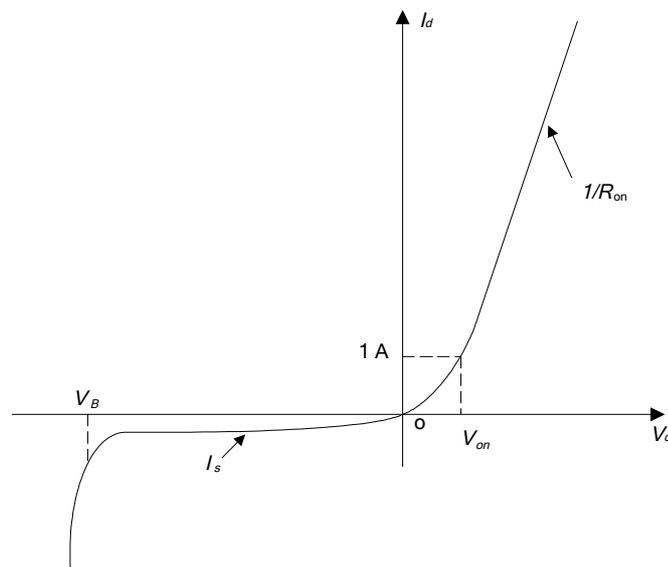
Figure 3-26 Diode static characteristics
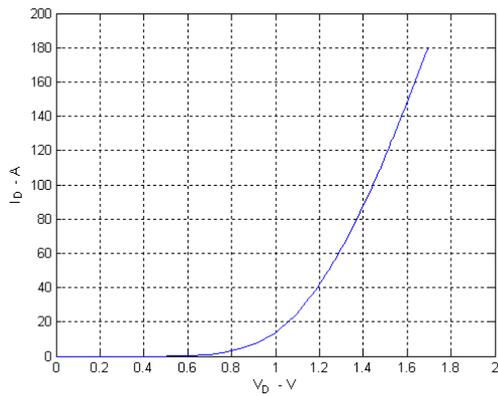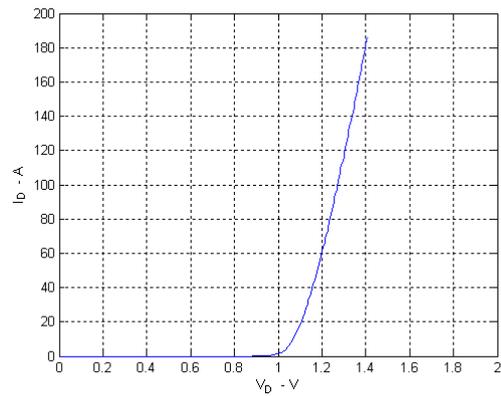
(a) 293 K   (b) 100 K

Figure 3-27 Sample diode on-state characteristics
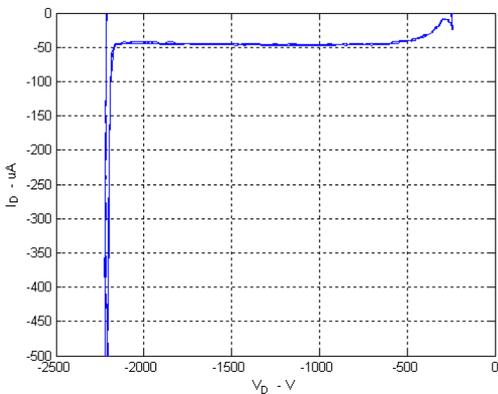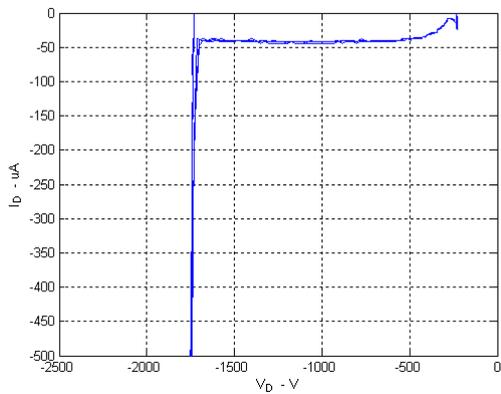
(a) 293 K   (b) 100 K

Figure 3-28 Sample diode reverse breakdown characteristics

Figure 3-27 and Figure 3-28 show the measured diode on-state and reverse breakdown characteristics at room temperature and 100 K. The measurements were carried out from room temperature down to 50 K in steps of 25 K.

Figure 3-29 shows the variation with temperature of the four parameters for the diode static characteristics, where the values of R_{on} are measured at a current level of 100 A, the values of I_s are measured at the rated voltage level , 1700 V, and the values of V_B are measured at a reverse current level of 100 μA.

The turn-on voltage increases approximately linearly as the temperature falls with a rate of approximately 1.6 mV/K. This increase may be attributed to an increased potential barrier height in the p-n junction due to a reduction in the intrinsic carrier concentration at low temperatures [3-12].

The on-state incremental resistance decreases sharply from room temperature down to 100 K. Below 100 K this resistance increases most probably due to carrier freeze-out. However, the results at very low temperatures should be treated with caution due to the small number of data points in this region.

The reverse leakage current does not change significantly with the temperature, but there is approximately a 20 % decrease of breakdown voltage at 50 K compared to that at room temperature. This is consistent with the reduction in forward blocking voltage observed in the PT and NPT IGBT devices.
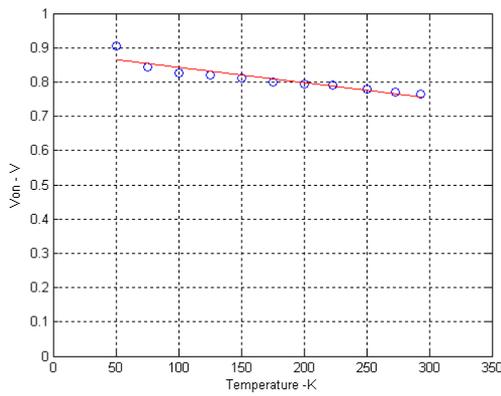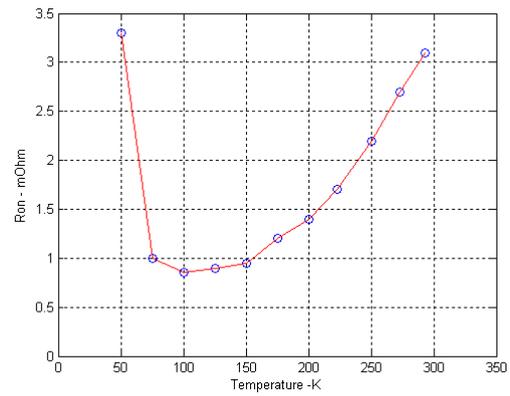
(a) V_{on} (b) R_{on}
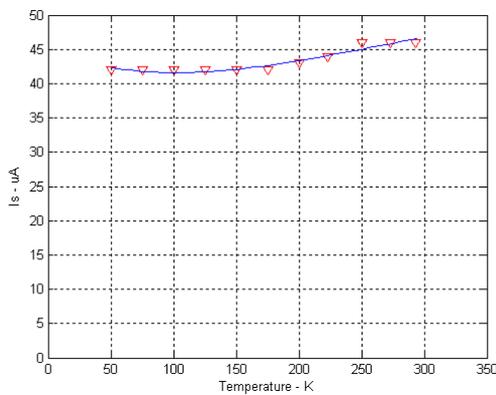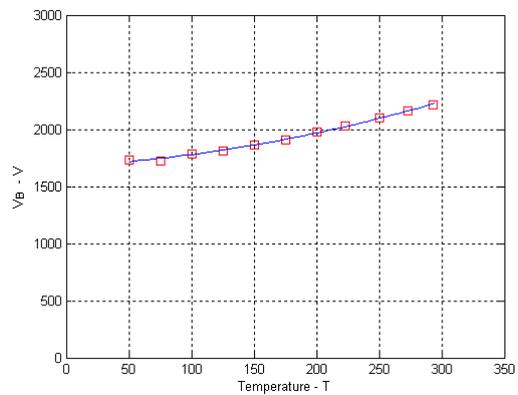
(c) I_S (d) V_B

Figure 3-29 Diode static parameter variations at low temperatures

3. 7. 2 Diode reverse recovery characteristics

The reverse recovery characteristics of the diode were obtained from the IGBT turn-on current waveforms since the tested diode was encapsulated in the module and could not be measured directly. The transforming process is shown in Figure 3-30.

The main parameters employed to describe the reverse recovery transient are:

➤ I_{FO}: forward current before turn-off;

➤ di_r/dt: the current gradient during turn-off;

➤ $-I_{rrm}$: peak reverse recovery current;

> t_{rr}: reverse recovery time, from the moment the current passes zero to the point where the current decays back to 10% of -I_{rrm}.

> Q_{rr}: turn-off recovered charge, approximately equal to $I_{rrm}t_{rr}/2$.
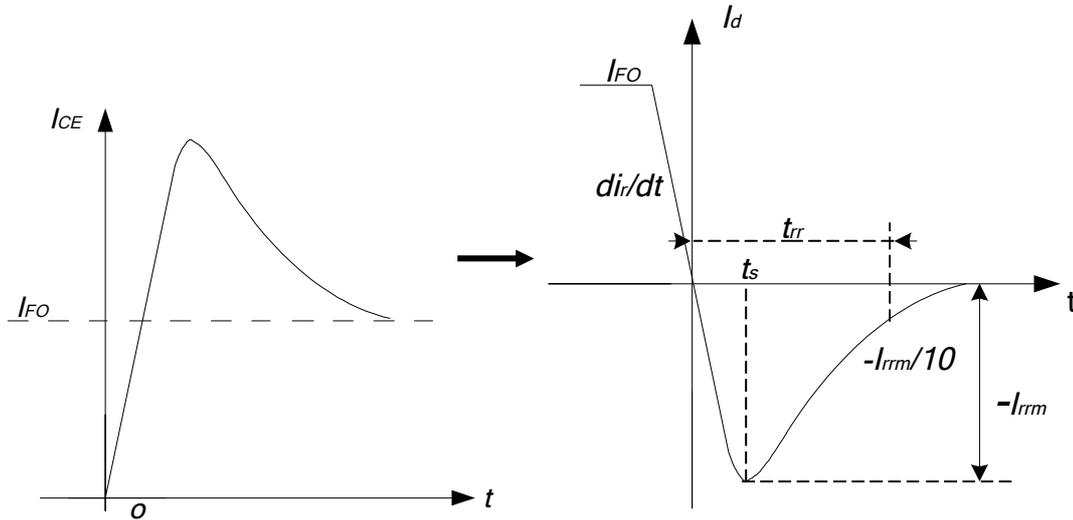
Figure 3-30 Diode reverse recovery transient
Left: IGBT current at turn-on;
Right: diode current;

Figure 3-31 shows the measured results at room temperature and 100 K for the reverse recovery transient. The current I_{FO} is approximately 100 A for the tested diode. Such tests have been carried out from room temperature down to 50 K in steps of 25 K.
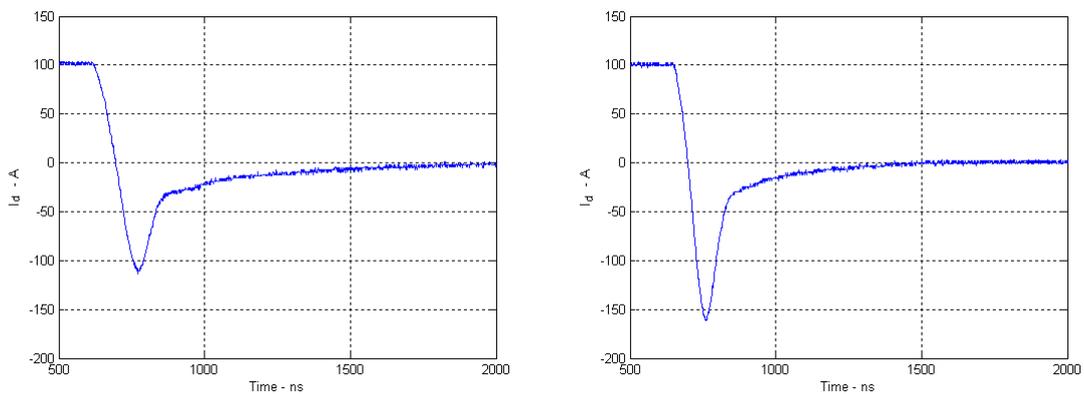
(a) 293 K   (b) 100 K
Figure 3-31 Diode reverse recovery currents at room temperature and 100 K

Figure 3-32 shows the variation of the diode reverse recovery parameters against temperature. The *di/dt* variation shows that the current slope becomes steeper at low temperature, from 1.8 A/ns at room temperature to approximately 3.5 A/ns at 50 K. This change is attributed to the faster switching speed of the NPT IGBT at low temperatures.

The peak reverse recovery current increases at reduced temperatures but remains approximately constant in the temperature range from 150 K down to 75 K. However, there is a sudden drop of I_{rrm} at 50 K. The reverse recovery time decreases at reduced temperatures, however it also remains approximately constant from 150 K down to 75 K and reduces very sharply below 75 K. The snappiness factor shows a similar variation against temperature to that of the reverse recovery time. The rapid change in characteristics as the temperature reduces below approximately 75 K has not been studied in detail in this work, however these results suggest that a more thorough study is warranted.
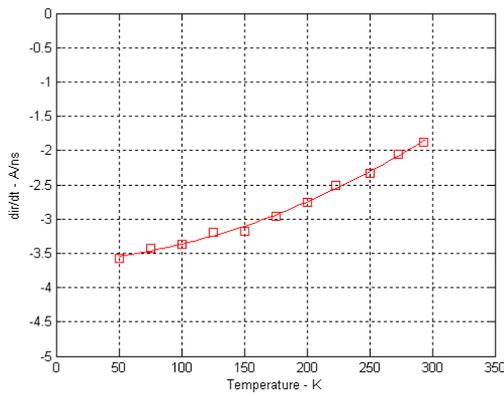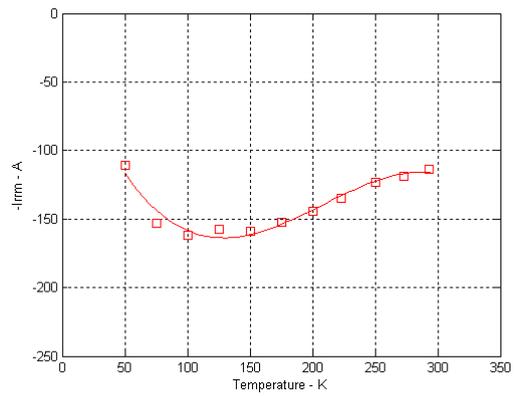
(a) di_r/dt (b) $-I_{rrm}$
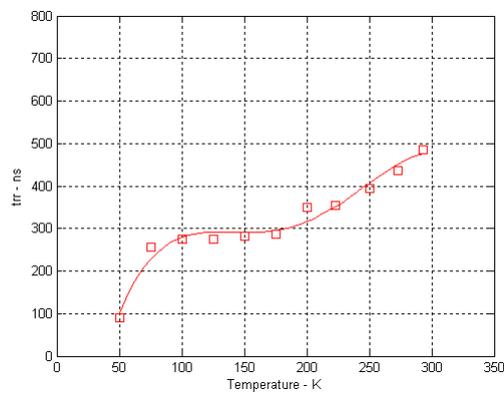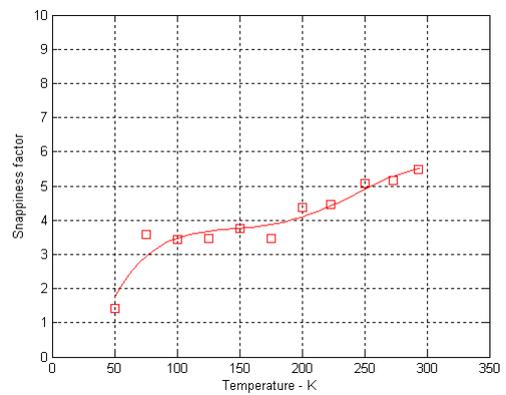
(c) t_{rr} (d) snappiness

Figure 3-32 Diode reverse recovery parameter variations at low temperatures

3. 8 Analysis of experimental results

The cryogenic characteristics of the tested IGBTs and diodes have been described in the pervious sections. The cryogenic environment provides improved characteristics such as lower on-state voltage drops and faster switching speeds. The relevant cryogenic properties will be discussed in this section.

3. 8. 1 IGBT cryogenic characteristics

As describe in section 3.4, all the tested IGBTs show lower on-state voltage drops at low temperatures. The IGBT on-state voltage is divided into two parts, the knee voltage and the

remaining voltage, corresponding to the voltages across the series-connected rectifier and MOSFET components in the simple model.

The knee voltages show different trends due to structural differences between the three devices. The PT and IGBT3 devices show increased knee voltages at low temperatures, but the NPT device's knee voltage varies very little. In the first term of equation (2-19), there are three elements dependent on temperature, n_i, L_a and D_a. At low temperatures, the reduced intrinsic carrier concentration, n_i, results in higher voltage drops, as indicated in (2-19). L_a, the diffusion length depends on the lifetime (τ_a) and ambipolar diffusion coefficient (D_a), which have opposite trends at low temperatures. These two effects tend to counteract each other, so the variation of L_a may have a minor effect according to (2-4). The ambipolar diffusion coefficient D_a increases at low temperature due to the increased mobility, which contributes to a lower knee voltage. Since the NPT IGBT has a wider low-doped drift region and no field-stop layer, the effect caused by the increased mobility tends to offset the effect caused by the reduced intrinsic carrier concentration. Therefore, the knee voltage of the NPT IGBT does not show much variation over the temperature range 50-300 K.

As shown in Figure 3-5, the on-state voltage decreases at low temperatures since the variation of the MOSFET component of voltage drop, is larger than the variation of the voltage across the rectifier component. In equation (2-19), the reduction of the second term due with the increased mobility at low temperatures dominates the variation of the total voltage drop across the IGBT device.

Due to the reduced minority carrier lifetime, τ_a, all the three IGBTs show much shorter tail times at low temperatures. This can be well explained by (2-25)~ (2-27).

3. 8. 2 Diode cryogenic characteristics

Several effects combine to determine the diode cryogenic on-state voltage drops. At low temperatures, the voltage drops across the end regions, V_{P+} and V_{N+} in equation (2-6), increase at low temperatures due to the reduced intrinsic carrier concentration. According to (2-2)~(2-4), the increased carrier mobility at low temperature is expected to result in a reduced voltage drop across the i-region. The reduced carrier lifetime offsets some effect of the increased mobility at low temperatures. The net result is normally that at low current densities V_F increases at low temperatures, whereas at high current densities it decreases. As shown in section 3.7.1, this is represented by an increase in the knee voltage and a decrease of the resistance R_{on}. Similar results have been published in [3-12].

The power diode shows much shorter reverse recovery time due to reduced carrier lifetimes at low temperatures.

3. 9 Summary

Three types of IGBT module have been tested in the temperature range from 50 K to room temperature. The low temperature effects on the IGBTs and the diodes in the tested modules have been studied. It is observed that cryogenic temperatures offer IGBTs significant improvements in both on-state and switching performance compared with those at room temperature.

The on-state voltage drops of these three devices reach a minimum at around 100 K. The reductions in on-state voltage drop at low temperatures are around 30 % for the 1700 V NPT IGBT, and 20% for the other two devices.

The reduction of the turn-off time occurs mainly in the temperature range from room temperature down to 150 K. In this range, the turn-off times of all the three devices reduce by a factor of approximately three. With shorter tails, the devices have dramatically lower switching losses at reduced temperatures. The IGBT3 device shows lower turn-off losses than the NPT device and this advantage increases as the temperature is reduced.

It should be noted that both turn-off times and turn-off losses for the two 1700 V IGBTs show sharp drops from 75 K down to 50 K. Further study is needed to examine the device performance in the region of 50 K.

The forward breakdown voltage of the IGBT3 device decreases dramatically at very low temperatures to around 40% of the room temperature value at 50 K, whereas a more modest reduction of 30% is seen for the NPT device.

For the diode, the static and reverse recovery characteristics are studied. At reduced temperatures, the power diode shows lower on-state voltage drops at high current levels whereas its on-state voltage increases at low current levels. Moreover, its reverse recovery processes are shorter, making it attractive for cryogenic applications.

Statement of original contributions

A cryogenic experimental investigation of three generations of IGBT: PT, NPT and IGBT3, over the temperature range 50- 300 K. Procedures to undertaken cryogenic tests and measurements, which cannot be found from textbooks. Based on the cryogenic system, static, gate charge and switching tests have been carried out. From the experimental work, the significantly improved performance of power IGBTs was quantified at low temperatures.

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4. 1 Introduction

To allow computer simulation techniques to be used to examine the performance of cryogenic power converters, accurate device models must first be developed and validated.

This chapter describes the Saber modelling of the tested IGBTs and diodes. A physically based compact device model from the University of Wales, Swansea is selected to model the cryogenic performance of the three tested IGBTs. A generic Saber power diode model with reverse recovery is selected to model the diode performance at low temperatures.

The experimental work described in Chapter 3 is used to parameterise the models for the tested IGBTs and the diode inside the 1700 V NPT Dynex module.

4. 2 IGBT model

The IGBT model selected in this chapter is a physically based level-1 model running in Saber from the Power Electronics Design Centre at the University of Wales, Swansea. This model has been used by the team at Swansea for the prediction of the transient current and voltage characteristics, as well as the device junction temperature in the temperature range of 300 –375 K, and showed excellent correspondence with physical behaviour [4-1,2].

4. 2. 1 IGBT parameters and equations

Similar to the equivalent circuit model of the power MOSFET given in [4-3], the equivalent circuit of the IGBT model is shown in Figure 4-1. This model has a simple structure comprising a voltage controlled current source along with parasitic resistances and capacitances, however its strength derives from the fact that the values of the elements in the equivalent circuit are calculated from expressions that are based on the physical structure and operation of the device.
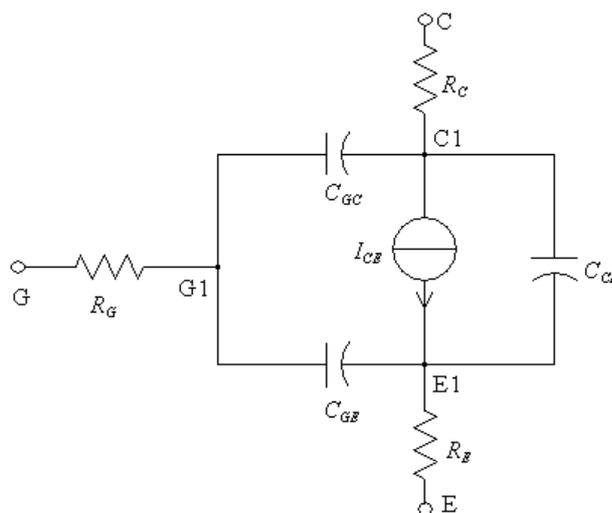
Figure 4-1 IGBT model

A total of 19 parameters are required in the various expressions for the values of the equivalent circuit elements. These parameters are classified into two categories, DC and AC. At a specific temperature, the DC parameters are constant, but the AC parameters may change at different current and voltage levels. The theory and equations relating to these parameters will be summarized in the remainder of this section.

The DC parameters are:

- K_{plin} - Transconductance in linear region ($V^{-2}A$)

- K_{psat} - Transconductance in saturation region ($V^{-2}A$)

- θ - Transverse field factor (V^{-1})

- V_T - Threshold voltage (V)

- λ - Channel length modulation parameter (V^{-1})

- N_d - Base doping (cm^{-3})

- BV_n - Breakdown voltage index

- V_B - Breakdown voltage (V)

- R_C - Collector resistance (Ω)

- R_G - Gate resistance (Ω)

- R_E - Emitter resistance (Ω)

The AC parameters are:

- A - Total active area (cm^2)

- A_{GC} - Gate collector overlap area (cm^2)

- V_{TC} - Gate collector overlap area threshold voltage (V)

- C_{GE} - Total gate emitter oxide capacitance (F)

- C_{GC} Total gate collector overlap oxide capacitance (F)

- n_{eff} Emitter efficiency (%)

- τ Minority carrier lifetime (ns)

- V_{OFF} Collector emitter offset voltage (V)

(a) The voltage controlled current source

According to Kirchhoff's Current Law, the current relationship in the IGBT equivalent circuit, shown in Figure 4-1, is expressed in the following differential equations:

$$\text{Node E1: } -I_{CE} - \frac{V_{EE1}}{R_E} - \frac{dQ_{CE}}{dt} - \frac{dQ_{GE}}{dt} = 0 \tag{4-1}$$

$$\text{Node G1: } -\frac{V_{GG1}}{R_G} - \frac{dQ_{GC}}{dt} + \frac{dQ_{GE}}{dt} = 0 \tag{4-2}$$

$$\text{Node C1: } I_{CE} - \frac{V_{CC1}}{R_C} + \frac{dQ_{GC}}{dt} + \frac{dQ_{CE}}{dt} = 0 \tag{4-3}$$

where '–' and '+' mean the current into and out of nodes respectively.

Q_{CE}, Q_{GC} and Q_{GE} are the charges on the capacitors C_{CE}, C_{GC} and C_{GE} respectively: $Q_{CE} = C_{CE}V_{CE}$, $Q_{GC} = C_{GC}V_{GC}$ and $Q_{GE} = C_{GE}V_{GE}$.

The current source I_{CE} is based upon the bipolar transistor/MOSFET model for the IGBT, in which the MOSFET provides the base drive current for the wide base PNP bipolar transistor. As described in section 2.3.4, the collector current consists of an electron current (I_e) flowing through the MOSFET channel and a hole current (I_h) flowing through the PNP transistor section:

$$I_{CE} = I_e + I_h \tag{4-4}$$

During transient conditions, the hole current decay rate is expressed as the following differential equation [4-6]

$$\frac{dI_h}{dt} = -\frac{I_h - n_{eff} I_e}{\tau} \tag{4-5}$$

where the emitter efficiency n_{eff} is the ratio between small changes in the hole current from the emitter and small changes in the total emitter current:

$$n_{eff} = \frac{\partial I_h}{\partial I_E} \tag{4-6}$$

n_{eff} is less than unity; and the extent to which it departs from unity represents the electron current that must be supplied from the drift region [4-10].

For an IGBT, τ is the hole lifetime in the N- base region. During a turn-off transient, the current will drop abruptly because the channel current component (I_e) is suddenly discontinued, that is $I_e = 0$. Tail current is obtained by solving (4-5):

$$i_{CE}(t) = I_{CE}(0) \exp\left(\frac{-t}{\tau}\right) \tag{4-7}$$

Considering the tail current expression given in (2-25), where $i_{CE}(t) = I_{CE}(0) \exp\left(\frac{-t}{\beta_{PNP} \tau_B}\right)$, the carrier lifetime τ is the product of the common-emitter current gain of the P base-N⁻ drift-P⁺ collector transistor (β_{PNP}) and the base transit time (τ_B).

Assuming that the electron current can be obtained from the working conditions, which will be explained in the following part of this section, there are five unknown variables in (4-1) ~ (4-5), namely V_{CC1}, Q_{GG1}, Q_{EE1}, I_{CE} and I_h. Using standard mathematic methods, these

equations can be solved, and then the current and voltage distribution in the IGBT equivalent circuit can be determined.

(b) Parasitic capacitances

Under transient conditions, the parasitic capacitors shown in Figure 4-1 play an important role. The miller capacitor C_{GE} has the most significant effect on the typical transients, that is, the switching processes of the device.

The gate capacitances C_{GE} and C_{GC} can be obtained from the gate charge test. However, it should be noted that the capacitance C_{GC} is highly non-linear and its value is related to the collector-gate depletion width and its actual value $C_{GC, ACT}$, may be expressed as [4-3]:

$$C_{GC,ACT} = \frac{C_{GC}}{1.0 + \dfrac{C_{GC}W_{GC}}{\varepsilon_0 \varepsilon_{Si} A_{GC}}} \tag{4-8}$$

where ε_0: the permittivity of free space, $= 8.85 \times 10^{-14}$ F/cm;

ε_{Si}: the relative permittivity of silicon, 11.90;

W_{GC}: the collector-gate depletion depth, cm. According to the p-n junction theory, the depletion depth can be calculated from the following two equations [4-5]:

$$W_{GC} = \sqrt{\frac{2\varepsilon_0 \varepsilon_{Si} V_1}{e N_d}} \tag{4-9}$$

and $\qquad V_1 = \dfrac{1}{2} \times \left(V_{GC} + V_{TC} + \sqrt{(V_{GC} + V_{TC})^2 + 1} \right) \tag{4-10}$

where e: electron charge, $= 1.60 \times 10^{-19}$ C.

$N_{d:}$ the doping concentration in the drift region, cm^{-3}.

The collector-emitter capacitance is obtained from

$$C_{CE} = \frac{\varepsilon_0 \varepsilon_{Si} A_{CE}}{W_{CE}}$$

(4-11)

where A_{CE} is the collector-emitter overlap area, $A_{CE} = A - A_{GC}$, cm^2;

W_{CE} is the collector-emitter depletion width, cm, which can be calculated from the following two equations [4-5]:

$$W_{CE} = \sqrt{\frac{2\varepsilon_0 \varepsilon_{Si} V_2}{e N_d}}$$

(4-12)

and

$$V_2 = \frac{1}{2} \times \left(V_{CE} + V_{bi} + \sqrt{(V_{CE} + V_{bi})^2 + 1} \right)$$

(4-13)

where V_{bi}: junction built-in potential, approximately 0.7 V.

(c) The electron current

The IGBT on-state characteristics are shown in Figure 4-2. In the range of $V_{OFF} < V_{CE} < V_B$, the electron current changes as follows:

- In the subthreshold region, $V_{GE} < V_T$, the electron current is zero.

- In the linear region, $V_{GE} > V_T$ and $V_{CE} - V_{OFF} < (V_{GE} - V_T) \times K_{psat} / K_{plin}$, the electron current has an approximately linear relationship with the collector voltage. This region corresponds to the area to the left of the dashed line in Figure 4-2.

- In the saturation region, $V_{GE} > V_T$ and $V_{CE} - V_{OFF} > (V_{GE} - V_T) \times K_{psat} / K_{plin}$, the electron current becomes saturated. This region corresponds to the operation area to the right of the dashed line in Figure 4-2.
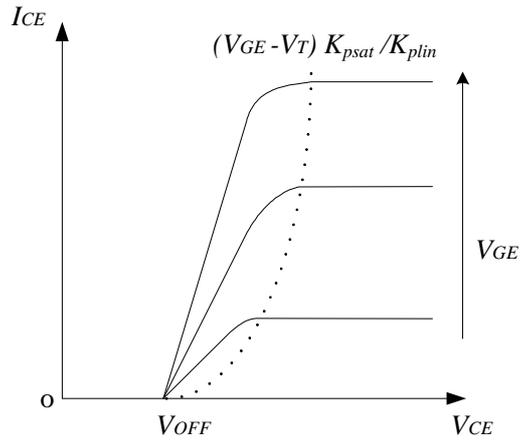
Figure 4-2 IGBT on-state characteristics

According to the simplified MOSFET theory [4-4], the electron current for the linear and saturation regions can be represented by $I_{e,lin}$ and $I_{e,sat}$ respectively:

$$I_{e,lin} = K_{plin} \times \left((V_{GE} - V_T)(V_{CE} - V_{OFF}) - \frac{1}{2}(V_{CE} - V_{OFF})^2 \right) \qquad (4\text{-}14)$$

$$I_{e,sat} = \frac{1}{2} K_{psat} \times (V_{GE} - V_T)^2 \qquad (4\text{-}15)$$

where $K_{plin} = \mu_{ns}(W/L_{CH})C_{OX}$ $\qquad (4\text{-}16)$

μ_{ns} is the surface electron mobility, cm^2/V-s;

W and L_{CH} are the channel width and length respectively, cm.

C_{OX} is the capacitance per unit area of the gate oxide, F cm^{-2}.

In the saturation region, the electric field becomes so large that it causes the electron drift velocity to saturate. The saturated electron current is related to carrier drift velocity as described by [4-4]:

$$I_{e,sat} = \frac{1}{2} C_{OX} W (V_{GE} - V_T) v_s \qquad (4\text{-}17)$$

where, v_s is electron saturation velocity, cm/s.

Incorporating (4-17) into (4-15) yields

$$K_{psat} = \frac{C_{OX} W v_s}{(V_{GS} - V_T)} \tag{4-18}$$

In addition, some other effects are considered in the IGBT model. First, in some types of devices, the output resistance significantly changes due to the expansion of the drain depletion region with drain voltage. This causes a small increase in I_{CE} with a collector voltage beyond pinch-off. This can be represented by introducing a channel-length modulation parameter, λ. Second, the device transconductance reduces with increasing gate bias. This is modelled by the use of parameter θ [4-3, 4].

The electron current in the linear region is therefore [4-3],

$$I_{e,lin} = K_{plin} \times \left((V_{GE} - V_T)(V_{CE} - V_{OFF}) - \frac{K_{plin}}{2K_{psat}} (V_{CE} - V_{OFF})^2 \right) \times \frac{M[1 + \lambda(V_{CE} - V_{OFF})]}{[1 + \theta(V_{GE} - V_T)]} \tag{4-19}$$

In the saturation region, the electron current is

$$I_{e,sat} = K_{psat} \times (V_{GE} - V_T)^2 \times \frac{M[1 + \lambda(V_{CE} - V_{OFF})]}{2[1 + \theta(V_{GE} - V_T)]} \tag{4-20}$$

M is the avalanche multiplication coefficient and is given by

$$M = \frac{1}{1 - \left| \frac{V_{CE}}{V_B} \right|^{BV_n}} \tag{4-21}$$

The electron current can be obtained directly if all the parameters are available. However, some parameters are not available, so a parameterisation methodology is necessary to determine unavailable parameters.

4. 2. 2 Parameterisation methodology

The parameterisation process is illustrated by the flow chart in Figure 4-3. Most parameters can be extracted from the experimental work, reasonable theoretical assumptions and approximations. However, several parameters, including K_{plin}, K_{psat}, R_C, τ and n_{eff}, cannot be determined directly due to the absence of necessary data. Here they are determined by iteratively fitting the experimental results.

The curve fitting process can be divided into three steps: (i) K_{psat} is tuned to fit the on-state characteristics in the saturation region; (ii) K_{plin} and R_C are tuned to fit the on-state characteristics in the linear region; and (iii) τ and n_{eff} are tuned to fit the tail current. Every step requires around 10 iterations to obtain satisfactory results. More detailed explanation is presented in the following sections.
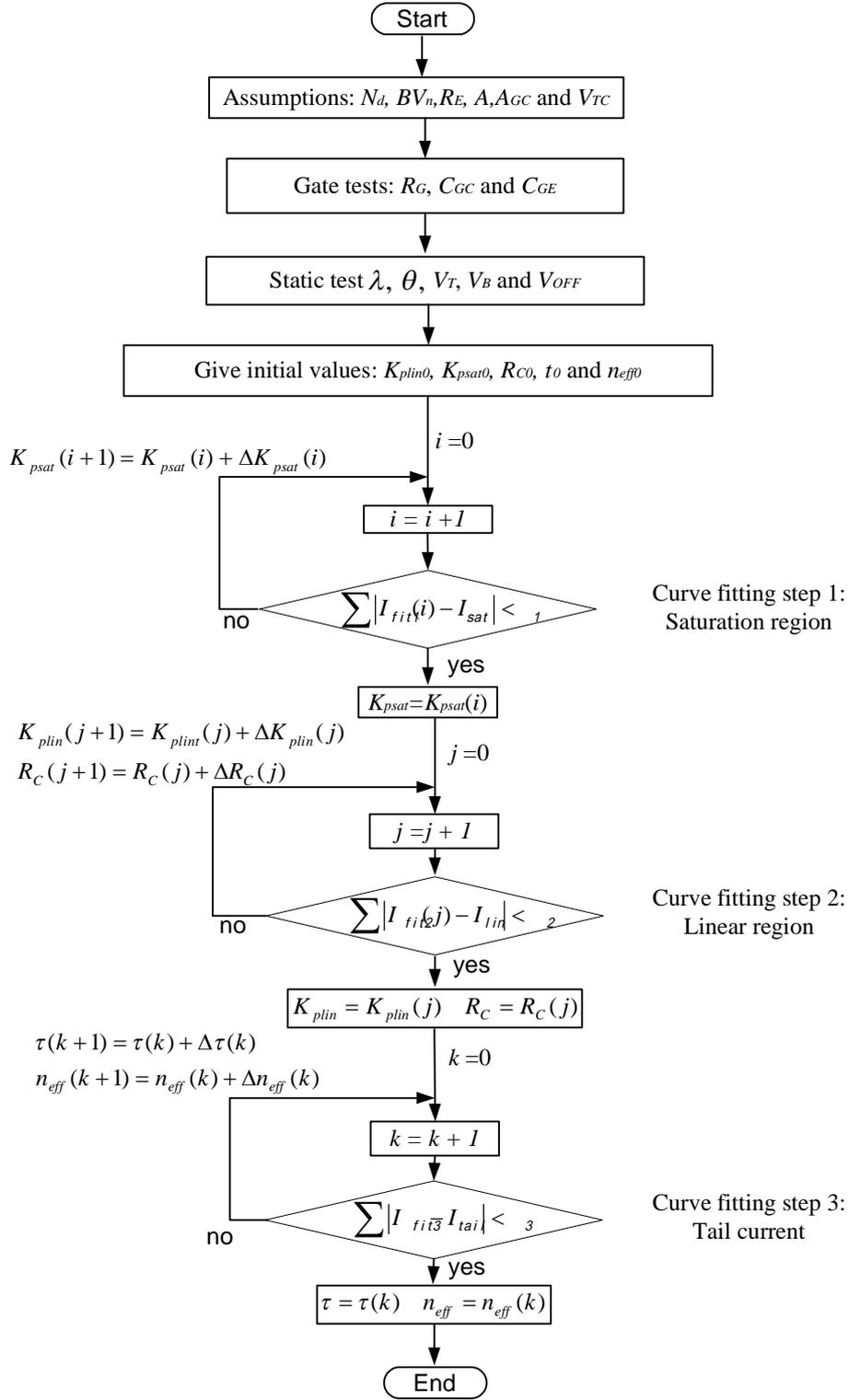
Figure 4-3 Flow chart for the model parameterisation process
I_{fit}: values from curve fitting;
I_{exp}: values from experimental work.

(a) Parameters from assumptions:

Considering the structural properties of the tested IGBTs, some assumptions were made to give values to 6 parameters, which are normally not very sensitive to temperature. These assumptions were reviewed in the later stages of the modelling work and considered to be acceptable.

- N_d. For high power IGBTs, the wafer doping concentration is at a level of 10^{14} cm^{-3} [4-7]. In this modelling work, $N_d = 1 \times 10^{14}$ cm^{-3} is assumed.

- BV_n. This constant is 4 for the case of an N$^+$P junction, or 6 for the case of a P$^+$N junction [4-5]. Considering that the junction between N drift and the P channel supports the forward blocking voltage, $BV_n = 4$ is used.

- R_E. Considering that the collector resistor plays a very important role in the DC characteristics and R_E is normally very small to avoid latch-ups, R_E was assumed to be 1 $\mu\Omega$ and all the resistance effect is attributed to R_C.

- A. Typical current densities for high power IGBT dies are in the region of 100 Acm^{-2} [4-8, 9]. Therefore the total active areas are assumed to be 3.50, 2.00 and 1.50 cm^2 respectively for the 350 A, 200 A and 150 A rated IGBTs.

- A_{GC}. The gate-collector overlap area was assumed as half of the total active area.

- V_{TC}. Like the junction built-in potential V_{bi}, V_{TC} is the voltage needed to build a depletion region between gate and collector. It is very small compared with the high voltages applied on the tested IGBTs. $V_{TC} = 0$ V was used in the modelling work.

(b) Parameters from gate charge tests

The gate resistance R_G, gate-emitter capacitance C_{GE} and gate-collector capacitance C_{GC} were obtained from the experimental work as described in section 3.5

(c) Parameters from static tests

The static tests were used to determine the following 8 parameters: K_{plin}, K_{psat}, λ, θ, V_T, Rc, V_B and V_{OFF}. In addition, the extraction of V_T, V_{OFF} and V_B was explained in Chapter 3. The extraction of the other parameters is described as follows.

From the sample results shown in Figure 4-4, it can be seen that the collector current does not increase significantly with V_{CE} in the saturation region, so it is reasonable to assume the value of λ as zero.

The transverse field parameter θ depends on the doping level and the surface conditions. The value normally used for a typical power IGBT is around 0.02 V^{-1} [4-4]. $\theta = 0.02$ V^{-1} was used and proved to be acceptable for the whole temperature range.

The parameters K_{plin}, K_{psat} and R_C could be calculated from (4-4) and (4-6). However, the gate cell parameters such as L_{CH} and W were unavailable, therefore a curve fitting method was used to extract these three parameters as explained in Figure 4-3.

The experimental results of the on-state characteristics are marked with dots in Figure 4-4. The on-state characteristics at $V_{GE} = 9$ V is in the saturation region and is fitted to obtained the value of K_{psat}; the on-state characteristics at $V_{GE} = 11$, 13 and 15 V are in the linear region and are fitted to obtain the value of K_{plin} and R_C. The fitting results from the model are shown as solid lines in Figure 4-4. It can be seen that the model fits well with the experimental results except for low current levels below 30 A. A complete set of results of the on-state characteristics from room temperature down to 50 K is given in Appendix A5.1

The parameterisation process was repeated over the temperature range from 50 K to room temperature in steps of 25 K. A set of values for each parameter was obtained as a function of temperature.
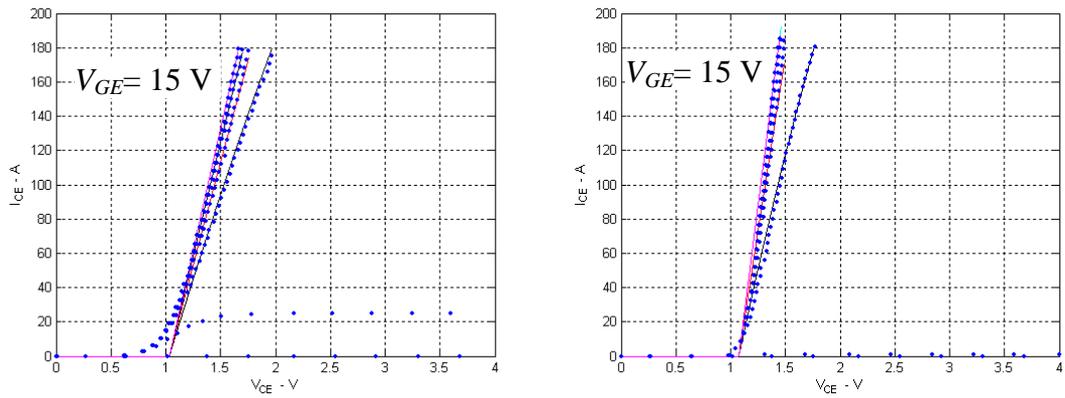
(a) 600 V PT IGBT, V_{GE}: 9, 11, 13, 15 V
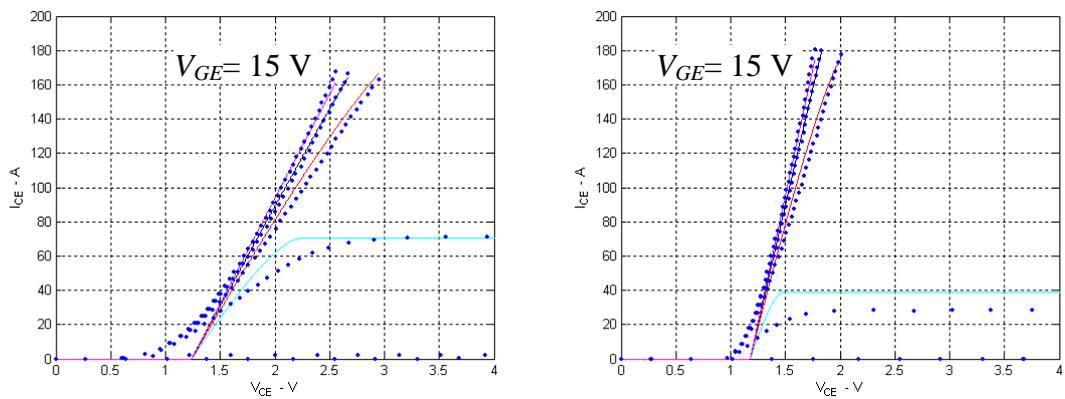
(b) 1700 V NPT IGBT, V_{GE}: 9, 11, 13, 15 V
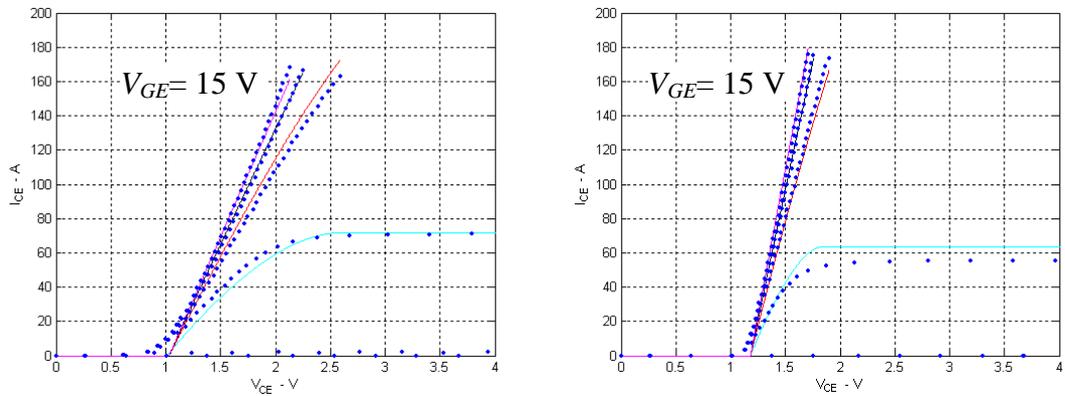
(c) 1700 V IGBT3, V_{GE}: 9, 11, 13, 15 V

Figure 4-4 On-state characteristics from the IGBT model
Dots: from measurements, solid lines: from modelling work.
Left: room temperature, right: 100 K.

(d) Parameters from switching tests

The two parameters n_{eff} and τ can be extracted from the collector current turn-off transients. The value of n_{eff} may be determined from the initial current drop in the turn-off current waveform. For example, if the current drops to one quarter of its on-state level, n_{eff} is around 0.25.

The value of τ may be determined from the length of the current tail. The longer the current tail, the longer the lifetime. For a particular device the parameters need to be adjusted iteratively for around 10 times until the convergence condition is obtained between the model and the experimental results. An automated optimisation technique could be helpful to obtain better fits.

To compare the switching results from the model with the experimental measurements, a Saber simulation was assembled on the basis of the simulation circuit shown in Figure 4-5, including the principal second order elements. The values of the second order elements were obtained by measurement or described in section 3.6.
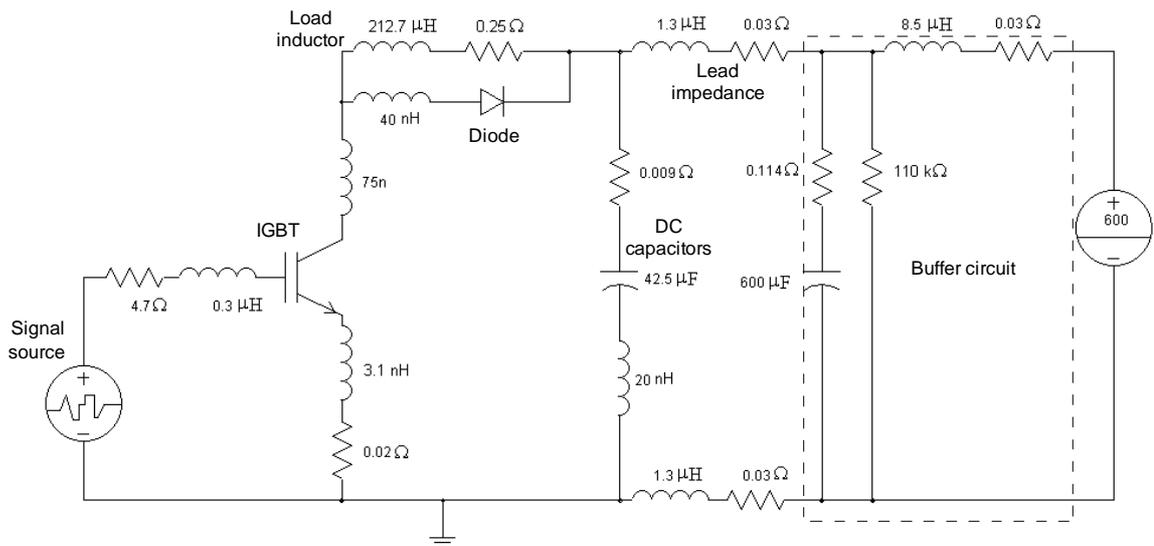
Figure 4-5 The circuit to simulate the IGBT turn-off transients
For 600 V device, V_{CC}=300 V; for 1700 V devices, V_{CC}= 600 V.

Sample turn off transient results are shown in Figure 4-6, 7 and 8 for the tested three devices. Waveforms are shown for the collector voltage and current at room temperature and 100 K at the turn off instant. The turn-off current results from the model fit very well with the experimental work though some voltage waveforms do not fit perfectly, which could be caused by the IGBT model, or by insufficient consideration of the parasitic components in the experimental circuit. A complete set of turn off transients from room temperature down to 50 K is given in Appendix A5.2.
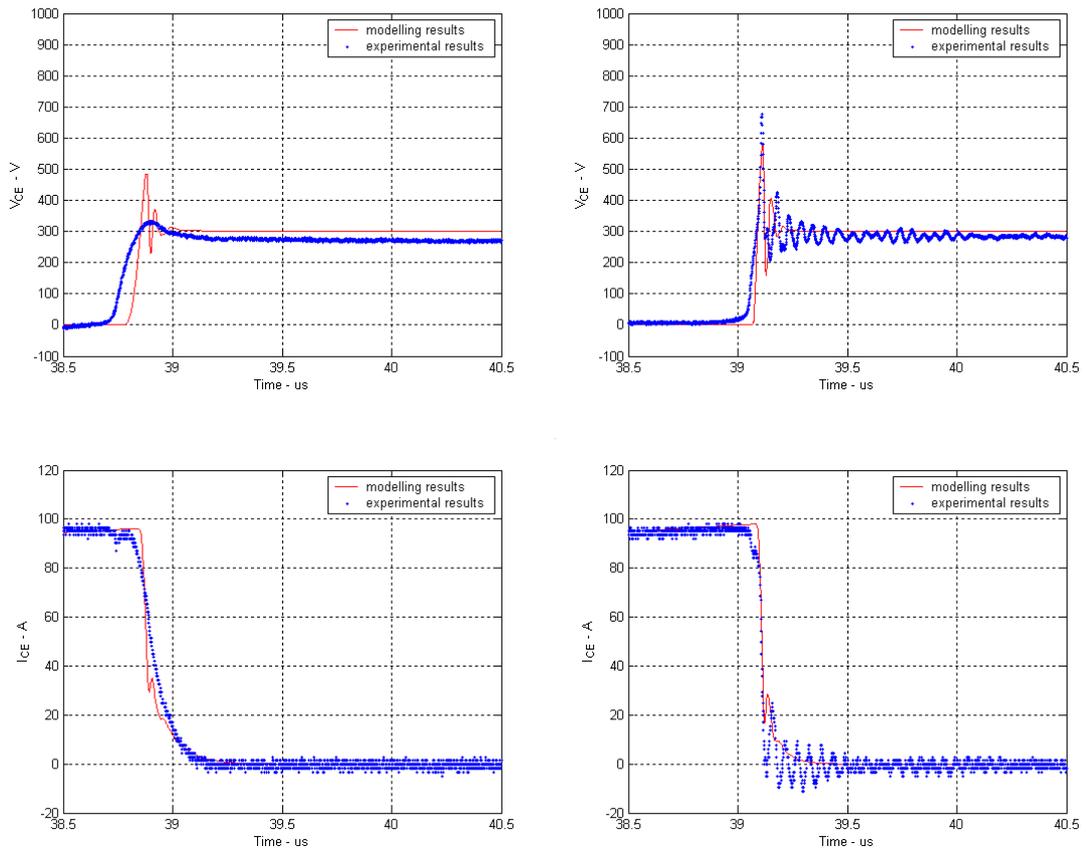
Figure 4-6 Turn-off transient of the 600 V PT IGBT
Left: 293 K; Right: 100 K
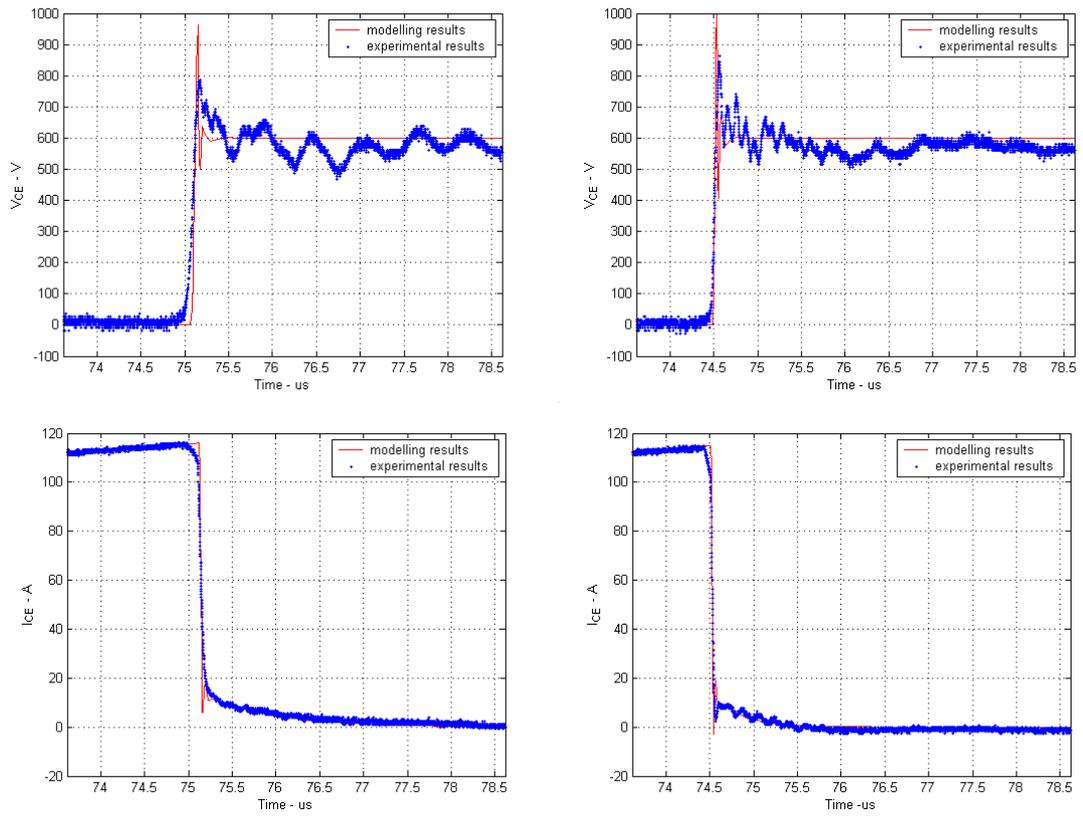
Figure 4-7 Turn-off transient of the 1700 V NPT IGBT
Left: 293 K; Right: 100 K
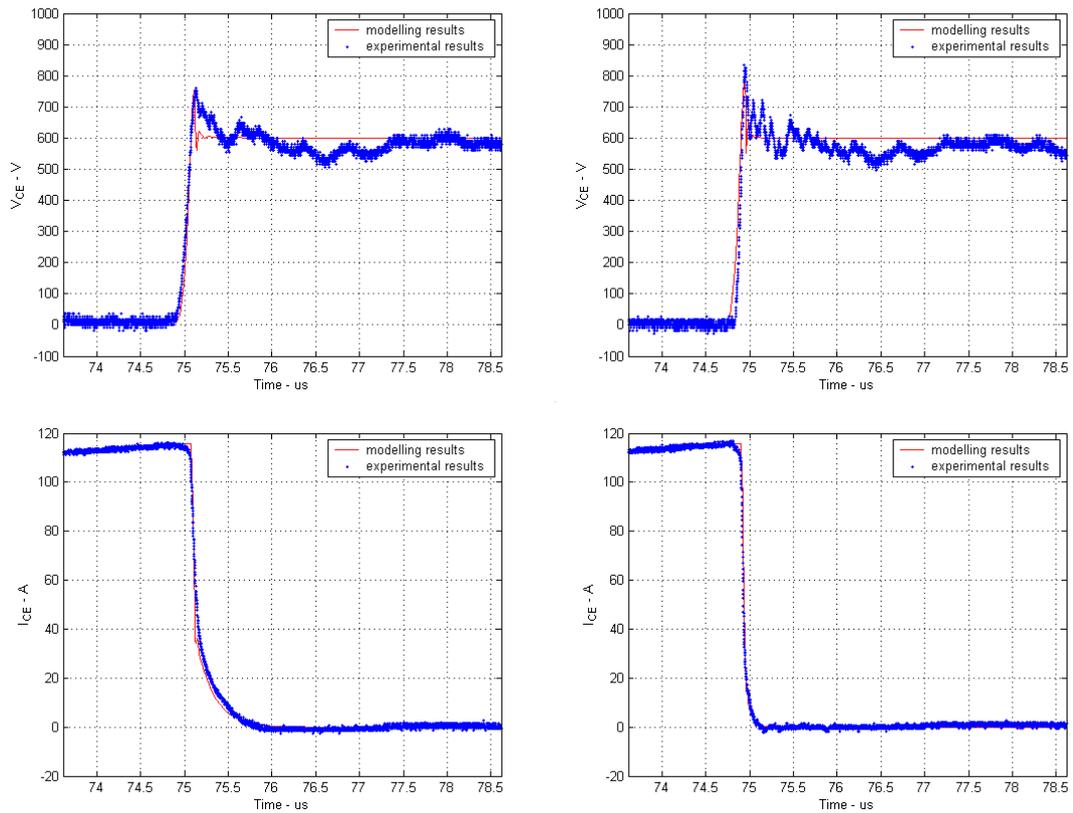
Figure 4-8 Turn-off transient of the 1700 V IGBT3
Left: 293 K; Right: 100 K

4. 2. 3 Parameter results

In the modelling process show that 9 parameters of the IGBT model are sensitive to temperature. The variation of the nine parameters against temperature is shown in Figure 4-9 for the three sample IGBTs. The variation in the measured values of V_T, V_B and R_G was described in Chapter 3, however, the results are repeated here to give a complete picture.

From equation 4-4 and 4-6, it can be seen that the parameters K_{plin} and K_{psat} are mainly determined by the MOSFET component in the IGBT structure.

The parameter K_{plin} increases with the reduction of the temperature mainly due to the increased mobility in the inversion layer of the channel. The K_{plin} of the two 1700 V device

increases linearly with the reduction of temperature, however, that of the 600 V PT device reaches a maximum at 150 K. This difference may be caused by the difference in the gate structures.

The parameter K_{psat} increases nonlinearly as the temperature is reduced. This is related to the variation of the saturation velocity. The electron saturation velocity in bulk silicon increases by 25% when temperature reduces from room temperature down to 50 K. The variation of electron saturation velocity may be different due to different silicon samples, which may be responsible for the difference of K_{psat} in three devices.

The parasitic collector resistor R_C has similar temperature characteristics as the silicon resistor. The two 1700 V devices have larger parasitic collector resistors than the 600 V PT device.

All the three devices show reduced emitter efficiencies from room temperature down to 50 K: 60% reduction for the IGBT3 device, twice the figure for the PT and NPT devices. The 600 V PT IGBT has a much larger emitter efficiency n_{eff} over the whole temperature range, which is consistent with the PT device characteristics as explained in section 2.3.2. The efficiency variation implies that the electron current plays a more important role at lower temperatures. From the electron and hole mobility temperature characteristics in bulk silicon given in [4-11], the mobility ratio μ_n/μ_p is shown in Figure 4-10. This ratio becomes higher at reduced temperatures, which means the electron current becomes dominant at low temperatures.

The three devices show shorter carrier lifetimes at low temperatures, especially the 1700 V NPT device, which is consistent with the shorter tails at lower temperatures seen in the experimental work. As explained in [4-12], the temperature characteristics of carrier lifetime is very dependent on the samples, which may cause the differences in the tail current in three devices.

The variations of V_{OFF} against temperature are different: V_{OFF} for the NPT device varies very little, whereas the values for the PT and IGBT3 devices increase by around 20% as the temperature falls from 300 K to 50 K. This discrepancy is similar to that in the voltage drops across the rectifier component in the IGBT devices, as described in 3.4.1. The increase in V_{OFF} at low temperatures may also be attributed to an increased potential barrier height in the buffer-emitter junction due to a reduction in the intrinsic carrier concentration [3-12].

From the results shown in Figure 4-9, it can be seen that there are many differences between PT, NPT and IGBT3 devices. Further research is required to understand the physical causes of these effects and to identify the optimum device designs for cryogenic operation.
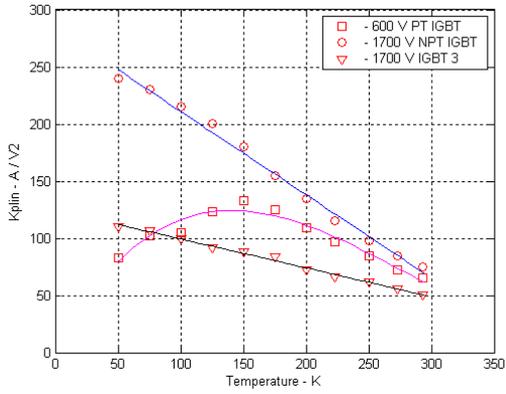
(a) K_{plin}
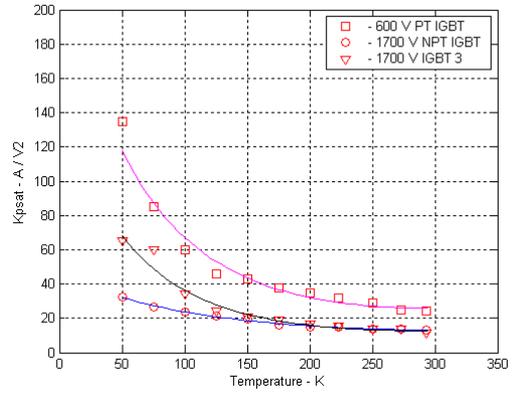
(b) K_{psat}

(c) V_T

(d) V_B

(e) R_C

(f) R_G

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(g) n_{eff}

(h) τ
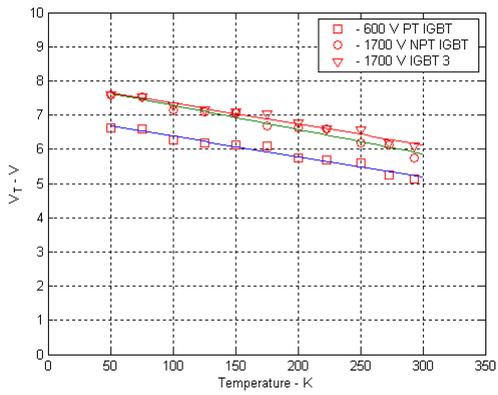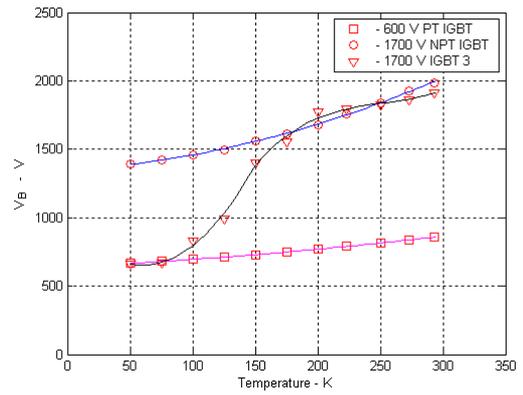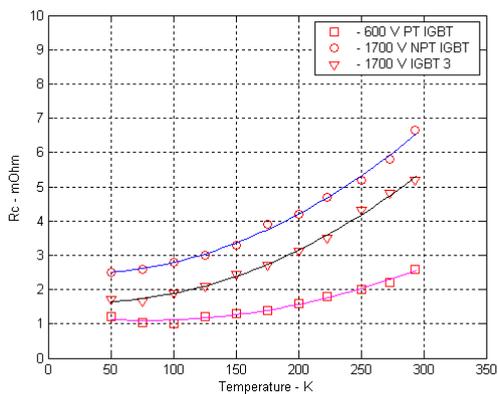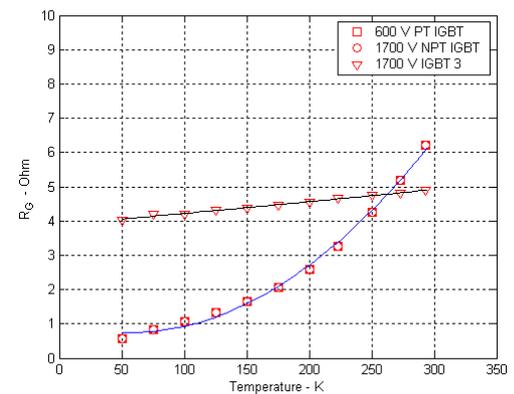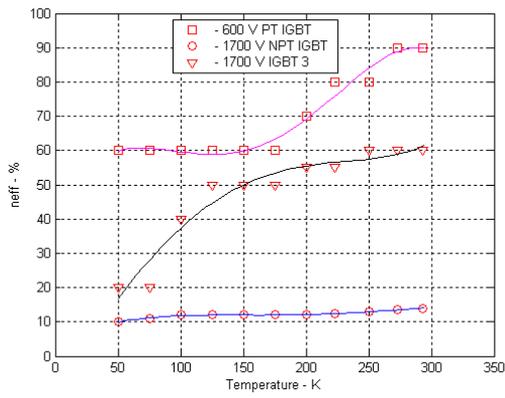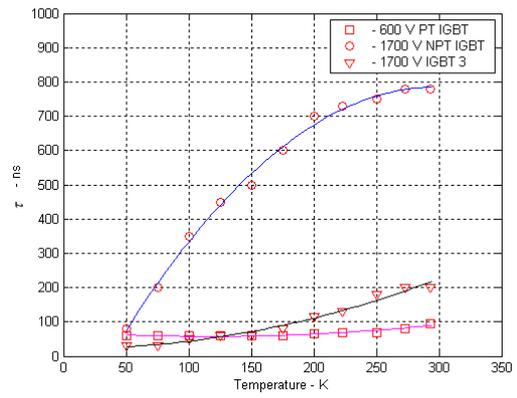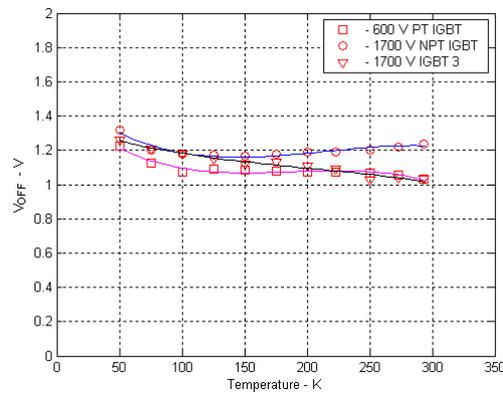
(i) V_{OFF}

Figure 4-9 Variation of model parameters with temperature for the three IGBTs
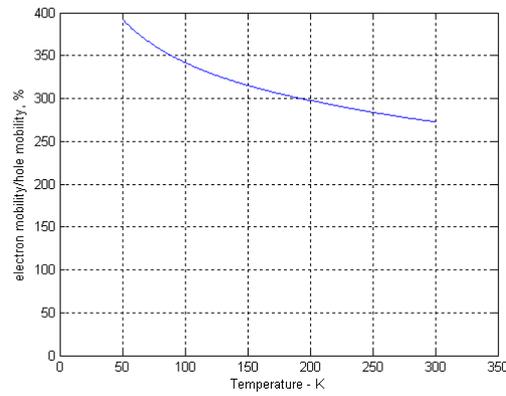
Figure 4-10 Mobility ratio μ_n/μ_p against temperature [4-11]

4. 2. 4 Power loss comparison between the model and experimental work

From Figure 4-4, it can be seen that the IGBT on-state voltages from the model and experimental work agree very well at the current level of 100 A over the temperature range 50-300 K. Therefore, it is expected that the on-state power losses from the IGBT model fit the experimental results.

From the description of the turn off process, the turn-off current and voltage results for the two 1700 V devices from the model fit very well with the experimental work as shown in Figure 4-7 and 8. The turn off energy losses for these two devices from the model are compared with their experimental counterparts in Figure 4-11 over the temperature range 50 to 300 K. These results further validate the IGBT device model.

(a) 1700 V NPT IGBT	(b) 1700 V IGBT 3
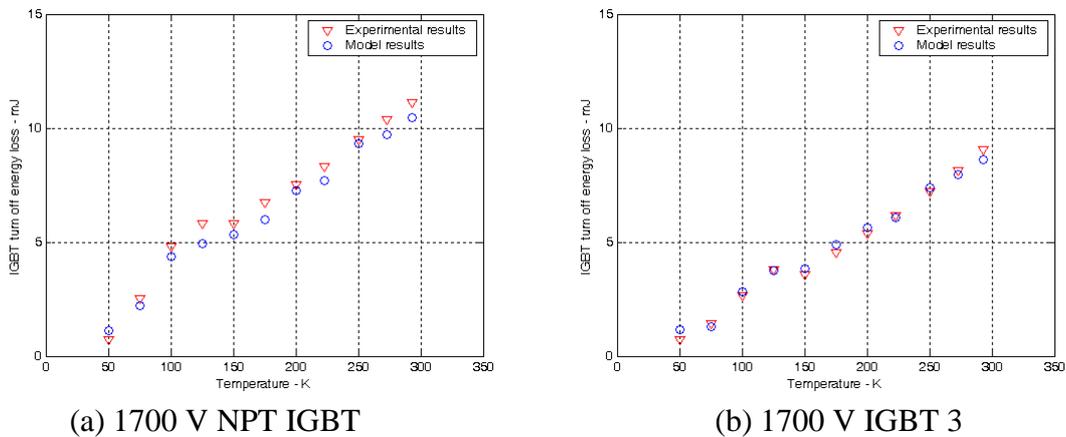
Figure 4-11 IGBT turn off energy loss comparisons

4. 3 Diode model

The selected diode model is also a level-1 model, called 'Power Diode Model with Reverse Recovery' and is a standard generic model in the Saber simulation package [4-13]. This model includes both the static and reverse recovery characteristics.

4. 3. 1 Diode parameters and equations

The parameters of the model can be classified into static, reverse recovery and junction capacitance parameters, and are listed below.

The static parameters are:

- V_{on} - Diode turn- on voltage, which corresponds to a current of 1 A through the diode (V).

- R_{on} - Diode on state resistance (Ω)

- I_S - Reverse leakage current (A)

The reverse recovery parameters are:

- I_{FO} - Diode forward current before turn off process (A);

- di_r/dt - Diode current slope at turn off (A/s);

- I_{rrm} - Peak value of diode reverse recovery current (A);

- t_{rr} - Diode reverse recovery time (s);

- Q_{rr} - Diode turn-off recovered charge (C);

The Junction capacitance parameter is:

- C_j - Diode junction capacitance corresponding to a junction voltage V_j (F)

The parameter values may be readily obtained from straightforward measurements of the diode behaviour.

(a) Diode static model

The diode static model is the basis to which all diode dynamic effects are added. As shown in Figure 4-12, it consists of a contact resistance R_{on} in series with an ideal diode that represents the junction voltage V_j by the exponential law:

$$I_d = I_S \left\{ \exp\left(\frac{V_j}{V_b}\right) - 1 \right\}$$
(4-21)

where $V_j = V_d - I_d R_{on}$.

Some models distinguish high-level injection, low-level recombination and emitter recombination effects by adding several ideal diodes in parallel [4-14, 15]. However, for power circuit simulation, one exponential law to describe the junction voltage gives sufficient accuracy [4-13].

Since the parameter V_{on} corresponds to a current level of 1 A, rearranging equation (4-21) gives the expression of the junction barrier potential:

$$V_b = \frac{V_{on} - R_{on}}{\ln\left(1 + \frac{1}{I_S}\right)}$$
(4-22)

From the parameters V_{on}, R_{on} and I_S, the diode static characteristics are defined.
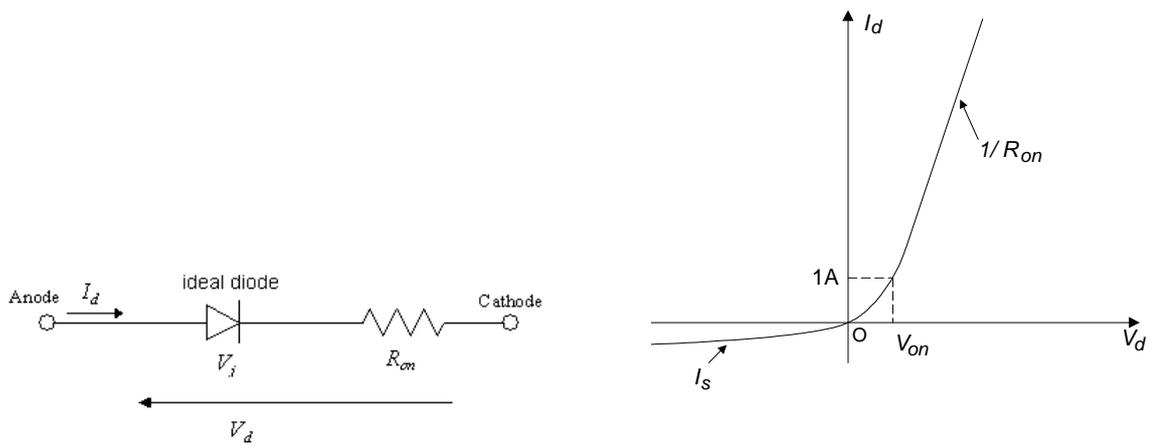
Figure 4-12 Diode static model and characteristics
Left: static model, right: static characteristics

(b) Diode reverse recovery model

Reverse recovery is the most important diode dynamic effect in power electronic circuits as it introduces overvoltage and high power dissipation during switching. Based on a macro-modelling approach, the reverse recovery submodel proposed by [4-14] consists of a resistance, an inductance and a voltage controlled current source, shown in Figure 4-13.
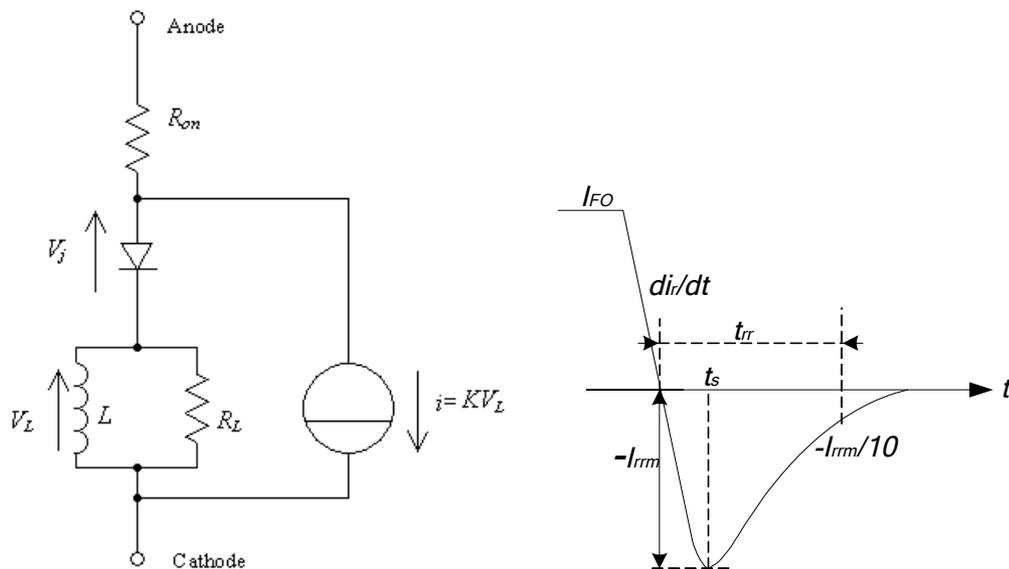
Figure 4-13 Diode reverse recovery model
Left: reverse recovery model, right: reverse recovery characteristics

Turned off with an inductive load, the circuit model provides the diode reverse recovery current waveform. For $t < t_s$, where t =0 is defined as the instant that I_d passes through zero, the ideal diode conducts and the external circuit determines the diode current. As I_d linearly decreases, the constant negative voltage across L commands a constant reverse current I_{rrm} through the controlled current source. At the moment $t = t_s$, I_d reaches $-I_{rrm}$ and the ideal diode gets blocked. After $t > t_s$, the ideal diode can be regarded as an open circuit. The subcircuit $R_L//L$ now acts independently of the external circuit and the current falls exponentially:

$$I_d(t) = -I_{rrm} \exp\left(-\frac{t - t_s}{L/R_L}\right)$$

(4-23)

Therefore the reverse recovery model only depends on two intrinsic parameters: R_L/L and K. Power diode data sheets provide I_{rrm}, t_{rr} and Q_{rr} for specified I_{FO}, di_r/dt and temperature conditions. t_{rr} is the time from the moment the current passes zero to the point where the current decays back to 10% of $-I_{rrm}$. Two intrinsic parameters R_L/L and K have been related to these external parameters in the datasheet [4-13]:

$$\frac{L}{R_L} = \frac{1}{\ln 10}\left\{t_{rr} - I_{rrm}\left(\frac{di_r}{dt}\right)^{-1}\right\}$$

(4-24)

$$K = \frac{I_{rrm}}{L}\left(\frac{di_r}{dt}\right)^{-1}\left\{1 - \exp\left(\frac{-I_{FO} - I_{rrm}}{L\frac{di_r}{dt}\left(K + \frac{1}{R_L}\right)}\right)\right\}^{-1}$$

(4-25)

The time constant R_L/L is given by (4-24), in which a degree of liberty exists between L and R_L, so the inductance of L is arbitrarily set equal to 10 pH. L being fixed, R_L can be directly deduced from (4-24) and K is obtained by solving (4-25).

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Once the turn-off conditions I_{FO} and di_r/dt are given, only two parameters out of I_{rrm}, t_{rr} and Q_{rr} are needed to define the turn-off current waveform. The diode template is implemented to handle any combination of two parameters. If all three are provided, only I_{rrm} and t_{rr} are used to calculate R_L and K.

(c) Junction capacitance

A second important dynamic effect in the diode is due to the space charge regions that develop on both sides of the junction. The corresponding capacitance depends on the width of the regions, which in turn depends on the applied voltage. An accurate description of the junction capacitance is given by [4-13, 14]:

$$C_j = \frac{C_0}{\left(1 - \dfrac{V_j}{V_b}\right)^m} \qquad \text{for } V_j < 0; \tag{4-26}$$

$$C_j = C_0\left(1 + m\frac{V_j}{V_b}\right) \qquad \text{for } V_j > 0. \tag{4-27}$$

where the gradient factor m depends on the doping profile and typically ranges from 0.3 to 0.5. C_0 is the junction capacitance for zero bias.

The junction capacitance is implemented as a voltage controlled current source, whose value can be defined as

$$I_c(V_j) = \frac{d}{dt}\int C_j dV_j \tag{4-28}$$

This current may play an important role in the reverse recovery process. Considering the current contribution from the junction capacitance, the complete diode model is shown in Figure 4-14.
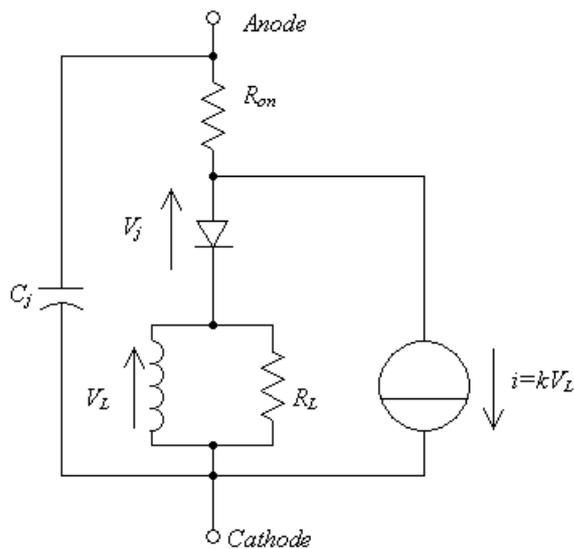
Figure 4-14 The complete diode model

Compared with the IGBT level–1 model, the diode model is simpler: the steady-state model just consists of one ideal diode and one resistor, and the dynamic model only has a parasitic non-linear capacitor and a voltage-controlled current source. This model remains valid over a wide range of current levels though it does not consider other characteristics.

4. 3. 2 Parameterisation methodology

On the basis of the experimental work described in Chapter 3, the diode model parameters can be determined.

(a) Static parameters

The diode parameters R_{on}, I_S and V_{on} were determined directly from the static characteristic tests, described in Chapter 3.

The modelling results at 293 K and 100 K are shown in Figure 4-15. It can be seen that the model agrees with the experimental work very closely for current levels above 20 A.
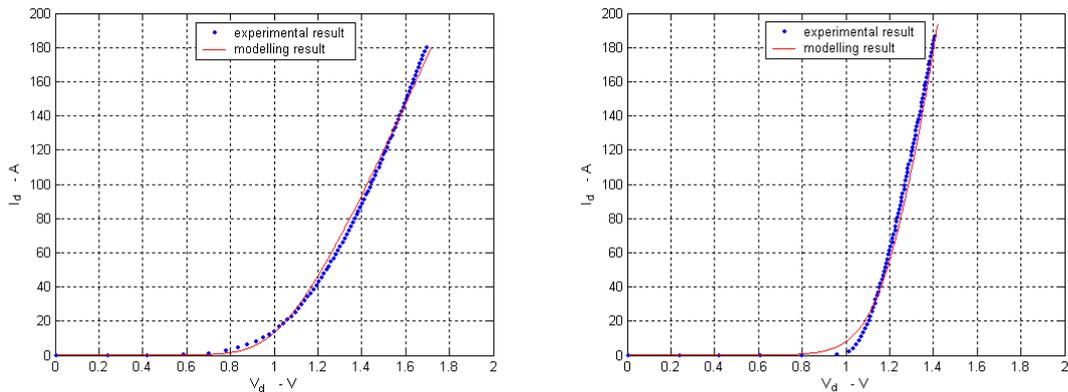
Figure 4-15 Diode static modelling results (Left: 293 K, right: 100K)

(b) Reverse recovery and junction capacitance parameters

The actual reverse recovery characteristics have waveforms like those shown in Figure 4-16. Different from the ideal reverse recovery waveform shown in Figure 4-13, the practical reverse recovery process after the moment t_s consists of two parts: a sharp recovery process (phase I) followed by a gradual recovery process (phase II). The phase I process may be modelled by the normal diode reverse recovery model described above, and the phase II process was modelled by appropriate choice of the parasitic junction capacitance.
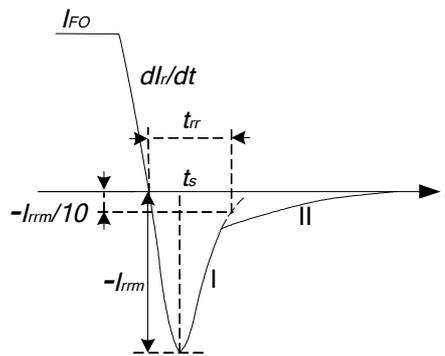
Figure 4-16 Practical power diode reverse recovery waveform

A circuit model of the switching test rig was assembled in Saber to simulate the diode reverse recovery characteristics as shown in Figure 4-5.

From the diode reverse recovery experimental results, the forward current value I_{FO}, the reverse peak current I_{rrm}, the current gradient di_r/dt and the reverse recovery time t_{rr} may be determined. It should be noted that the parameter t_{rr} is the time needed to reach - $I_{rrm}/10$ along the phase I loci as shown in Figure 4-16, not along the reverse current loci as used in Chapter 3, so their values are slightly different.

According to [4-13], C_j can be extracted from a standard C-V test. However, the studied diode was encapsulated inside the power module, so such a test could not be carried out. The junction capacitance values were found related with the phase II loci shown in Figure 4-16. The larger the junction capacitance, the longer the phase II. Therefore the capacitance values at different temperatures were determined by iteratively fitting the experimental results

Figure 4-17 shows the diode reverse recovery model results. Waveforms are shown for the IGBT voltage V_{CE} at the turn on instant and the corresponding diode current at room temperature and 100 K. The model results for the reverse recovery current fit the experimental results closely and the IGBT voltage V_{CE} also fits quite well.
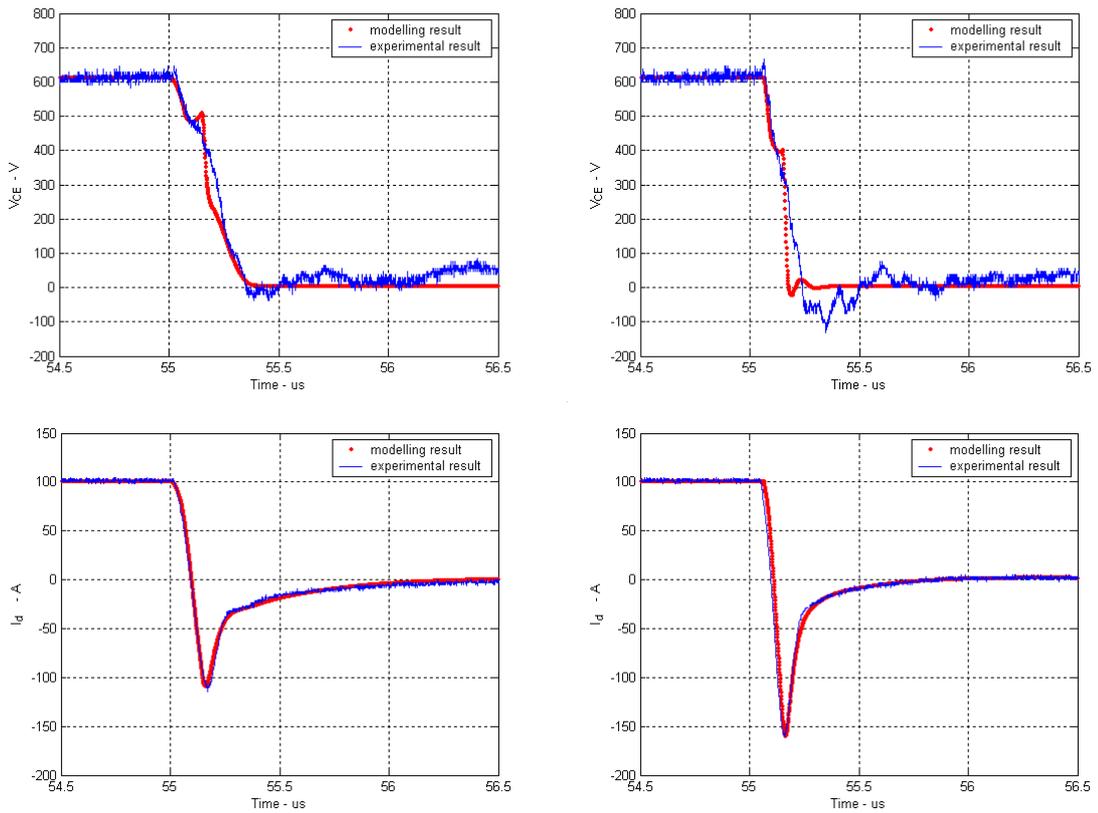
(a) 293 K   (b) 100 K

Figure 4-17 Diode reverse recovery model results

4. 3. 3 Parameter results

From the modelling work, all the parameters for the diode model were determined from 50 K to room temperature at intervals of 25 K, shown in Figure 4-18. Some parameters for the diode in the 1700 V Dynex module were already presented in Chapter 3. Two other parameters, t_{rr} and C_j are discussed as follows.

The recovery time t_{rr} gradually decreases by a half from room temperature down to 75 K. Its reduction at low temperatures will greatly decrease the diode switching energy loss.

The junction capacitance values were from curve fitting, not from measurements due to the unavailability of test samples. The values are around 30 nF the same order as the NPT

1700V IGBT input capacitance given in the datasheet, 15 nF. The junction capacitance gradually decreases by one-third from room temperature down to 75 K.

(a) V_{on}

(b) R_{on}

(c) I_S
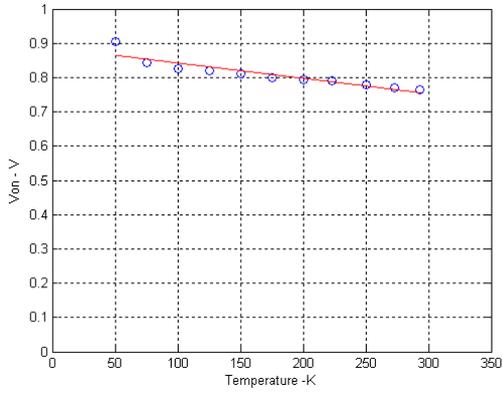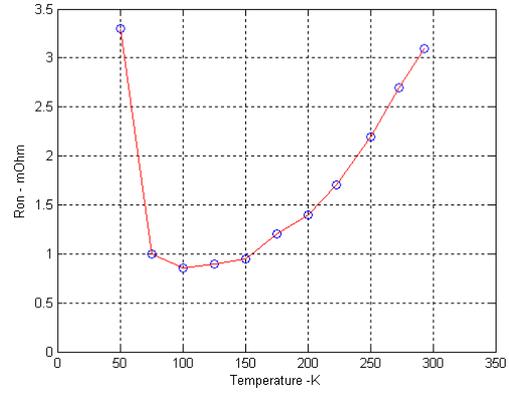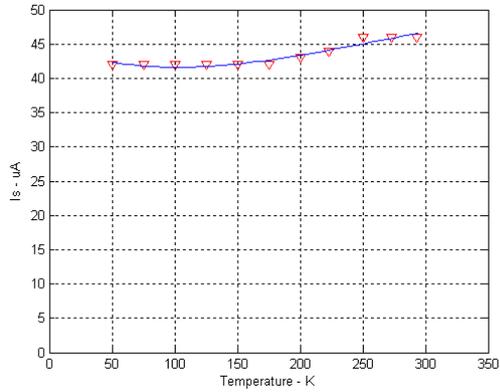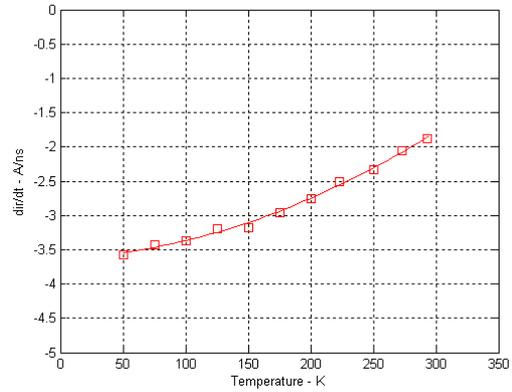
(d) di_r/dt
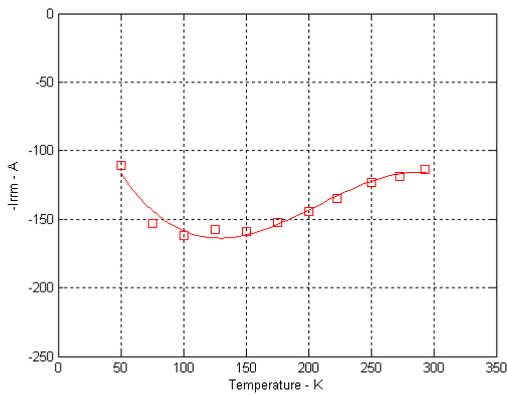
(e) $-I_{rrm}$
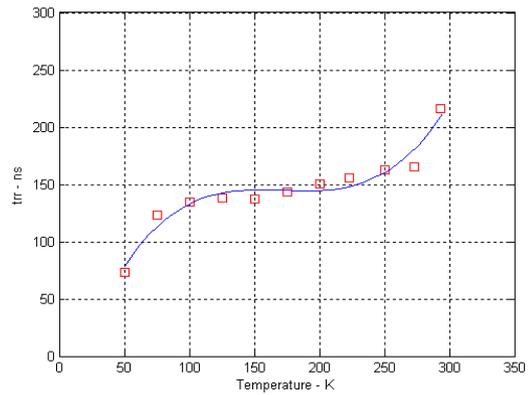
(f) t_{rr}
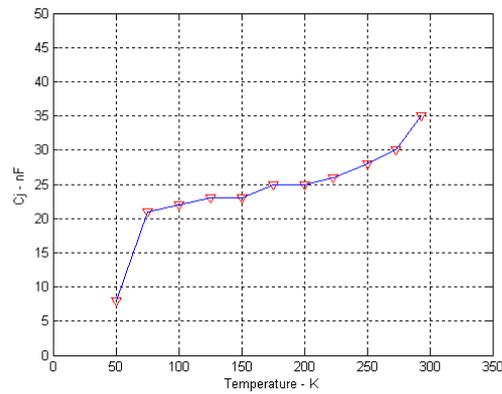
(g) C_j

Figure 4-18 Parameter variations against temperature for the diode
in the 1700 V Dynex module

It should be noted that the parameters showed a sharp reduction from 75 K to 50 K. Further

study is needed to examine the diode characteristics in the region of 50 K.

4. 3. 4 Power loss comparison between the model and experimental work

From Figure 4-15, it can be seen that the diode on-state voltages from the model and

experimental work agree very well at the current level of 100 A over the temperature range

50 to 300 K. Therefore, it is expected that the on-state power loss from the diode model will

fit the experimental results.

The reverse recovery energy losses from the diode model and experimental work fit well, as

shown in Figure 4-19. It can be seen that the energy loss does not change much from room

temperature down to 100 K since the increment of reverse recovery peak current offsets the

effect caused by the reduction of reverse recovery time in this temperature range. Below 100

K, the effect of the reducing reverse recovery time becomes dominant and the energy loss is

further reduced.

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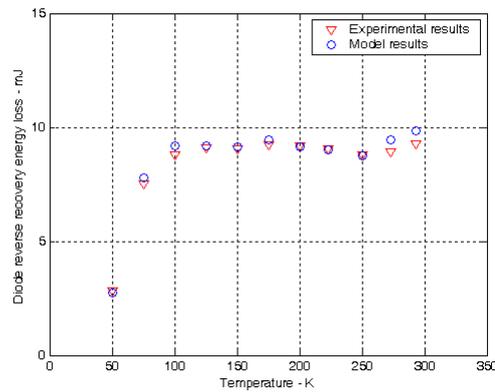
Figure 4-19 Diode reverse recovery energy loss comparisons

4. 4 Summary

This chapter described an IGBT and a diode model. The model parameters for the three tested IGBTs and the diode inside the 1700 V Dynex module were extracted on the basis of the cryogenic experimental work described in Chapter 3. The variation of model parameters was identified and discussed.

The results from the simulation work using the IGBT and diode model agree very well with the experimental results, confirming that they form a good basis for examining the behaviour of other power electronic circuit at low and cryogenic temperatures.

Statement of original contributions

The experimental results are used to parameterise a physically based, compact, level one IGBT model. Little research has been undertaken on the circuit level modelling of devices at low temperatures. The results demonstrated that these models can be used satisfactorily over the temperature range 50 to 300 K. The model parameter variations are showed in the thesis.

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Chapter 5 Evaluation of cryogenic converter performance by simulations

5. 1 Introduction

In this chapter, Saber simulation is used to examine the cryogenic performance of a DC-DC step-down (buck) converter and a pulse-width modulated inverter leg. The temperature-dependent models built for the NPT IGBT and the diode in the Dynex 1700V module, as described in Chapter 4, were used as power switches. The simulated temperature ranged from 50 K to room temperature, 293 K.

For the DC-DC buck converter, the total energy losses at two switching frequencies were studied by simulations. For each case several duty ratios were tried to study the variation of the switching and conduction losses at low temperatures. Two current levels, 100 A and 150 A were tried. For the inverter leg, two different modulation ratios were used to study the variation of the switching and conduction losses at low temperatures. For each case, several loads with different power factor were tried respectively and also different switching frequencies.

5. 2 DC-DC step-down (buck) converter simulations

Since it is one of the most widely used DC-DC converters, and furthermore forms the basis of numerous more complex topologies, the step-down converter was selected as the first candidate circuit for study by simulation at cryogenic temperatures.

5. 2. 1 Converter circuit

As the name implies, a step-down converter provides a lower average output voltage than the DC input voltage. Its main application is in regulated DC power supplies and DC-motor speed control [5-1].

A basic step-down DC-DC converter is shown in Figure 5-1, consisting of an ideal switch and a resistive load. The output voltage ripple is limited by using a low-pass filter, consisting of an inductor and a capacitor.

The average output voltage V_o may be obtained by calculating the average of the v_{oi} waveform, as shown in Figure 5-2a. In the continuous conduction mode V_o is

$$V_o = \frac{t_{on}}{T_s} V_{dc} = D V_{dc} \tag{5-1}$$

where D is the switch duty ratio. Therefore in the continuous-conduction mode, the average output voltage may be continuously controlled by controlling the duty ratio D of the switch in the range of 0 to 1. This is a form of PWM control.
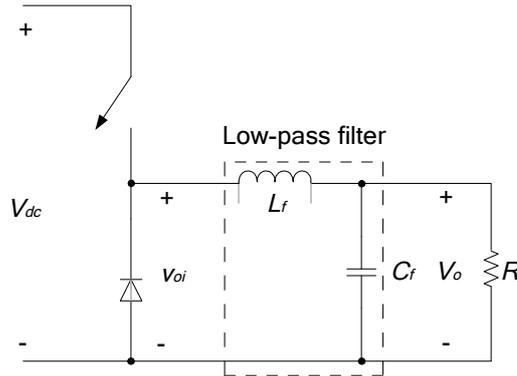
Figure 5-1 Basic circuit of a step-down DC-DC converter [5-1]

The ripple in the output voltage can be calculated by considering the waveforms shown in Figure 5-2 for the continuous-conduction mode of operation. Assuming all the ripple component in i_L flows through the capacitor and the average inductor current flows through the load resistor, the shaded area in Figure 5-2 represents an additional charge, ΔQ, on the capacitor. Therefore the peak-to-peak voltage ripple ΔV_o can be written as

$$\Delta V_o = \frac{\Delta Q}{C_f} = \frac{1}{C_f} \cdot \frac{1}{2} \cdot \frac{\Delta I_L}{2} \cdot \frac{T_s}{2} \tag{5-2}$$

The amplitude of the ripple current through the inductor ΔI_L is given by

$$\Delta I_L = \frac{V_o}{L_f}(1-D)T_s \tag{5-3}$$

Substituting (5-3) into (5-2) generates

$$\Delta V_o = \frac{T_s}{8C} \frac{V_o}{L_f}(1-D)T_s \tag{5-4}$$

Combing (5-1) and (5-4), the proportionate output voltage ripple is

$$\frac{\Delta V_o}{V_o} = \frac{1}{8}\frac{T_s^2(1-D)}{L_f C_f} = \frac{\pi^2}{2}(1-D)\left(\frac{f_c}{f_s}\right)^2 \tag{5-5}$$

where f_s is the switching frequency, the reciprocal of T_s.

f_c is the corner frequency of the low-pass filter, which can be expressed by

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$$f_c = \frac{1}{2\pi\sqrt{L_f C_f}}$$

(5-6)
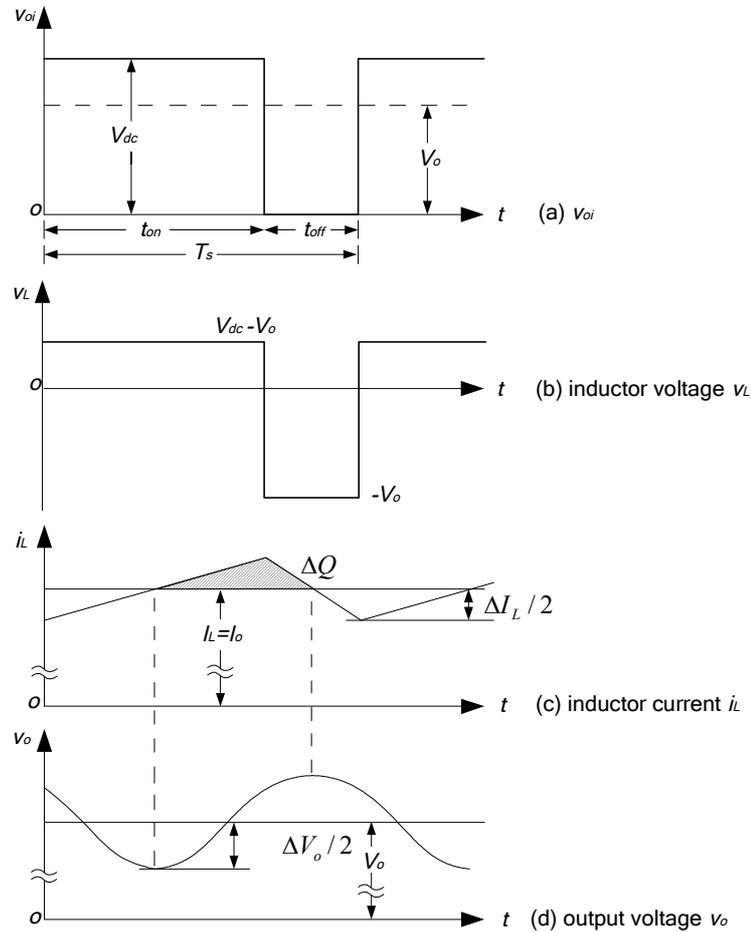
Figure 5-2 Voltage and current waveforms in a step-down converter [5-1]

In the simulation work, the ideal switch and diode shown in Figure 5-1 were formed by the temperature dependent models described in chapter 4, for the 1700 V NPT IGBT and the diode in the corresponding module. The temperature effects on the inductor and capacitor were not considered.

The conduction and switching losses for the IGBT and diode were considered in the temperature range of 50 K to room temperature. The power dissipation in the circuit would

be a crucial factor in a cryogenic application since the cryosystem would have to be sized to remove the losses.

The IGBT and diode models are based on the cryogenic tests at 600 V and 110 A, so the input DC voltage V_{dc} was selected as 600 V, and the output load current was selected in the range of 100 A to 150 A by selecting appropriate load resistors. The stray inductance in the circuit is not considered here. The gate drive signals of ±15V are generated from a simple rectangle waveform generator. A 4.7 Ω gate resistor is used for the IGBT operation.
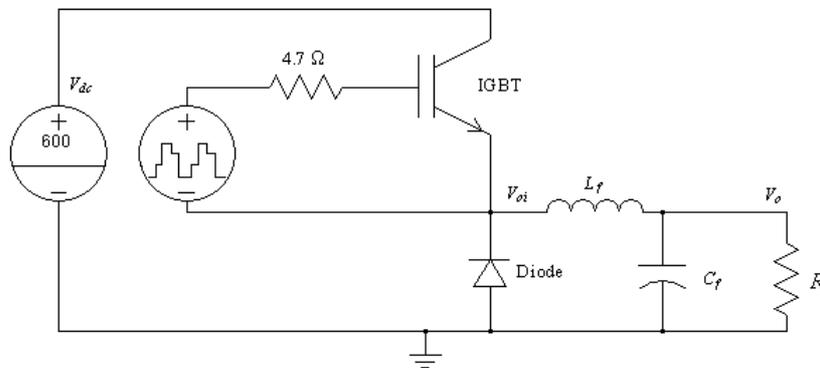
Figure 5-3 DC-DC step-down converter simulation circuit

(1) Load selection

To examine the effect of different frequencies on the cryogenic performance, two frequencies 10 kHz and 50 kHz were simulated, which are referred to as mode I and II here. The load current was set at 100 A and 150 A for each value of duty ratio and switching frequency. The converter was supposed to work in the continuous mode in the duty ratio range of 0.1 to 0.9, in which three duty ratios 0.3, 0.5 and 0.7 were simulated. The list of six simulations is shown in Table 5-1.

Mode I	f_s (k Hz)	V_{dc} (V)	D	V_o (V)	I_o (A)	R (Ω)
Case I-1	10	600	0.3	180	100 /150	1.8/1.2
Case I-2	10	600	0.5	300	100 /150	3.0/2.0
Case I-3	10	600	0.7	420	100 /150	4.2/2.8

(a) Mode I, 10 kHz

Mode II	f_s (k Hz)	V_{dc} (V)	D	V_o (V)	I_o (A)	R (Ω)
Case II-1	50	600	0.3	180	100/150	1.8/1.2
Case II-2	50	600	0.5	300	100/150	3.0/2.0
Case II-3	50	600	0.7	420	100/150	4.2/2.8

(b) Mode II, 50 kHz

Table 5-1 Parameters for the converter simulation

(2) L_f and C_f selection

From (5-6), the ripple component in the output voltage can be limited by appropriate selection of the f_c/f_s ratio. The percentage ripple in the output voltage is usually chosen to be less than, for instance 1% [5-1]. Taking the lower switching frequency and the smallest duty ratio, that is, f_s =10 kHz and D=0.3, then according to (5-6), the value for the corner frequency of the low pass filter is given by

$$ f_{c\max} = \sqrt{\frac{\Delta V_o / V_o}{(\pi^2 / 2)(1-D)}} \times f_s = \sqrt{\frac{0.01}{(\pi^2 / 2)(1-0.3)}} \times 10 \times 10^3 = 538 \text{ Hz} \qquad (5\text{-}7) $$

In this case, f_c is selected as 500 Hz.

The most demanding design requirement for L_f is to maintain a continuous inductor current when the output current decreases to its minimum value, that is, the output current at the boundary between the continuous and discontinuous mode

$$ I_{oB} \leq I_{o,\min} \qquad (5\text{-}8) $$

where $I_{oB} = \dfrac{T_s V_{dc}}{8L_f}$, as given in [5-1].

$I_{o,min}$ is the minimum output current, A.

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The minimum output current corresponds to the largest value of load resistance and the smallest value of duty ratio:

$$I_{o,\min} = \frac{V_{o,\min}}{R_{\max}} = \frac{D_{\min}V_{dc}}{R_{\max}} = \frac{0.1 \times 600}{4.2} = 14.3 \text{ A} \qquad (5\text{-}9)$$

where $V_{o,min}$ is the minimum voltage and R_{max} is the maximum load resistance.

Therefore the minimum value of L_f required to maintain a continuous inductor current is given by

$$L_{f,\min} = \frac{T_s V_{dc}}{8 I_{o,\min}} = \frac{0.1 \times 10^{-3} \times 600}{8 \times 14.3} = 524.5 \text{ }\mu\text{H} \qquad (5\text{-}10)$$

The inductor value was selected to be 550 µH. According to (5-6), a 184 µF capacitor was selected to give a 500 Hz corner frequency.

From (5-1) and (5-3), the current ripple in the inductor current is expressed by

$$\Delta I_L = \frac{V_o(1-D)T_s}{L_f} = \frac{D(1-D)V_{dc}T_s}{L_f} \qquad (5\text{-}11)$$

The current ripple reaches its maximum value at $D=0.5$ and $T_s=0.1$ ms (for the 10 kHz cases):

$$\Delta I_{L,\max} = \frac{0.5 \times (1-0.5) \times 600 \times 0.1 \times 10^{-3}}{550 \times 10^{-6}} = 27.3 \text{ A} \qquad (5\text{-}12)$$

The parameters for all the components in Figure 5-3 are parameterised, so the simulation work can be carried out now.

5. 2. 2 Simulation work

The power device dissipation in the steady-state operation of the described power converter was studied in the simulation work. The simulation work was carried out from start-up to 0.02 s with a time of 5 ns and the max truncation error of 50×10^{-6} using Saber.

The operation after 0.01 s was regarded as steady state as the average value of the inductor voltage is zero. Figure 5-4 shows 10- cycles of the voltage and current waveforms, 1 ms in the simulation work. These waveforms are from case I-2 with 150 A output current. The percentage ripple in the output voltage is around 0.63%. The transient overshoots in the IGBT and diode current waveforms are caused by the diode reverse recovery process.
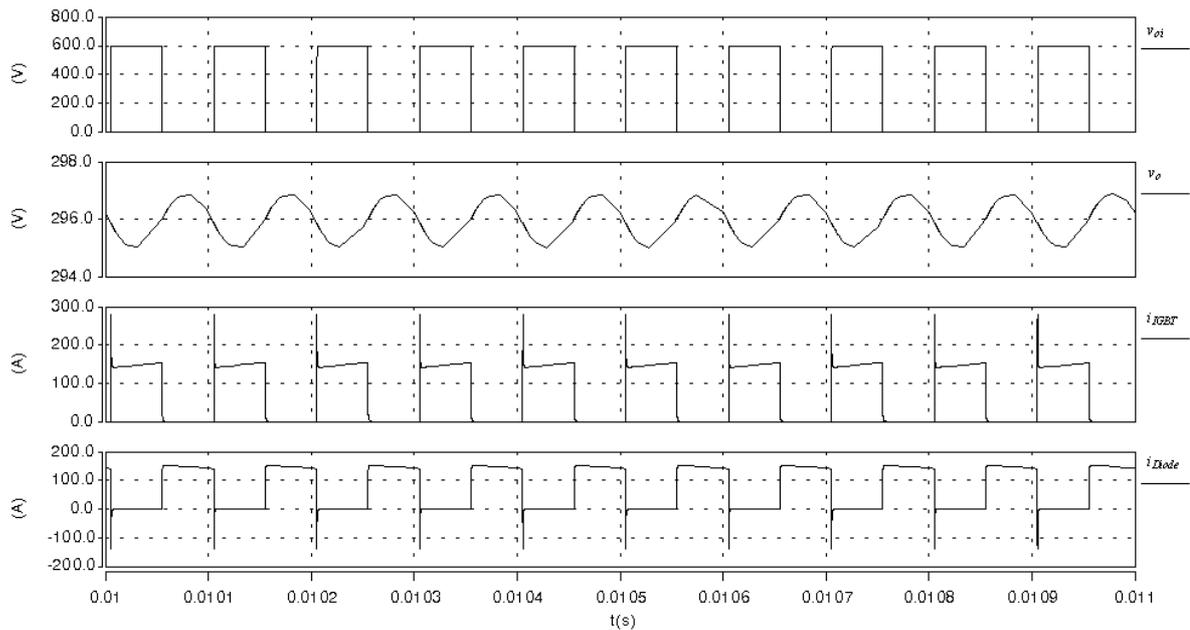
Figure 5-4 Converter current and voltage waveforms at 293 K from case I-2, 150A
from top to bottom: v_{oi}, v_o, i_{IGBT}, i_{diode}

The average steady-state power dissipation in the semiconductor devices was calculated from the energy dissipation in the time interval from 0.01 s to 0.02 s. This time interval is 100 cycles for the 10 kHz cases and 500 cycles for the 50 kHz cases. The energy loss was

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obtained by integrating the product of the device voltage and current with respect to time, and the average power dissipation was obtained by dividing the total energy by the time interval. Figure 5-5 shows the average power losses from the IGBT and the diode for the 10 kHz cases. Figure 5-6 shows the average power losses for the 50 kHz cases.

The total power loss, including the IGBT loss and the diode loss, decreases by a factor of around 2 and 3 from room temperature down to 50 K for the 10 kHz and 50 kHz cases respectively. The efficiency variation against temperature is shown in Figure 5-7. For the 10 kHz cases, the efficiency is slightly improved, the best case I-1 being from 97.5% at room temperature to 98.5% at 50 K. For the 50 kHz cases, the efficiency is greatly improved, the best case II-1 being from 90.0% at room temperature to 97.0% at 50 K. This indicates that switching losses have a stronger temperature dependence than conduction losses. Therefore low temperature operation offers greater performance benefits.

At both frequencies, the IGBT loss greatly decreases at low temperatures as seen in the simulation work. The diode loss remains at the room temperature level in the temperature range from room temperature down to 75 K because the slight increase of its on-state loss is counteracted by the slightly decreased switching loss at low temperatures.

There is a sudden drop for the diode power loss below 75 K. This is caused by the variation of the reverse recovery process: the reverse recovery peak current and reverse recovery time are both sharply reduced below 75 K. This suggests that the power diode may work much better in the temperature range below 75 K. However, further experimental work is required at temperatures below 75 K to examine these effects in more detail.
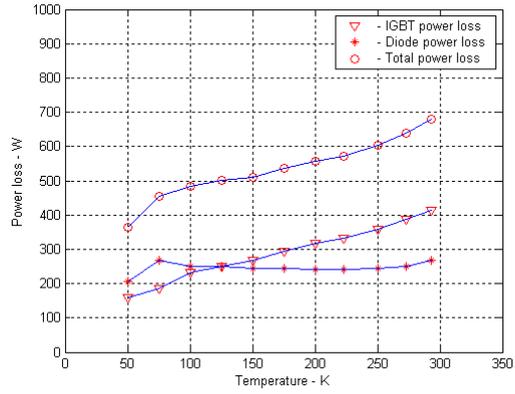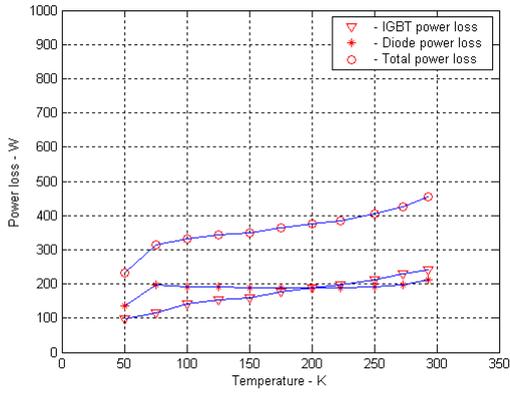
(a) Case I-1, D=0.3
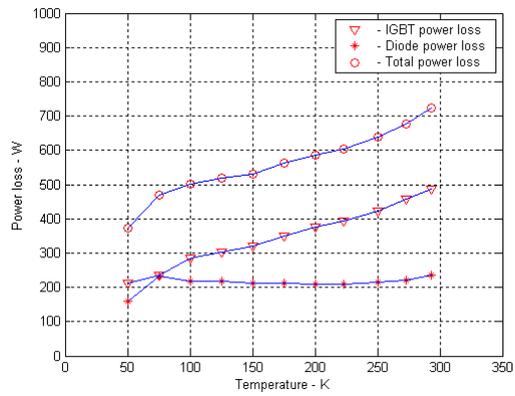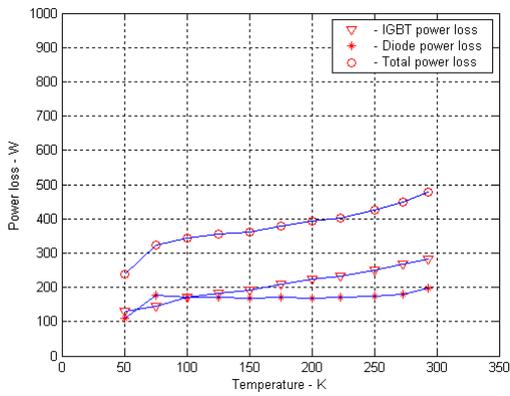
(b) Case I-2, D=0.5
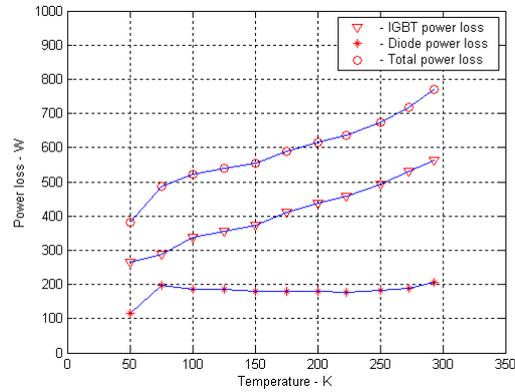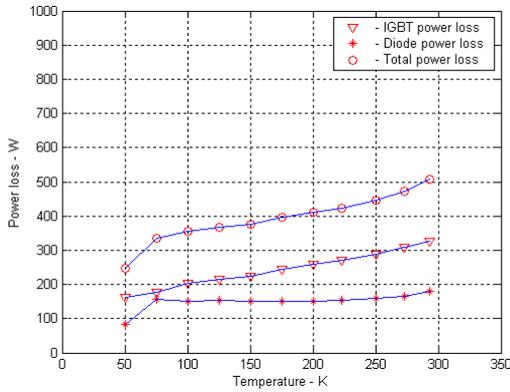
(c) Case I-3, D=0.7

Figure 5-5 Buck converter energy losses for Mode I, 10 kHz
Left: 100A; right: 150 A.
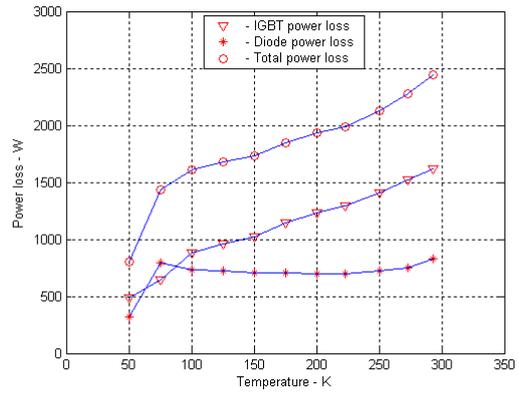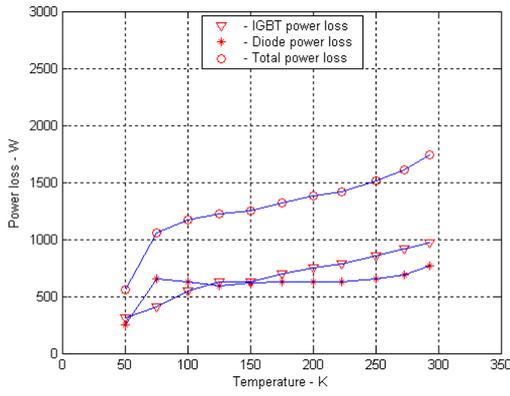
(a) Case II-1, D=0.3
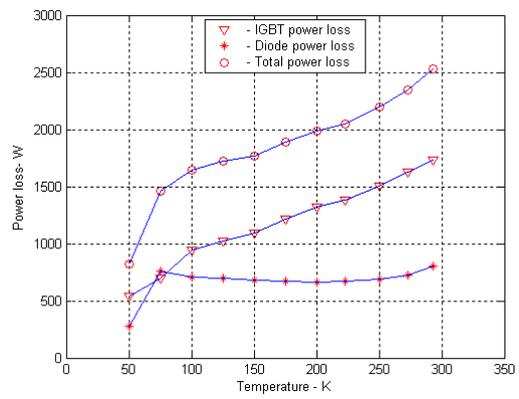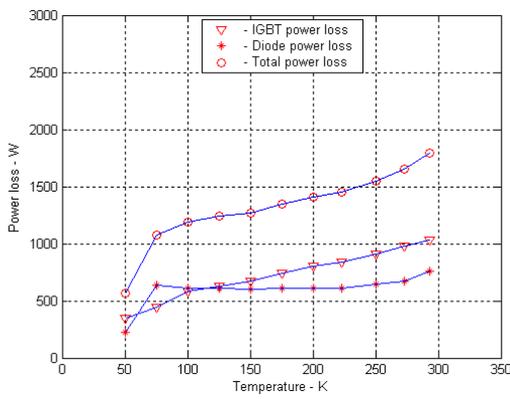
(b) Case II-2, D=0.5
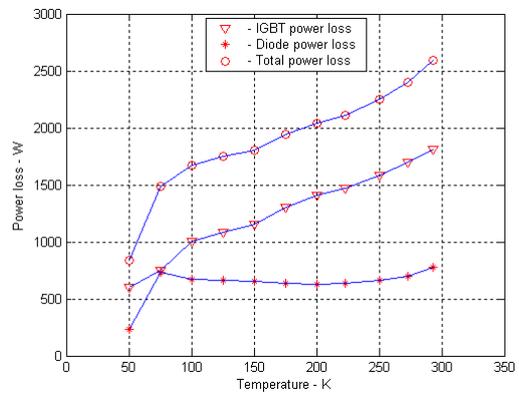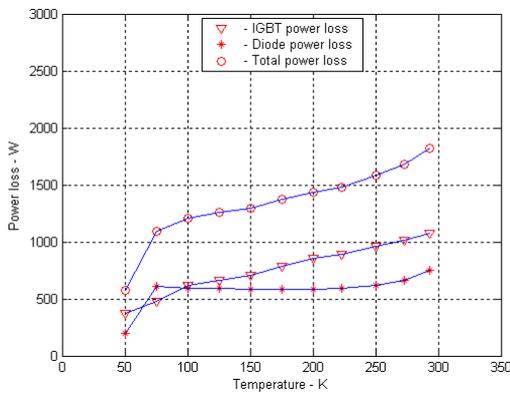
(c) Case II-3, D=0.7
Figure 5-6 Buck converter energy losses for Mode II, 50 kHz
Left: 100A; right: 150 A.
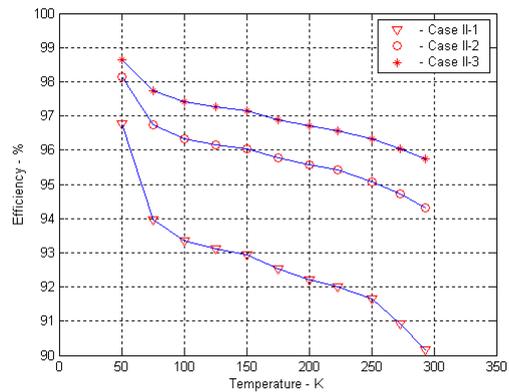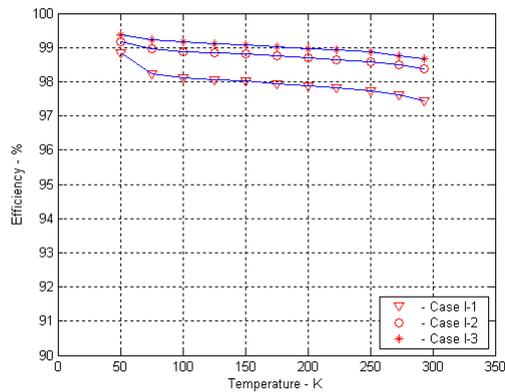
(a) Mode I, 10 kHz   (b) Mode II, 50 kHz

Figure 5-7 Buck converter efficiency variation against temperature

5. 2. 3 Converter summary

A DC-DC step-down converter consisting of an IGBT and a diode was simulated in Saber from room temperature down to 50 K. The operation at two switching frequencies, 10 kHz and 50 kHz was simulated and in particular attention was concentrated on the power device loss variation against temperature.

The simulation results suggest that the converter operates more efficiently at low temperatures due to the reduction of power device losses, especially when the switching frequency is quite high. The efficiency for the 50 kHz case being improved from 90.0% at room temperature to 97.0% at 50 K compared with 97.5% to 98.5% for the 10 kHz case. This suggests that low temperature operation may be more appropriate for the high frequency power electronics applications.

The benefit at low temperature mainly comes from the reduction of the IGBT loss since there is only a small variation of the diode power loss from room temperature down to 75 K.

However, a sudden reduction of the diode power loss from 75 K to 50 K suggests that diode may work better below 75 K. This effect requires further investigation.

5. 3 PWM Inverter leg simulations

The voltage-source DC-to-AC inverter leg is studied here. The circuit accepts a DC voltage source as input and produces a single-phase sinusoidal AC voltage output with a frequency that is much lower than the switching frequency.

5. 3. 1 Inverter circuit

The basic inverter leg circuit is shown in Figure 5-8 (a). For ease of explanation, the input DC voltage V_{dc} is assumed to be constant. The inverter switches are operated using naturally sampled pulse width modulation to shape and control the output voltage. As shown in Figure 5-8(b), the sinusoidal control signal $v_{control}$ is used to modulate the switching duty ratio and has a frequency f_1 that establishes the desired fundamental frequency of the output voltage. The control signal is compared with a triangular waveform with a frequency f_s, which establishes the inverter switching frequency and is generally kept constant along with its amplitude V_{tri}.

The depth of modulation m_a is defined as

$$m_a = \frac{V_{control}}{V_{tri}}$$

(5-13)

and the frequency ratio m_f is defined as

$$m_f = \frac{f_s}{f_1}$$

(5-14)

The fundamental-frequency component of the output voltage is given by [5-1]

$$(V_{oi})_1 = m_a \times \frac{V_{dc}}{2}$$
(5-15)

In a sinusoidal PWM, the amplitude of the fundamental-frequency component of the output voltage varies linearly with m_a provided that m_a is in the range from 0 to 1, which is referred to as the linear range and the output voltage is free of low-order harmonics. In the overmodulation range, $m_a > 1$, significant low-order harmonics occur in the inverter output voltage.

The harmonics in the inverter output voltage waveforms appear as sidebands, centred around the switching frequency and its multiples, that is, around harmonics m_f, $2\,m_f$, $3\,m_f$, and so on. This general pattern holds true for all values of m_a in the range of 0 to 1.

For a frequency ratio $m_f \geq 9$, the harmonic amplitudes are almost independent of m_f. The harmonics can be treated as a function of the amplitude modulation ratio m_a [5-1].
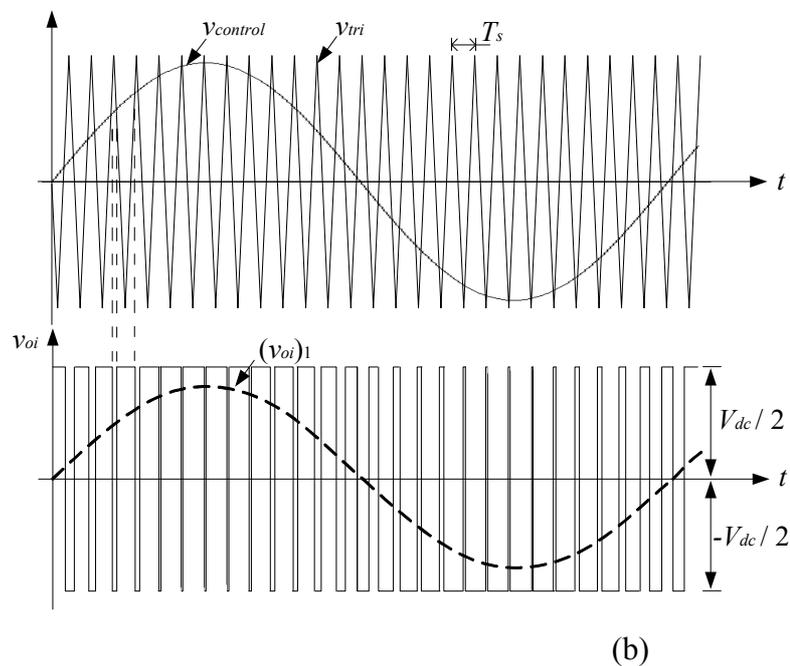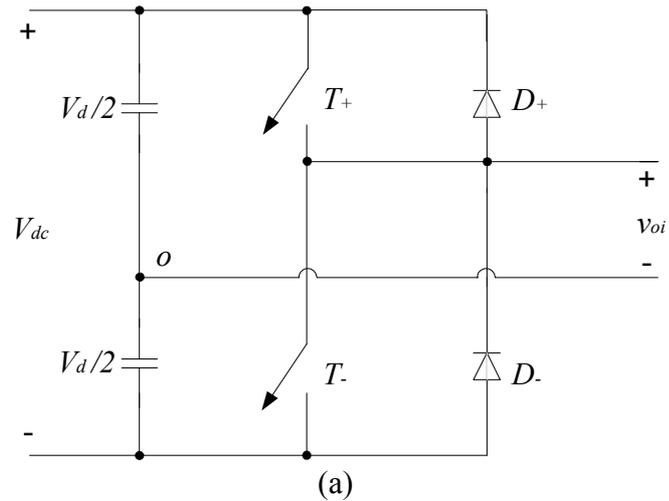
Figure 5-8 Basic inverter leg circuit and PWM waveforms
(a) the inverter leg circuit; (b) PWM waveforms

In the simulation work, the switch and diode in the basic inverter leg are formed by the models of the 1700 V NPT IGBT and the associated anti-parallel diode. V_{dc} is selected as 600 V and the two capacitors in the DC link are replaced by two voltage sources since the capacitors normally have very large values. The simulation circuit is shown in Figure 5-9 (a). The load selection will be discussed later.

The gate drive signals of ±15V are generated from a simple naturally sampled modulator consisting of a triangular waveform generator and comparator. The blanking times are added at the logic buffer and inverter block, and the logic signal is then converted into a voltage signal. A 15 V offset voltage is subtracted from the voltage signal to obtain bi-directional gate voltages. The gate voltage used here is in the rage of ± 15 V. A 4.7 Ω gate resistor is used for each IGBT device.

(a)

(b)
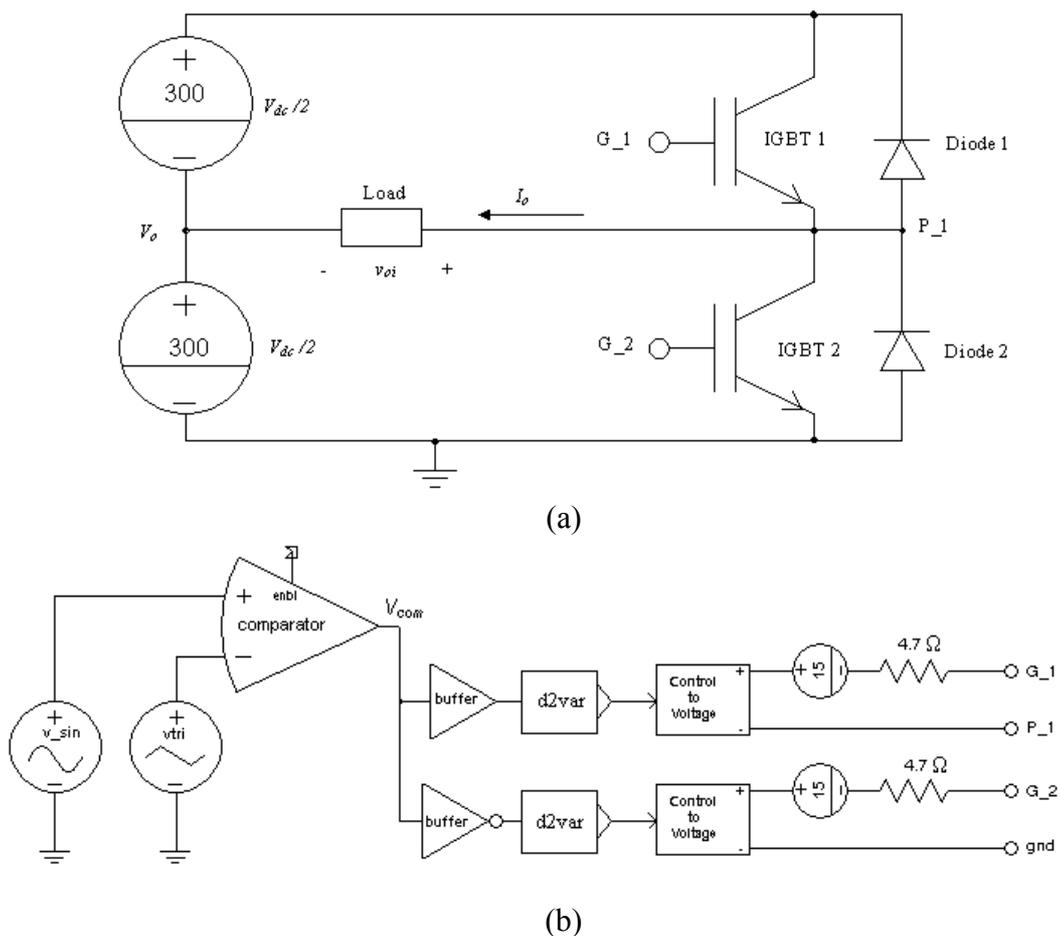
Figure 5-9 Inverter leg simulation circuit
(a) The inverter leg circuit; (b) the gate circuit.

5. 3. 2 Simulation work

Two values of m_a, the depth of modulation, namely 0.9 and 0.5, are simulated, which are referred to as mode I and II, and the output frequency is set at 50 Hz. According to (5-15),

the output fundamental frequency voltage amplitude is $(V_{oi})_1 = 0.9 \times 300 = 270$ V when $m_a = 0.9$. To supply an output current of 150 A, the impedance of the load should be:

$$Z_L = \frac{(V_{oi})_1}{(I_{oi})_1} = \frac{270}{150} = 1.80 \ (\Omega) \tag{5-16}$$

Three loads with different fundamental frequency power factors are studied, which are 0.75, 0.85 and 0.95. The corresponding resistance and inductance values being

- For $\cos\psi = 0.75$, R=1.35 Ω, L=3.8 mH;

- For $\cos\psi = 0.85$, R=1.53 Ω, L= 3.0 mH;

- For $\cos\psi = 0.95$, R=1.71 Ω, L=1.8 mH.

For $m_a = 0.9$, four cases have been studied as listed in Table 5-2 (a). Three cases have the three different loads, and an inverter switching frequency of 5 kHz. For the fourth case, the inverter leg switches at 20 kHz and the load power factor is 0.85.

The simulations are repeated with the lower depth of modulation of 0.5, all the parameters remaining unchanged as shown in Table 5-3b. As a result, the inverter leg operates at a lower current level, around 83 A.

Mode I	m_a	V_{dc} (V)	$(V_{oi})_1$ (V)	I_o (A)	Z (Ω)	$\cos\psi$	f_s (kHz)
Case I-1	0.9	600	270	150	1.8	0.75	5
Case I-2	0.9	600	270	150	1.8	0.85	5
Case I-3	0.9	600	270	150	1.8	0.95	5
Case I-4	0.9	600	270	150	1.8	0.85	20

(a) Mode I, m_a =0.9

Mode II	m_a	V_{dc} (V)	$(V_{oi})_1$ (V)	I_o (A)	Z (Ω)	$\cos\psi$	f_s (kHz)
Case II-1	0.5	600	150	83	1.8	0.75	5
Case II-2	0.5	600	150	83	1.8	0.85	5
Case II-3	0.5	600	150	83	1.8	0.95	5
Case II-4	0.5	600	150	83	1.8	0.85	20

(b) Mode II, m_a=0.5

Table 5-2 Parameters for the inverter leg simulation
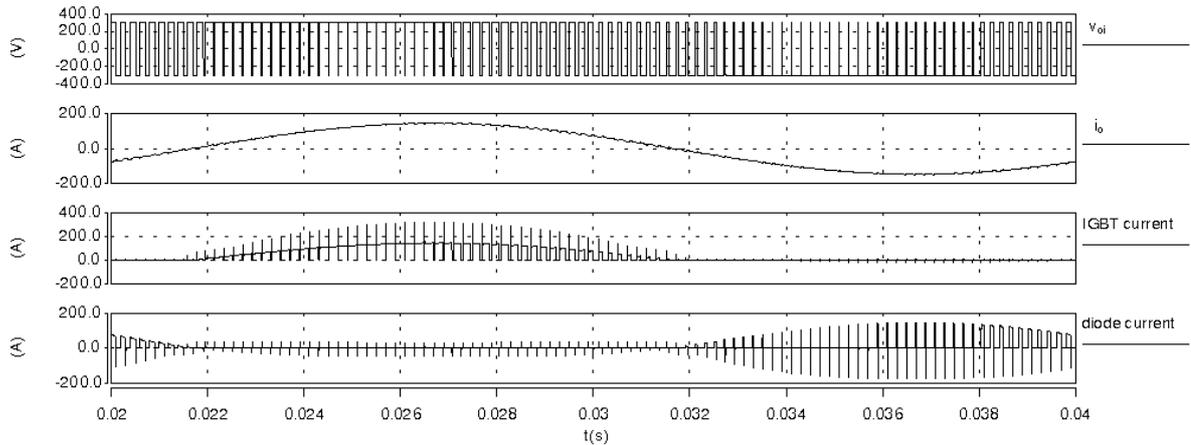
Figure 5-10 Inverter current and voltage waveforms for case I-2
From top to bottom: v_{oi}, i_o, i_{IGBT}, i_{diode}

Figure 5-10 shows the steady-state voltage and current waveforms in one fundamental cycle 0.02s from the simulation of case I-2. The PWM output voltage generates an almost sinusoidal current through the inductive load. The THD in the load current is 2.03% due to small dead time. The transient overshoots in the IGBT and diode current waveforms are caused by the diode reverse recovery.

The energy loss in the devices in the simulations is calculated by integrating the product of the current and voltage across the IGBT and diode in one cycle, 0.02s. From the results shown in Figure 5-11 and 5-12, the total energy loss decreases by a factor of 2 and 3 from room temperature down to 50 K for the 5 kHz cases and 20 kHz respectively. Similar to the DC-DC converter cases, the inverter leg efficiency improvement is much greater at the higher frequency. The efficiency variation against temperature is shown in Figure 5-13. For the 5 kHz cases, the efficiency is slightly improved at cryogenic temperatures, the best case II-1 being from 94.6% at room temperature to 97.3% at 50 K. For the 20 kHz cases, the efficiency is greatly improved, the best case II-1 being from 86.6% at room temperature to

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95.3% at 50 K. Similar to the simulation of the DC-DC converter, the total energy loss reduction at low temperature mainly comes from the IGBT, the diode losses varying relatively little.

The power factor has little effect on the inverter energy loss as shown in Figure 5-11 and 12. The IGBT energy loss values for the m_a=0.5 cases are less than half of those for the m_a=0.9 cases because of the reduction of the current level and also the shorter conduction time of the device. However, the diode energy loss values for the m_a=0.5 cases are approximately the same as those for the m_a=0.9 cases because the reduction of the current level balances the increase in the conduction time.
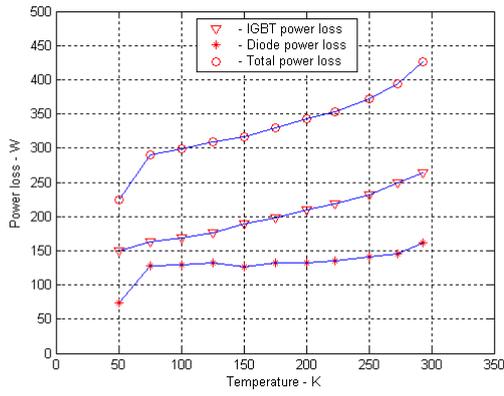
(a) Case I-1
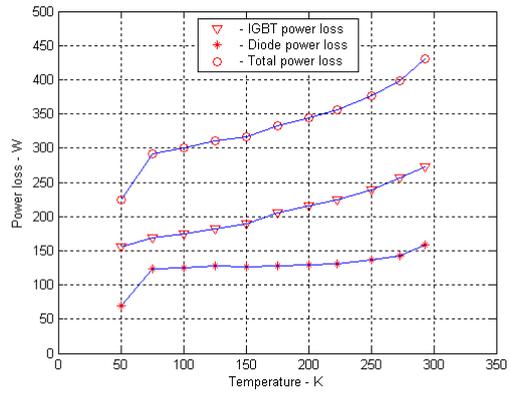
(b) Case I-2
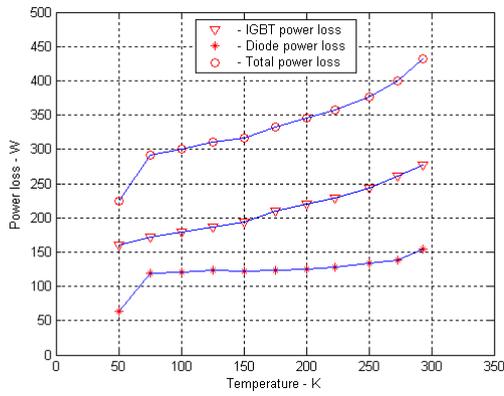
(c) Case I-3
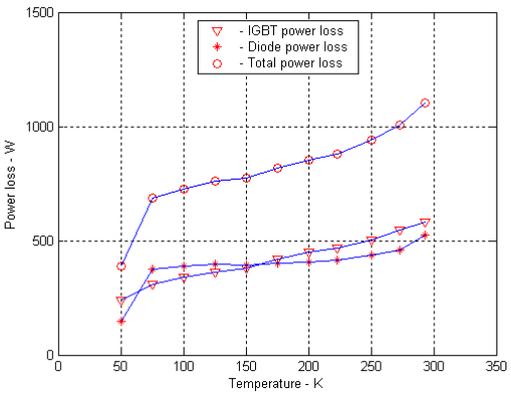
(d) Case I-4

Figure 5-11 Inverter energy losses for Mode I, m_a =0.9
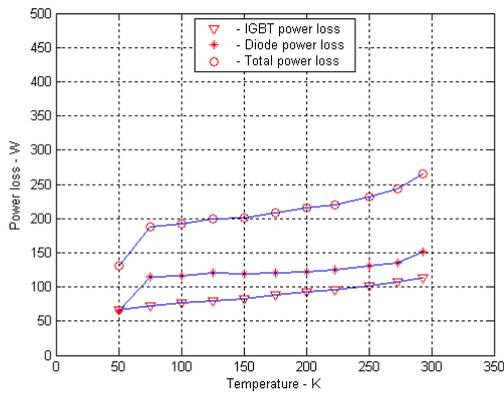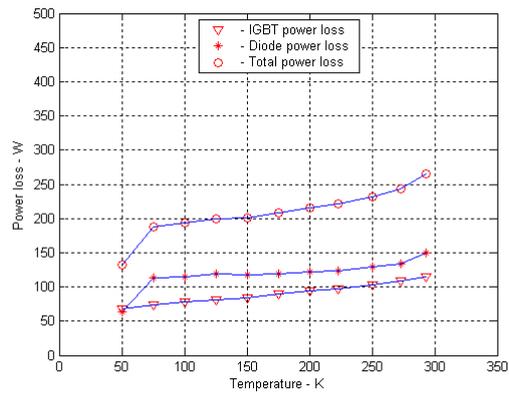
(a) Case II-1 (b) Case II-2
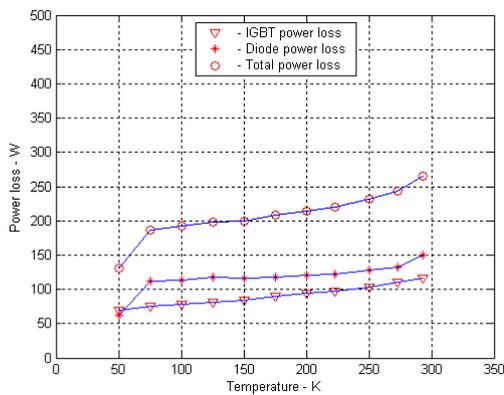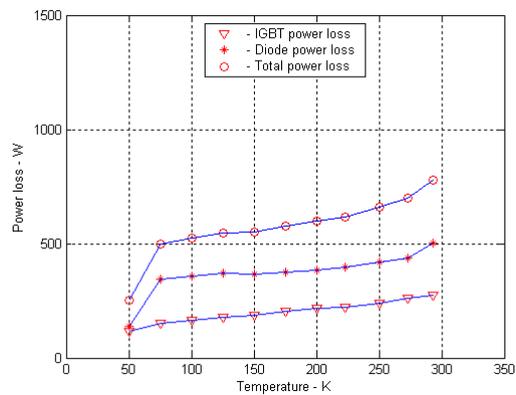
(c) Case II-3 (d) Case II-4

Figure 5-12 Inverter energy losses for Mode I, m_a =0.5
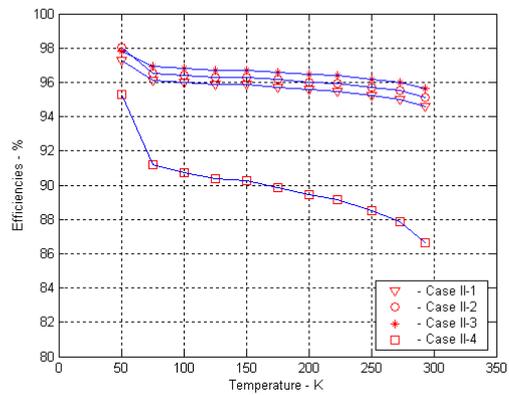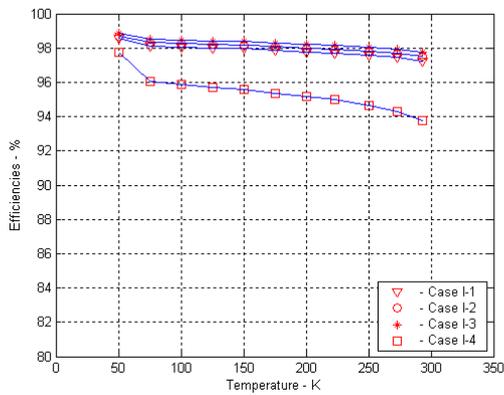
Figure 5-13 Inverter efficiency variation against temperature
Left: Mode I, m_a=0.9; right: Mode II, m_a=0.5

5. 3. 3 Inverter summary

An inverter leg consisting of IGBTs and diodes was simulated in Saber from room temperature down to 50 K.

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The simulation results suggest that the inverter leg operates more efficiently at low temperatures due to the reduction of power device losses, especially when the switching frequency is quite high. The efficiency for the 20 kHz case is improved from 86.6% at room temperature to 95.3% at 50 K, much greater than the 5 kHz case which shows an increase from 94.6% to 97.3%. The benefit of low temperature operation mainly comes from the reduction of the IGBT loss.

5.4 Summary

A DC-DC converter and an inverter leg, including the IGBT and diode temperature-dependent models, are simulated in Saber from room temperature down to 50 K. The simulation results show that the power electronic circuits work more efficiently at low temperatures. The benefit at low temperatures mainly comes from the reduction of the IGBT energy loss. The diode energy loss shows little variation over the whole temperature range from room temperature down to 50 K.

However, the temperature effect on other components, like the capacitor and inductor, in the converter and inverter circuits is not considered in the simulation work. More research work, including both experiment and simulation work, needs to be done to implement the cryogenic converters and inverters.

Also, the possible suggested improvement in diode switching characteristics at very low temperature warrants further investigation.

Statement of original contributions

The circuit level IGBT and diode models are used to simulate the performance of DC/DC step-down converter and a sinusoidal pulse-width-modulated inverter leg at cryogenic temperatures. The simulation results show that the power electronic circuits work more efficiently at low temperatures. For example, the efficiency of the DC-DC converter working at 50 kHz is increased from 90.0% at room temperature to 97.0% at 50 K.

References
[5-1] Mohan, M.; Undeland, T. and Robbins, W., *Power Electronics: Converters, Applications and Design*, Wiley, 1989

Chapter 6   Conclusions and further work

6. 1 Introduction

Cryogenic operation has been identified as a possible way of improving the performance of power electronic devices and circuits, for example reducing the losses in the devices themselves and increasing power density. Furthermore as superconductoring machines, fault current limiters and magnetic energy storage systems are developed, it is possible that requirements will emerge for the associated power electronics equipment to be co-located in the cryosystem, bringing overall system benefits.

The silicon devices suitable for the applications in the temperature range of 77 K to 300 K are nearly always field-effect transistors: MOSFET, JFET, MESFET and IGBT. Through re-optimisations, the diode may be able to find applications at low temperatures. The MOSFET has been demonstrated in cryogenic energy conversions in vehicles and spacecraft. The bipolar junction transistor is not anticipated to be an attractive choice at cryogenic temperatures because of a large reduction in its current gain and a reduced on-state current density. The IGBT is expected to replace it in most applications as it has done at room temperature [6-1]. The cryogenic characteristics of power IGBTs were explored in this thesis by means of experiments, modelling and simulations.

6. 2 Contribution of this thesis

Three types of IGBT were selected: Punch-through (PT) IGBT, Non-Punch-Through (NPT) and IGBT3. The PT and NPT are conventional technologies and are widely used in the power industry. The IGBT3 represents the main field for improvements in IGBT technology,

combining the trench gate and field-stop concepts [6-2, 3]. As a recent entrant in the power device market, the cryogenic performance of IGBT3 has not been reported. The main work carried out in the temperature range of 50 K to room temperature is reviewed in the following subsections.

6. 2. 1 Experimental exploration of three types of IGBTs

A cryosystem comprising a temperature controlled cold head and vacuum chamber was built. The cold head is a metallic plate to hold the test sample that can be cooled from room temperature down to 20 K within approximately 40 minutes. A temperature regulation circuit was constructed to regulate the cold head temperature.

Three types of IGBT half-bridge modules, including PT, NPT and IGBT3 devices, have been selected to carried out the static tests, gate charge tests, and switching tests in the temperature range of 50 K to 300 K. Compared to commercial-off-shelf devices, the sample devices are gel free –important as the insulation gel degraded at low temperatures.

The IGBT performances, both on state and switching, were greatly improved at cryogenic temperatures. The on-state voltage and turn-off time showed significant reductions at low temperatures. The reductions in on-state voltage drop are around 20-30 %, and the turn-off time reduces by a factor of approximately three or four over the temperature range from room temperature down to 50 K.

However, the breakdown levels of the IGBTs decreased at low temperatures. The forward breakdown voltage of the IGBT3 showed a dramatic reduction, around 60%, twice of those

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of the NPT and PT devices. The re-optimisation of the drift area in the IGBT3 may be necessary avoid such a degradation at low temperatures.

The diodes in the tested IGBT modules showed slightly higher on-state voltage drops at low temperatures and their reverse recovery processes were shorter.

6. 2. 2 Modelling of IGBTs

A physically based compact device model from the University of Wales, Swansea, was selected to model the low temperature effects of the three tested IGBTs. A generic Saber power diode model with reverse recovery was selected to model the low temperature effect of the diode. The results from static tests, gate charge tests and switching tests were used to parameterise the models. The results from the simulation work using the IGBT and diode models agree very well with the experimental results, confirming the validity of these simple models for representing the devices at cryogenic temperatures.

6. 2. 3 Simulation of converters

A DC-DC buck converter and an inverter leg, including the IGBT and diode temperature-dependent models, were simulated in Saber over the temperature range of 50 K to 300 K. The simulation results showed that the power electronic circuits could work more efficiently at low temperatures. For example the efficiency of the DC-DC converter working at 50 kHz is increased from 90.0% at room temperature to 97.0% at 50 K and the efficiency of the inverter leg working at 20 kHz is improved from 86.6% at room temperature to 95.3% at 50

K. This benefit mainly comes from the reduction of the IGBT energy loss at low temperatures.

6. 3 Further work

The work carried in the thesis is still far from practical application. The further work may include:

(1) Further characterisation of cryogenic IGBTs

The main cryogenic characteristics were explored through experimental work described in the thesis. However, theoretical explanations on the physical level are necessary to fully understand these cryogenic characteristics, especially the degradation of the forward breakdown levels of the IGBT3. With further understanding of the cryogenic characteristics of IGBTs, the cryo-IGBT can be developed with a re-optimised structure to provide improved characteristics at cryogenic temperatures.

(2) Further modelling of cryogenic IGBTs

More detailed models, like level-2 or 3, may be necessary to obtain more knowledge about the cryogenic performance of IGBTs. The modelling work may need the further cryogenic tests of IGBTs to parameterise the models. The modelling results will be helpful to understand the cryogenic performance of IGBTs. In particular a more detailed study of the device behaviour in the temperature range 20-70 K is likely to reveal valuable results and insight.

(3) Further study of cryogenic converters

The cryogenic experimental work on a multi-chip IGBT converter needs be carried out to check whether the efficiency can be further improved using a multi-chip IGBT compared with a wire-connected converter, as has been shown in the MOSFET-based cryogenic converters. Some simulation work may be needed to optimise the converter structure. On the basis of the experimental and simulation results, the re-optimised converter module working at cryogenic temperatures may be considered.

6. 4 Conclusions

The cryogenic characterisation of IGBTs carried out in this thesis proved that the IGBT could work more efficiently at low temperatures, with the decrease of on-state voltage and turn-off time, despite the decrease of breakdown levels. Further work is necessary to demonstrate and implement the cryogenic application of IGBTs. With the emerging requirements for clean energy and increased power densities, cryogenic power electronics may offer an effective means of reductions of system size, weight and increased efficiency.

References

[6-1] Singh, R.; Baliga, B., *Cryogenic Operation of Silicon Power Devices*, Kluwer Academic publishers, 1998

[6-2] Laska, T.; Pfirsch, F.; Hirler, F.; Niedermeyr, J.; Schaffer, C. and Schmidt, T., 1200 V-trench-IGBT study with square short circuit SOA, *IEEE International Symposium of Power Semiconductor Devices & ICs'1998 (ISPSD'1998)*, pp. 433– 436, 1998

[6-3] Laska, T.; Munzer, M.; Pfirsch, F.; Schaeffer, C. and Schmidt, T., The Field Stop IGBT (FS IGBT). A new power device concept with a great improvement potential, *IEEE International Symposium of Power Semiconductor Devices & ICs'2000 (ISPSD'2000),* pp. 355– 358, 2000

Appendix 1 List of publications resulting from work in this thesis

Papers published:

S. Yang, A. Forsyth, Characterisation of Power Devices for Extreme Low Temperature Operation, *10th European Conference on Power Electronics and Applications*, September 2003, Toulouse, France

S. Yang, A. Forsyth, Characterisation of 1700 V Trench Field Stop IGBTs for Extreme Low Temperature Operation, *Sixth European Workshop on Low Temperature Electronics (WOLTE-6)*, June 2004, Noordwijk, the Netherlands

Papers in preparation:

A. Forsyth, S. Yang, P. Mawby and P. Igic, Modelling and simulation of cryogenic power electronic converters, *IEE Proceedings on Circuits, Devices and Systems*
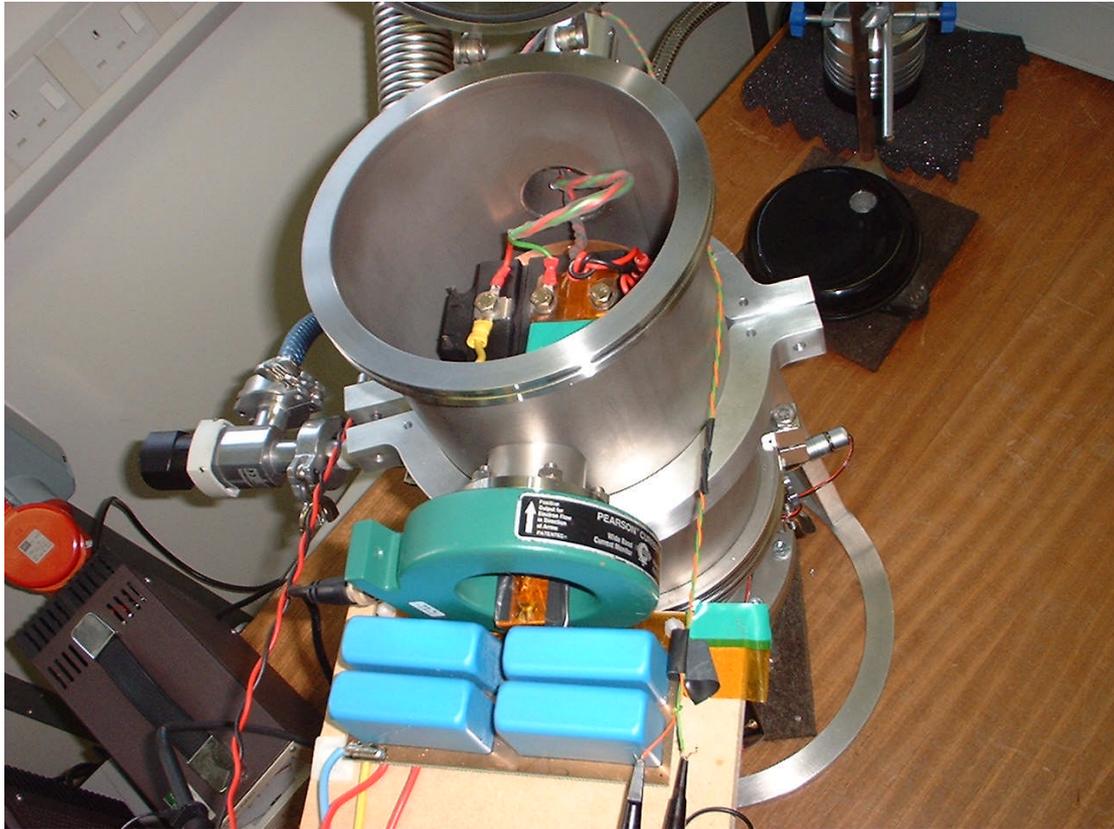
Appendix 4 MIL-STD-750D test method 3471 for semiconductor devices

METHOD 3471.2

GATE CHARGE

1. <u>Purpose</u>. The purpose of this test is to measure the gate charge (Q_g) of power MOSFET's and IGBT. For the IGBT, replace the drain and source MOSFET designations with collector and emitter IGBT designations, D = C and S = E.

1.1 <u>Definitions</u>.

a. Test 1: $Q_{g(th)}$ is the gate charge that must be supplied to reach the minimum specified gate-source threshold voltage. It establishes line loci through the origin of a $Q = f(V_{gs})$ graph that is invariant with I_D, V_{DD}, and T_J. It establishes a relationship with capacitance (i.e.,

$$C_{GS} = \frac{Q_{g(th)}}{V_{g(th)}} = \frac{Q_{gs}}{V_{GP}}).$$

b. Test 2: $Q_{g(on)}$ is the gate charge that must be supplied to reach the gate-source voltage specified for the device $r_{DS(on)}$ measurement.

c. Test 3: $Q_{gm(on)}$ is the gate charge that must be supplied to the device to reach the maximum rated gate-source voltage. $Q_{gm(on)}$ and $Q_{g(on)}$ establish line loci on a $Q = f(V_{gs})$ graph that may be considered invariant with I_D and T_J. The slope of the loci is invariant with V_{DD}, while the intercept with the Q axis is variant with V_{DD}.

d. Test 4: V_{GP} is the gate voltage necessary to support a specified drain current. V_{GP}, I_D is a point on the device gate voltage, drain current transfer characteristic. V_{GP} is variant with I_D and T_J. It may be measured one of two ways:

(1) Using a dc parameter test set employing a circuit similar to that described in method 3474 for SOA setting $V_{DD} > V_{GS}$.

(2) Using a gate charge test circuit employing a constant I_D drain load.

e. Test 5: Q_{gs} is the charge required by C_{GS} to reach a specified I_D. It is variant with I_D and T_J. It is measured in a gate charge test circuit employing a constant drain current load.

f. Test 6: Q_{gd} is the charge supplied to the drain from the gate to change the drain voltage under constant drain current conditions. It is variant with V_{DD} and may be considered invariant with I_D and T_J. It can be related to an effective gate-drain capacitance (i.e., $C_{rss} = Q_{gd}/V_{DD}$). The effective input capacitance is: $C_{iss} = C_{GS} + C_{rss}$.

2. Test procedure.

a. The gate charge test is performed by driving the device gate with a constant current and measuring the resulting gate source voltage response. Constant gate current scales the gate source voltage, a function of time, to a function of coulombs. The value of gate current is chosen so that the device on-state is of the order of 100 µs.

    The resulting gate-source voltage waveform is nonlinear and is representative of device behavior in the low to mid-frequency ranges. The slope of the generated response reflects the active device capacitance ($C_g = dQ_g /dV_{GS}$) as it varies during the switching transition. The input characteristic obtained from this test reflects the chip design while avoiding high frequency effects.

b. Figure 3471-1 is the test circuit schematic for testing an n-channel device. Polarities are simply reversed for a p-channel device.

c. Figure 3471-2 is an example of a practical embodiment of figure 3471-1. It illustrates a gate drive and instrument circuit that will test n-channel and p-channel devices.

d. The circuit has I_g programmability ranging from microamperes to milliamperes. For very large power MOSFET devices, the output I_g can be extended to tens of milliamperes by paralleling additional CA3280 devices.

e. The circuit provides an independent gate voltage clamp control to prevent voltage excursions from exceeding test device gate voltage ratings.

f. The CA3240E follower ensures that the smallest power devices will not be loaded by the oscilloscope. (R_{in} = 1.5 T Ω, I_{IN} = 10 pA, C_{IN} = 4 pF).

g. Gate charge is to be measured starting at zero gate voltage to a specified gate voltage value.

h. The magnitude of input step constant gate current I_g should be such that gate propagation and inductive effects are not evident. Typically this means the device on-state should be of the order of 100 µs.

i. The dynamic response, source impedance, and duty factor of the pulsed gate current generator are to be such that they do not materially affect the measurement.

j. Typically, the instrument used for a gate charge measurement is an oscilloscope with an input amplifier and probe. The switching response and probe impedance are to be such that they do not materially affect the measurement. Too low a probe resistance relative to the magnitude of I_g can significantly increase the apparent Q_g for a given V_{GS}. Too high a value of probe capacitance relative to the device C_{iss} will also increase the apparent Q_g for a given V_{GS}.

$$I_g = \frac{C_g\, dV_{GS}}{dt}, \quad Q_g = C_g\, V_{GS}.$$

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3. <u>Summary</u>. Figure 3471-3 illustrates the waveform and tests 1 through 4, condition A. Figure 3471-4 illustrates the waveform for tests 2, 4, 5, and 6, condition B. Only four of the six tests need be performed since the results of the remaining two are uniquely determined and may be calculated. Either condition A or condition B may be used.

3.1 <u>Condition A</u>.

3.1.1 <u>Test 1, $Q_{g(th)}$</u>.

a. Case temperature (T_C): +25°C.

b. Drain current: $I_D \geq 100$ mA.

c. Off-state drain voltage (V_{DD}): Between 50 percent and 80 percent of the device's rated drain-source breakdown voltage.

d. Load resistor (R_L): Equal to V_{DD}/I_D.

e. Gate current (I_g): Constant gate current such that the transition from off-state to on-state or on-state to off-state is of the order of 50 µs. The value of I_g varies with die size and ranges from 0.1 mA to 5 mA.

f. Gate to source voltage ($V_{g(th)\,min}$): The minimum rated gate-source threshold voltage.

g. Minimum off-state gate charge ($Q_{g(th)}$): A minimum and maximum limit shall be specified.

3.1.2 <u>Test 2, $Q_{g(on)}$</u>.

a. T_C, I_D, V_{DD}, R_L, I_g: Same as test 1 in 3.1.1.

b. V_{GS}: The gate-source voltage specified for the $r_{DS(on)}$ test, $V_{(on)}$.

c. On-state gate charge ($Q_{g(on)}$): A minimum and maximum limit shall be specified.

3.1.3 <u>Test 3, $Q_{gm(on)}$</u>.

a. T_C, I_D, V_{DD}, R_L, I_g: Same as test 1 in 3.1.1.

b. V_{GS}: The maximum rated gate-source voltage, $V_{(max)}$.

c. Maximum on-state gate charge ($Q_{gm(on)}$): A minimum and maximum limit shall be specified.

3.1.4 <u>Test 4, V$_{GP}$.</u> This test is to be performed on a dc parameter test set.

a. I$_D$ = The continuous rated drain current at T$_C$ = +25°C.

b. V$_{DS}$ > V$_{GS}$. Normally V$_{DD}$ ≈ 3 V$_{GS}$ is satisfactory.

c. The pulse width and duty factor are such that they do not materially affect the measurement.

d. V$_{GP}$ shall be specified as a maximum and minimum.

e. T$_C$ = +25°C.

3.1.5 <u>Test 5, Q$_{gs}$; test 6, Q$_{gd}$.</u> No tests are required. The calculations in terms of the results of tests 1 through 4 are as follows:

a.
$$Q_{gs} = Q_{g(th)} \left[\frac{V_{GP}}{V_{g(th)min}} \right]$$

b. Determine the fully on-state charge slope:

$$m = \left[\frac{V_{(max)} - V_{(on)}}{Q_{gm(on)} - Q_{g(on)}} \right]$$

c. Determine the V$_{gs}$ axis intercept:

$$b = V_{(on)} - m \; Q_{g(on)}.$$

d. Calculate Q_{gd}: $Q_{gd} = \left[\frac{(V_{GP} - b)}{m} \right] - Q_{gs}.$

3.2 <u>Condition B.</u>

3.2.1 <u>Test 2, Q$_{g(on)}$.</u>

a. Case temperature (T$_C$): +25°C.

b. On-state drain current (I$_D$): The continuous rated drain current at T$_C$ = +25°C.

c. Off-state drain voltage (V$_{DD}$): Between 50 percent and 80 percent of the device's rated drain-source breakdown voltage.

d. The drain load shall be such that the drain current will remain essentially constant.

e. Gate current (I$_g$): Same as test 1 in 3.1.1, condition A.

f. Gate to source voltage V$_{(on)}$: Same as test 1 in 3.1.1, condition A.

g. On-state gate charge (Q$_{g(on)}$): A minimum and maximum limit shall be specified.

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3.2.2 <u>Test 4, V$_{GP}$</u>.

a. T$_C$, I$_D$, V$_{DD}$, Load, I$_g$: Same as test 2 in 3.2.1, condition B.

b. V$_{GP}$: This is the gate plateau voltage where Q$_{gs}$ and Q$_{gd}$ are measured. This voltage is essentially constant during the drain voltage transition when Q$_{gd}$ is supplied from the gate to the drain under constant I$_g$, I$_D$ conditions.

3.2.3 <u>Test 5, Q$_{gs}$</u>.

a. T$_C$, I$_D$, V$_{DD}$, Load, I$_g$: Same as test 2 in 3.2.1, condition B.

b. V$_{GS}$: Equal to V$_{GP}$ at the specified I$_D$.

c. Q$_{gs}$: A minimum and maximum limit shall be specified.

3.2.4 <u>Test 6, Q$_{gd}$</u>.

a. T$_C$, I$_D$, V$_{DD}$, Load, I$_g$: Same as test 2 in 3.2.1, condition B.

b. V$_{GS}$: Equal to V$_{GP}$ at the specified I$_D$.

c. Q$_{gs}$: A minimum and maximum limit shall be specified.

3.2.5 <u>Test 1, Q$_{g(th)}$; test 3, Q$_{gm(on)}$</u>. No tests are required. The calculations in terms of the results of test 2, 4, 5, and 6 are as follows:

a.
$$Q_{g(th)} = Q_{gs} \left[\frac{V_{g(th)} \min}{V_{GP}} \right].$$

b. Determine the fully on-state charge slope:

$$m = \left[\frac{V_{(on)} - V_{GP}}{Q_{g(on)} - Q_{gs} - Q_{gd}} \right]$$

c. Determine the V$_{gs}$ axis intercept:

$$b = V_{(on)} - m \, Q_{g(on)}.$$

d. Calculate Q$_{gm(on)}$:

$$Q_{gm(on)} = \frac{[V_{(max)} - b]}{m}$$

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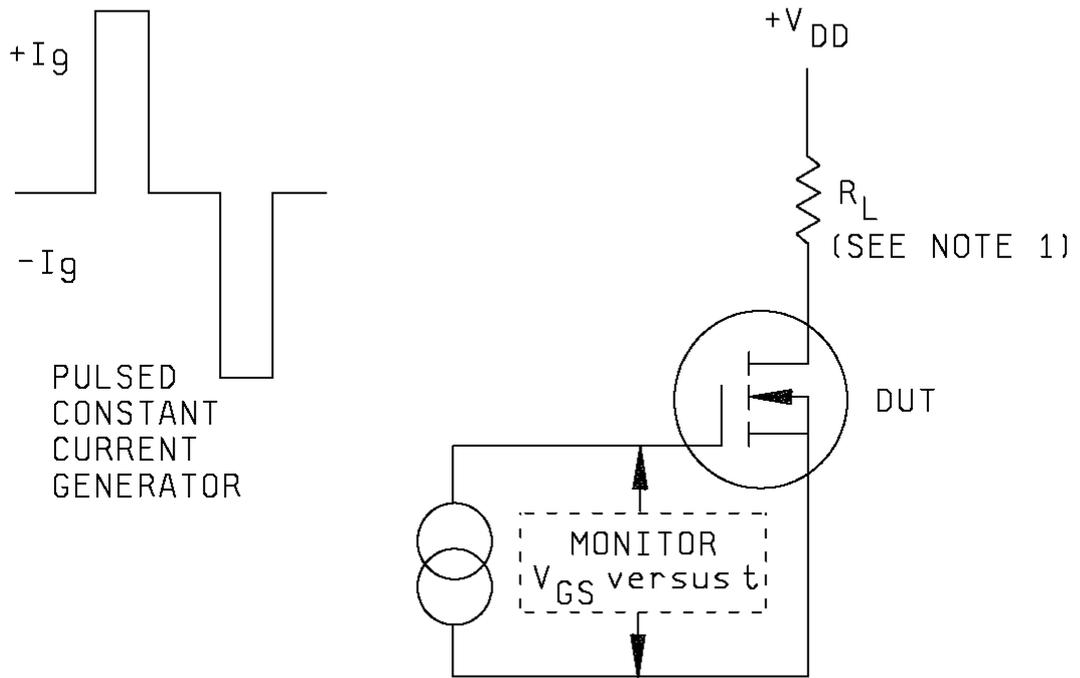
NOTES:
1. Condition B requires a constant drain current regulator.
2. $I_g \times t = Q_g$.

FIGURE 3471-1. Pulsed constant current generator.
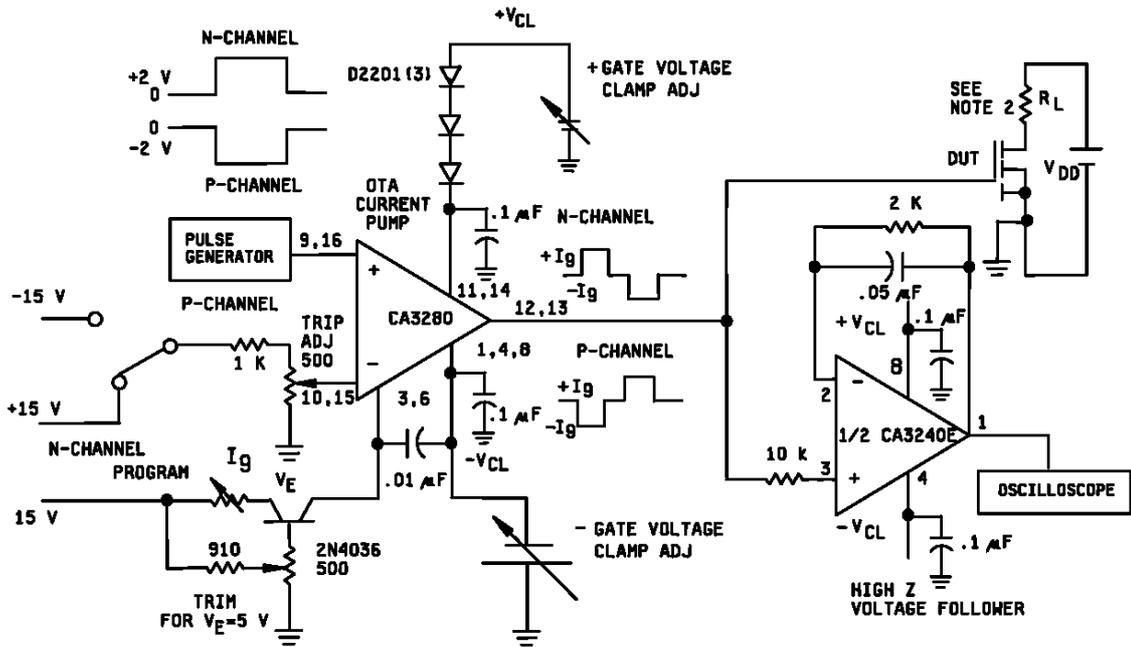
NOTES:
  1. This test method provides gate voltage as a monotonic function of gate charge. Charge or capacitance may be unambiguously specified at any gate voltage. Gate voltage assuring that the device is well into the on-state will result in very reproducible measurements. For a given device, the gate charges at these voltages are independent of drain current and a weak function of the off-state voltage.
  2. Condition B requires a constant current drain regulator.

FIGURE 3471-2. Practical gate charge test circuit.
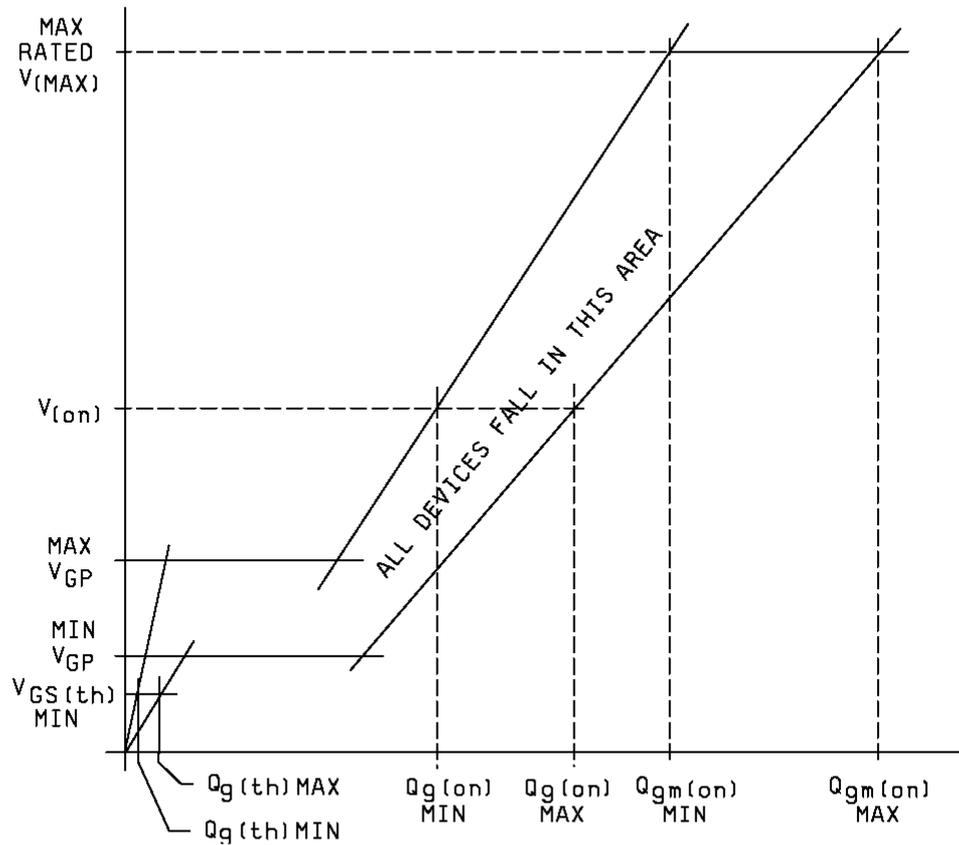
NOTES:
1. $Q_g = I_g t$.
2. V_{GP} is measured by a dc test, same I_D, $V_{DS} >> V_{GP}$ (see 3.14).
3. $V_{(max)}$ and $V_{(on)}$ are <u>specified</u> voltages for charge measurements $Q_{gm(on)}$ and $Q_{g(on)}$.
4. $V_{GS(th)}$ min is a <u>specified</u> voltage for measuring $Q_{g(th)}$.

FIGURE 3471-3. <u>Gate charge characterization showing measured characteristics</u>.

182
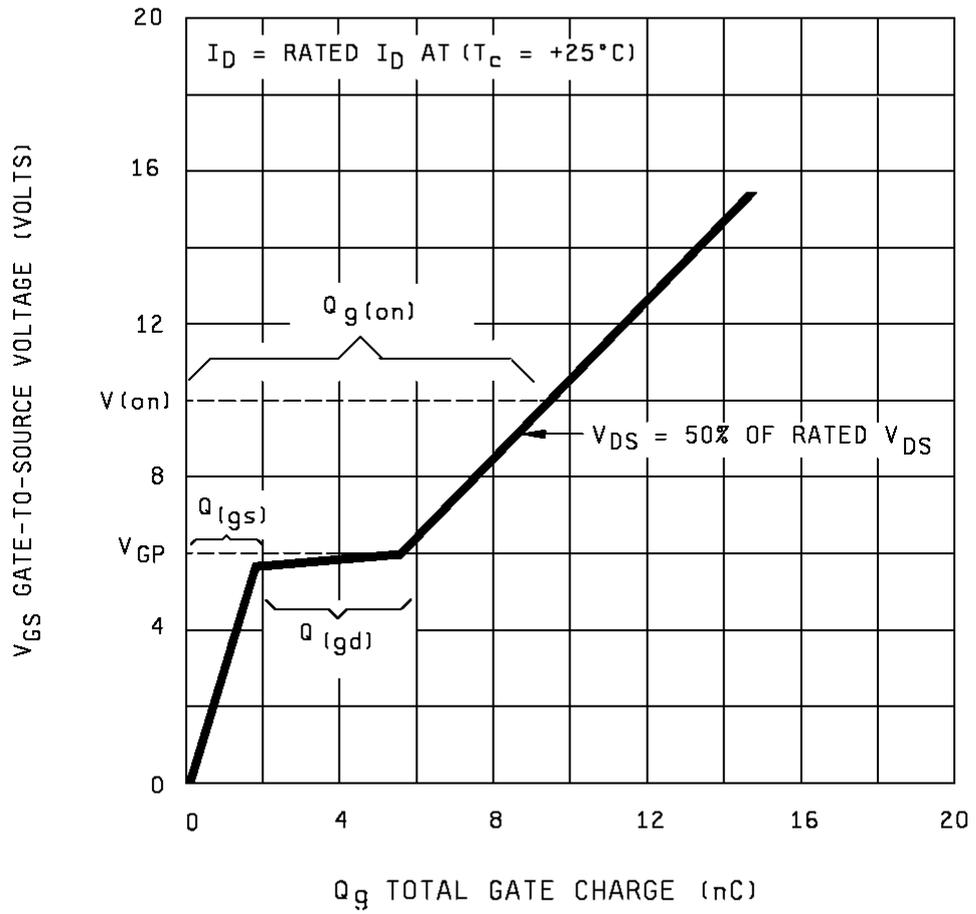
FIGURE 3471-4. Gate charge, condition B.
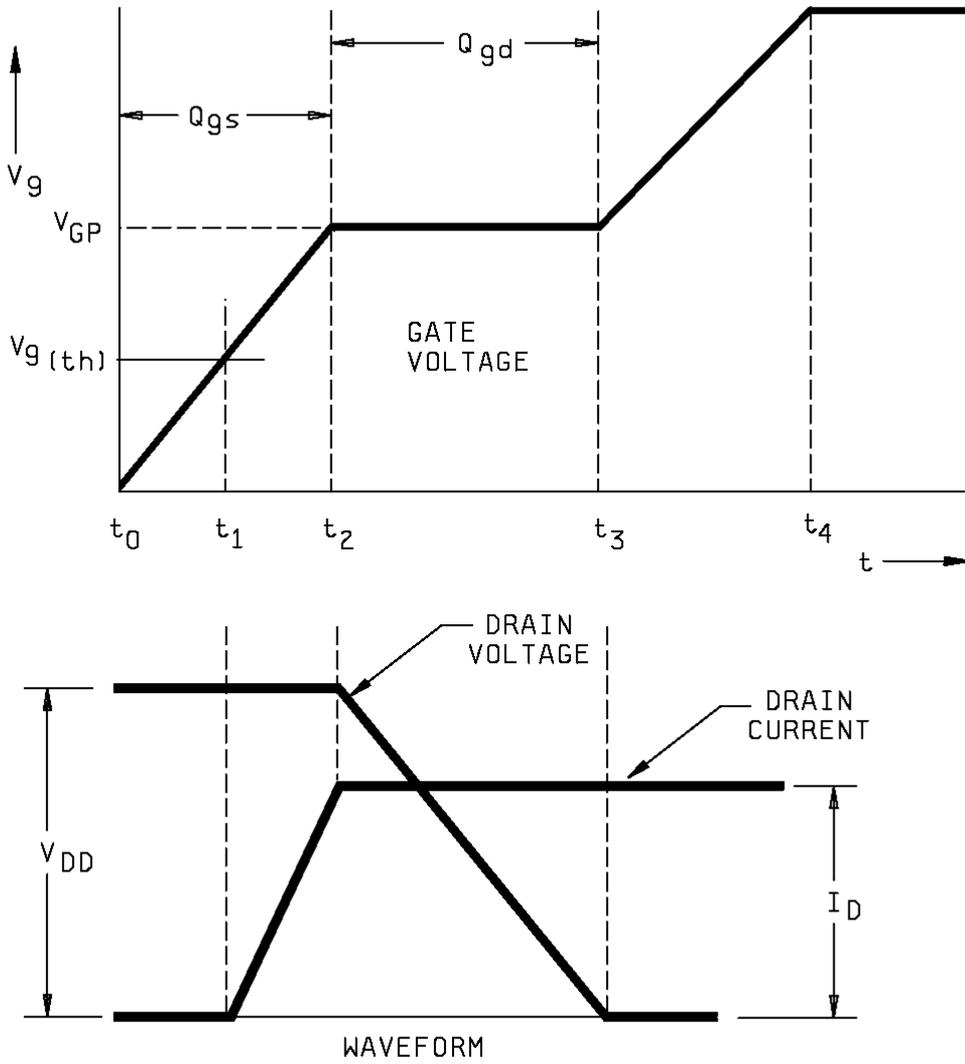
FIGURE 3471-5. Idealized gate charge waveforms, condition B.

184
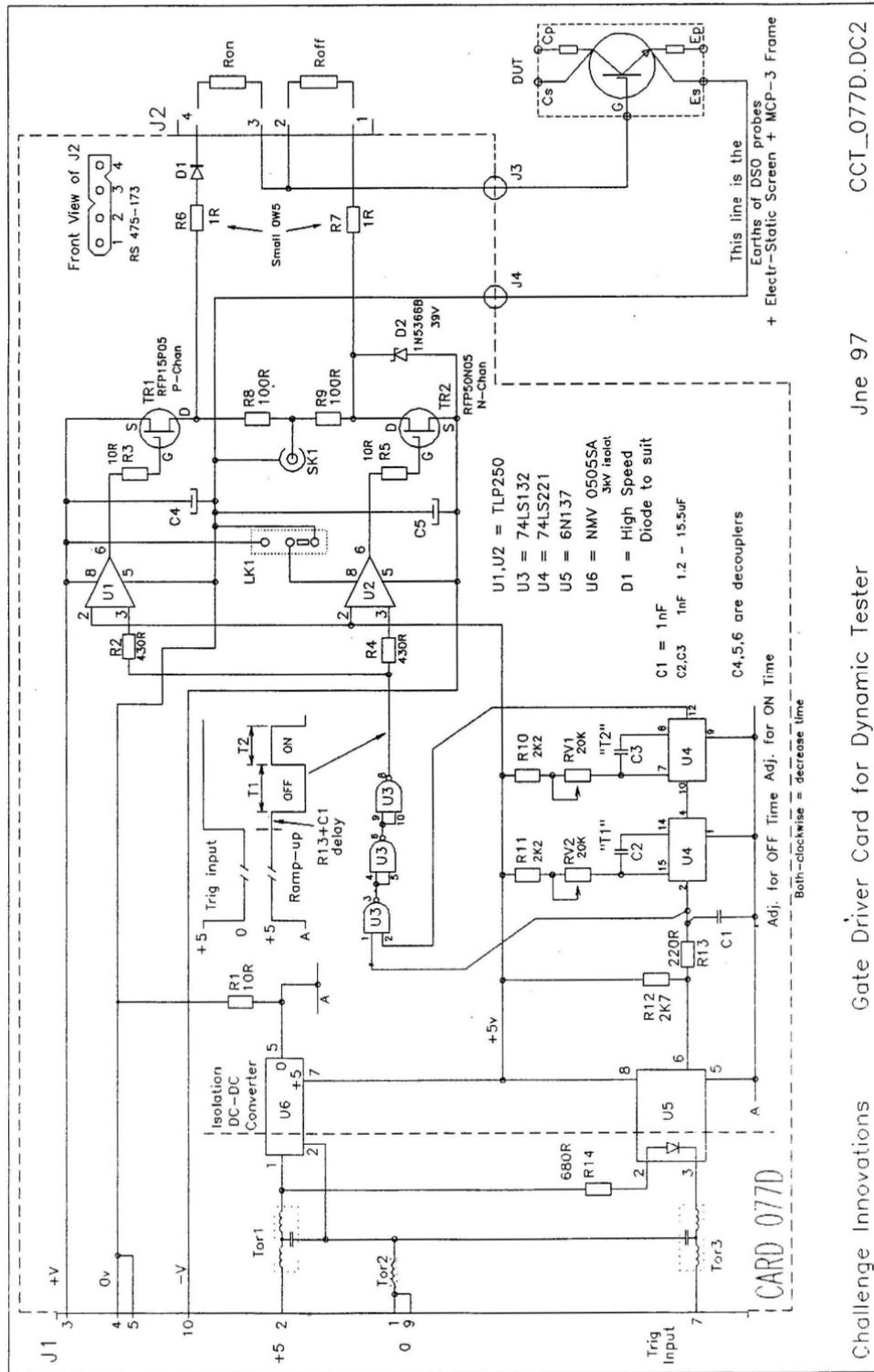
Gate Driver Card for Dynamic Tester

Challenge Innovations

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Appendix 6 IGBT model results

An IGBT model has been described in Chapter 4 and sample results at room temperature and 100 K have been given for all three IGBTs, namely Dynex 600 V PT, Dynex 1700 NPT and Infineon 1700 V IGBT3 devices.

A complete set of results, including on-state characteristics and turn off transients, from room temperature down to 50 K in steps of 25 K will be given for all the three devices. From these results, the selected IGBT model can be further validated.

A 6. 1 On-state characteristics from the IGBT model at low temperatures

The on-state characteristics from the IGBT model for all the three IGBTs are shown in this section. The model results are shown in solid lines and the experimental results are marked with dots. The gate voltage changes from 9 to 15V. Explanations of the results can be found in Chapter 4.
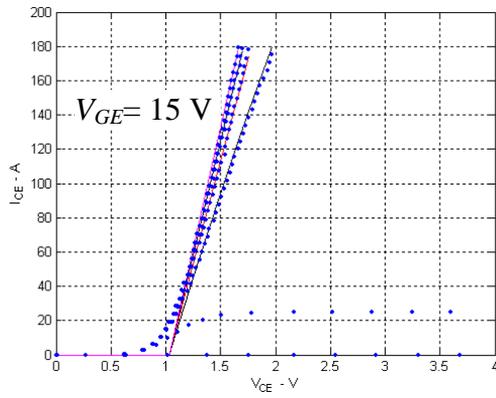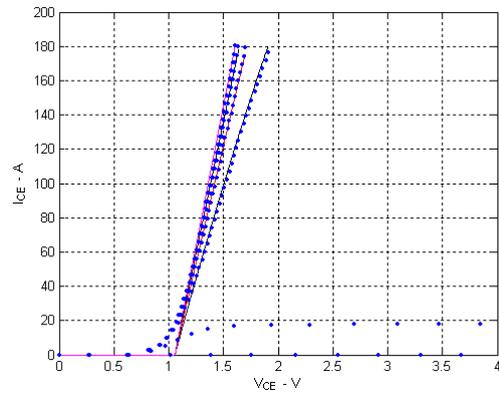
(1) For the Dynex 600 V device

293 K

273 K

250 K

225 K

200 K

175 K

150 K

125 K

100 K

75 K

50 K
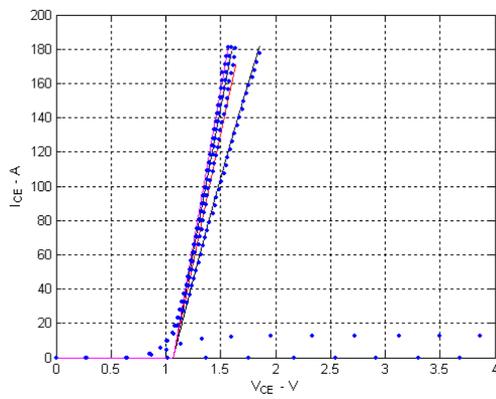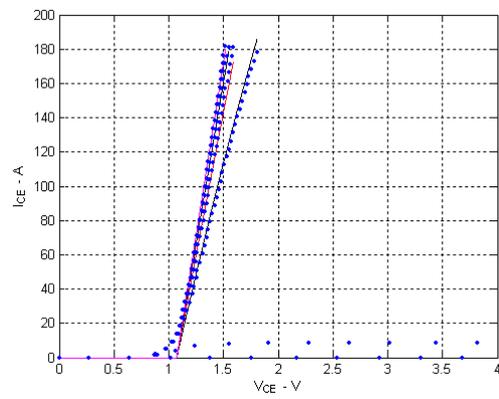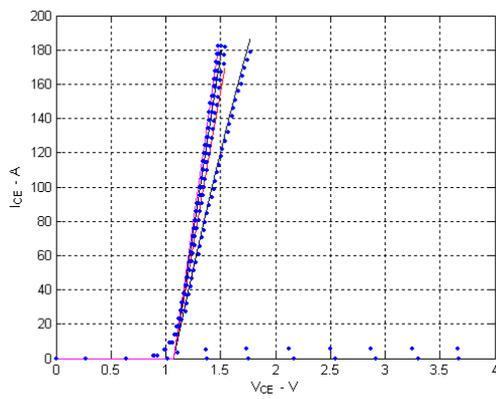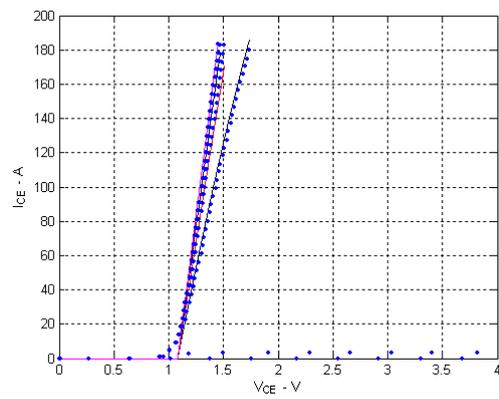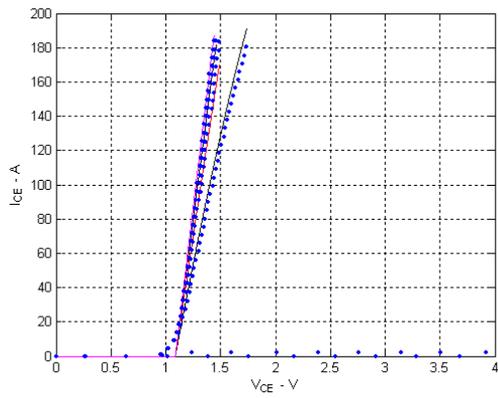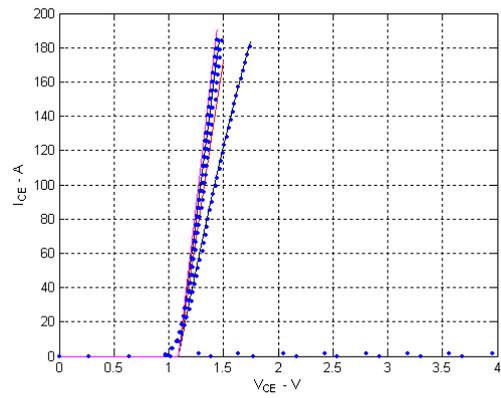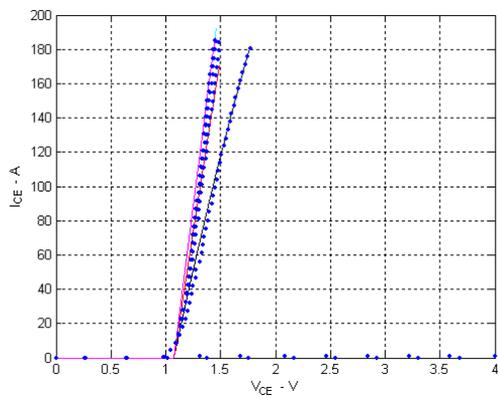
(2) For the Dynex 1700 V device
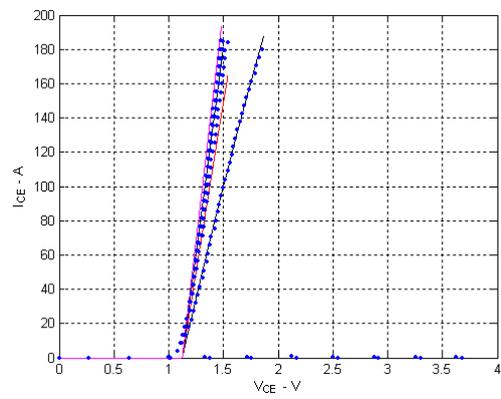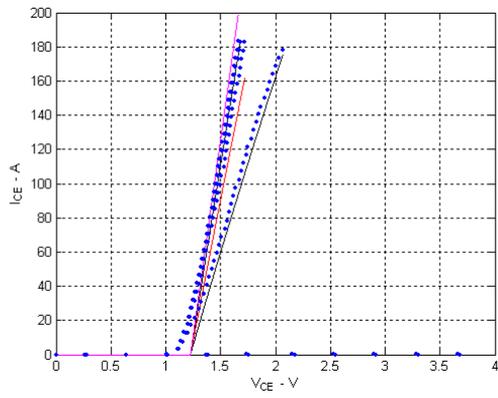
293 K

273 K
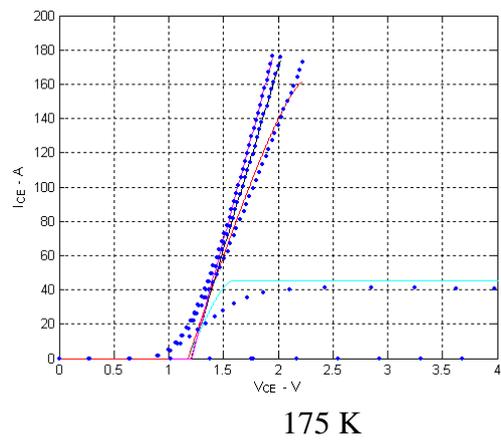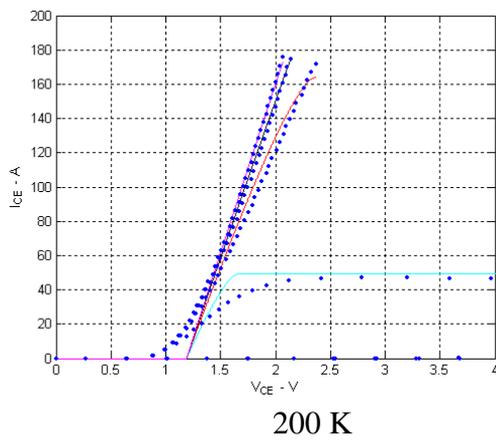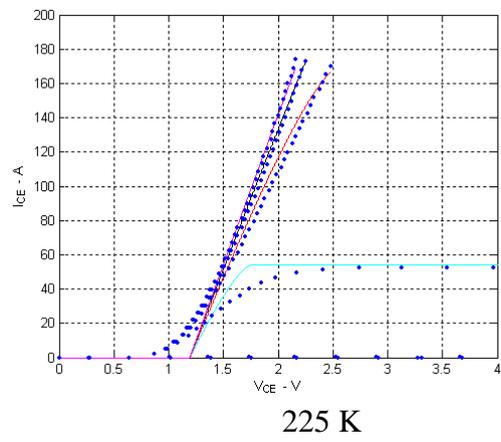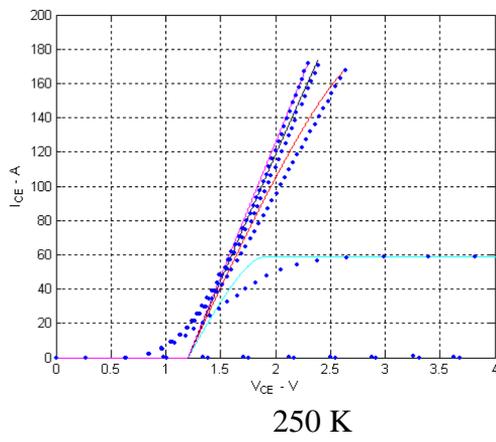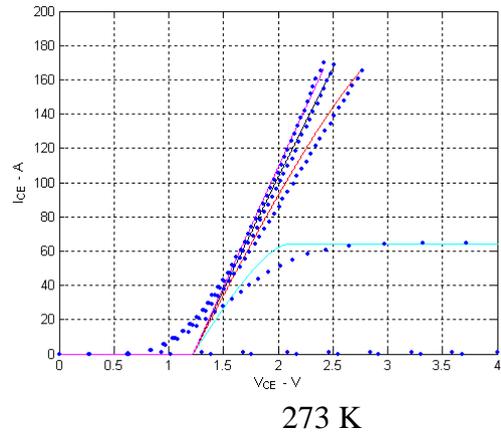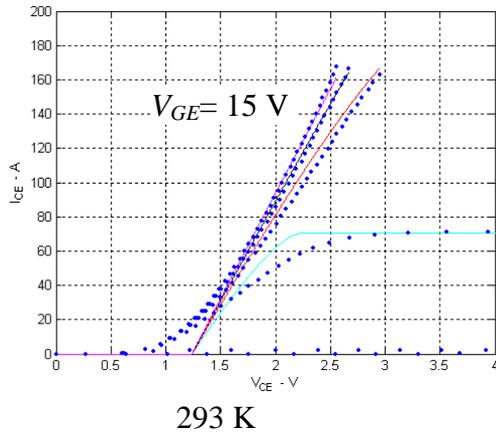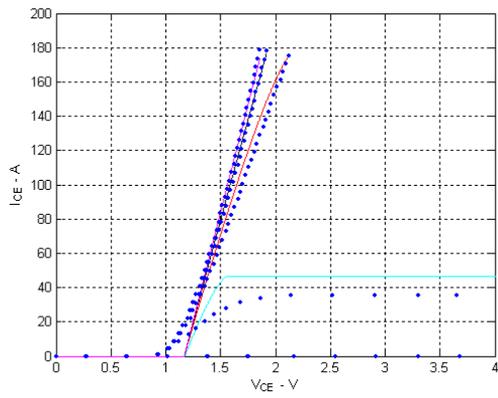
250 K
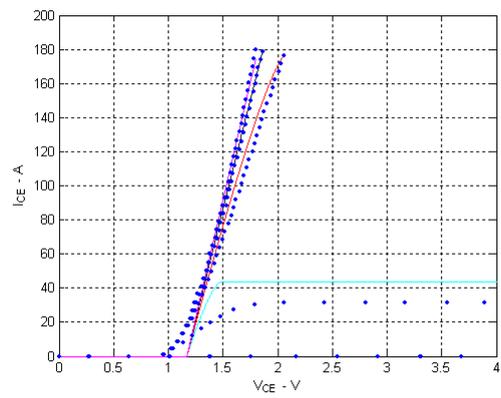
225 K
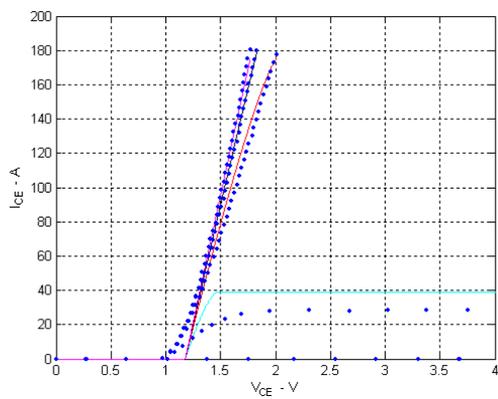
200 K
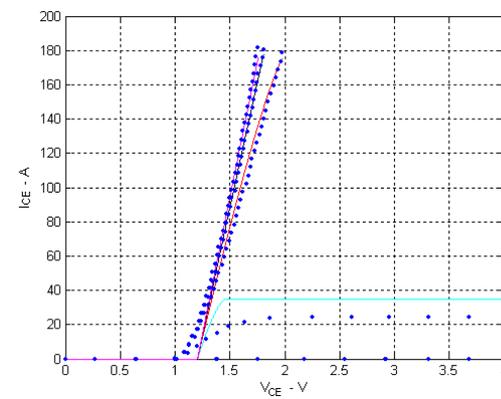
175 K

150 K

125 K

100 K

75 K
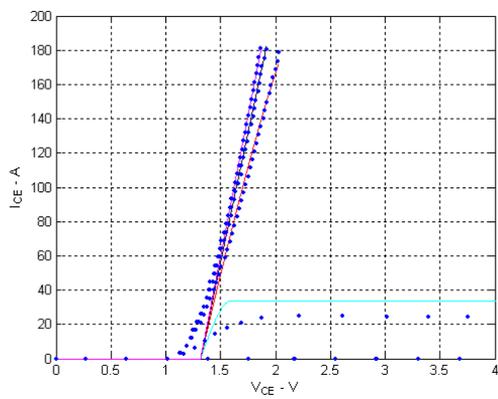
(3) For the Infineon 1700 V device
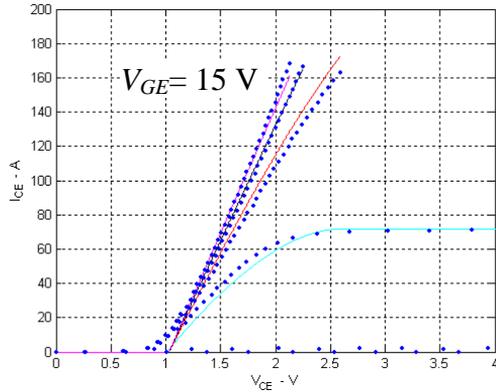
293 K
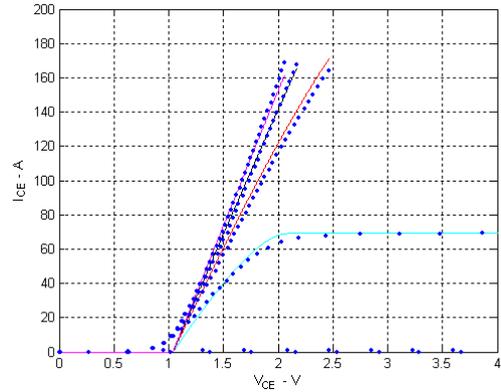
273 K
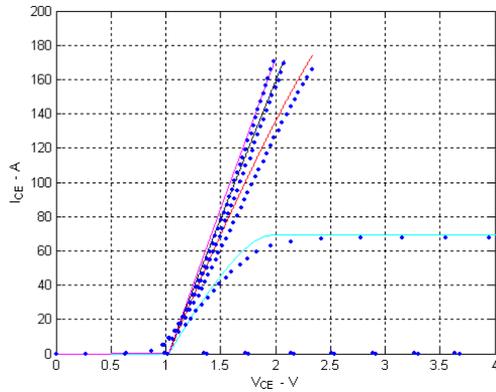
250 K
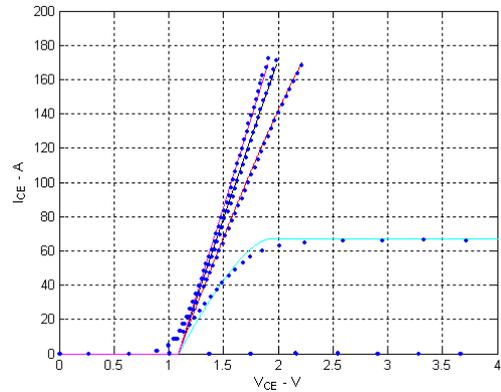
225 K
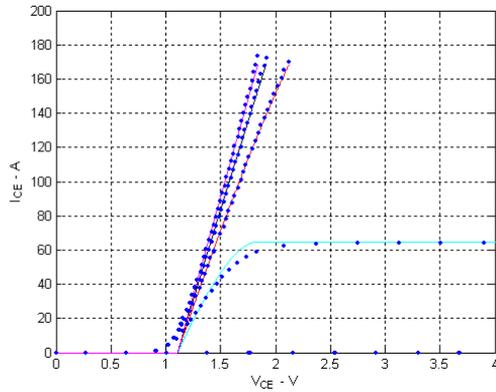
200K
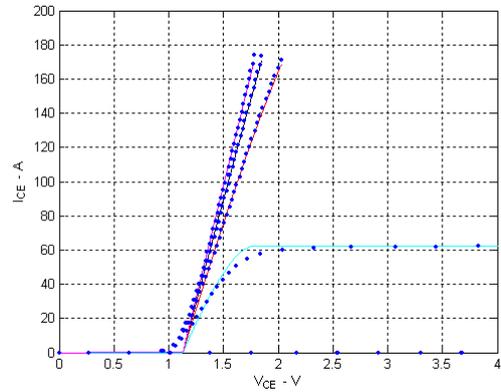
175 K
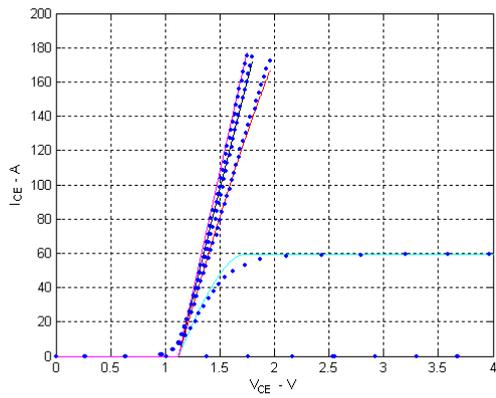
150 K
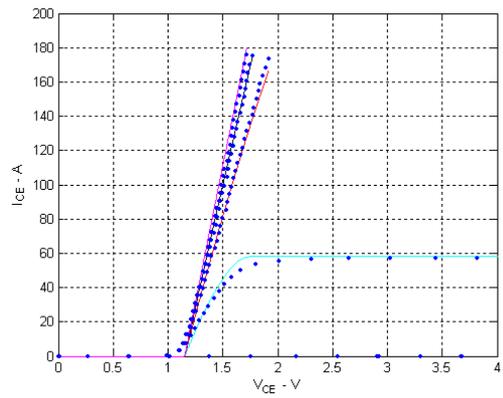
125 K
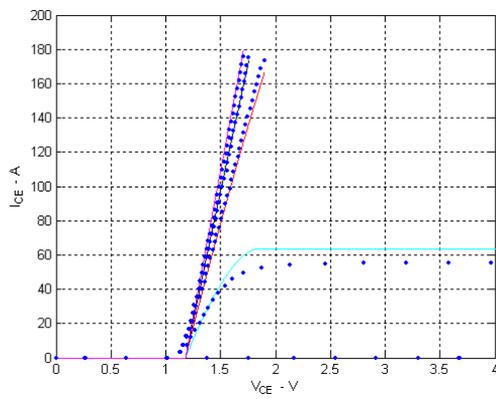
100 K
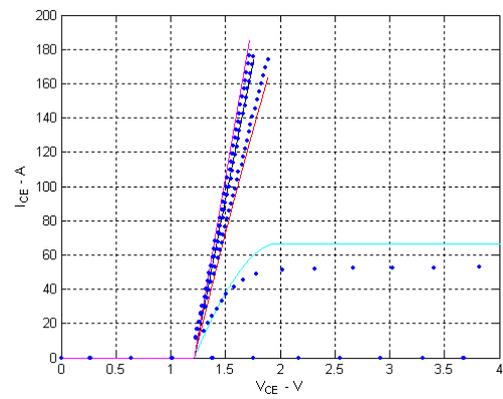
75 K
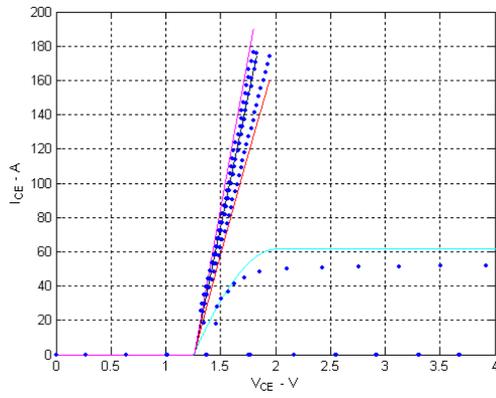
50 K

A 6. 2 Turn off transients from the IGBT model at low temperatures

The turn off transients from the IGBT model for all the three IGBTs are shown in this section. Waveforms are shown for the collector voltage and current from room temperature down to 50 K at the turn off instant. The model results are shown in solid lines and the experimental results are marked with dots. Explanations of the results can be found in Chapter 4.
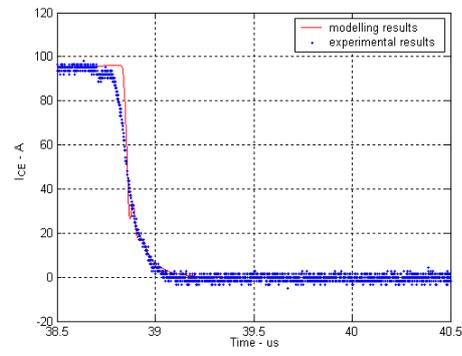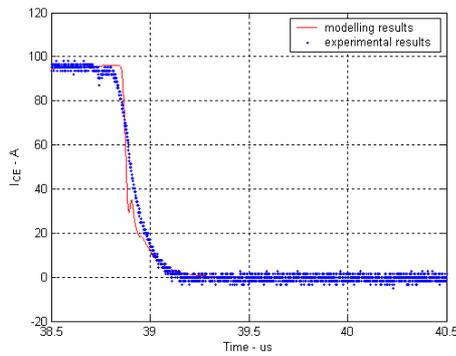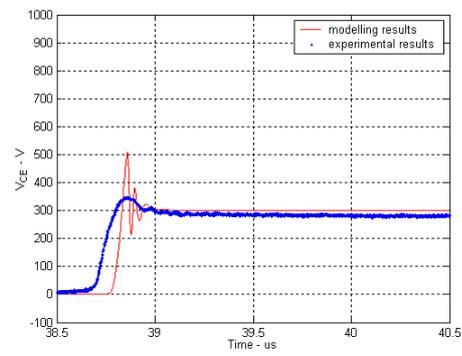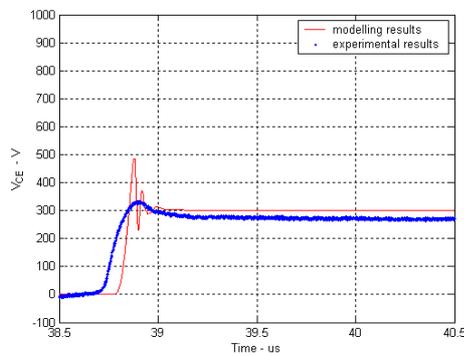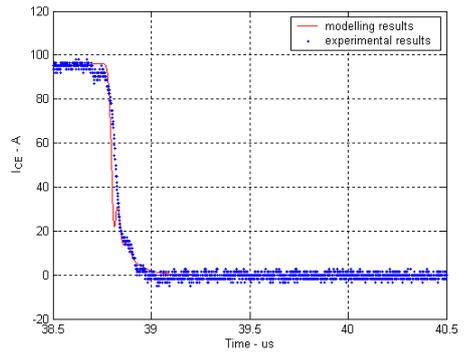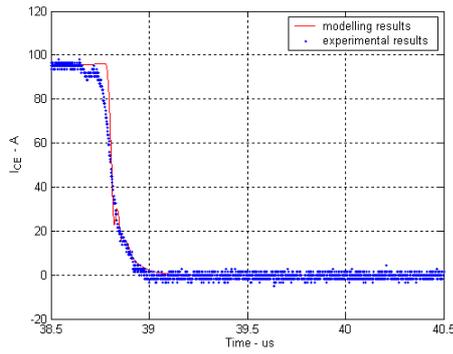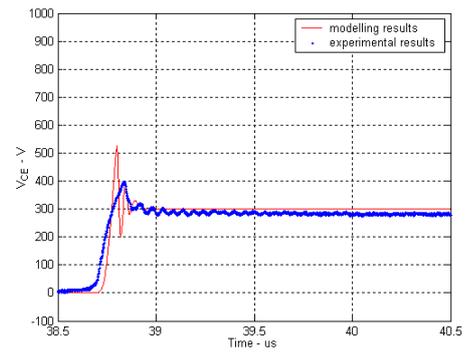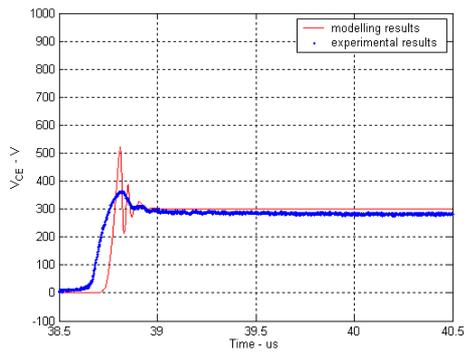
(1) For the Dynex 600 V device

293 K   273 K

250 K

225 K

200 K

175 K

194

150 K

125 K

100 K

75 K

50 K

(2) For the Dynex 1700 V device

293 K

273 K

250 K

225 K

197
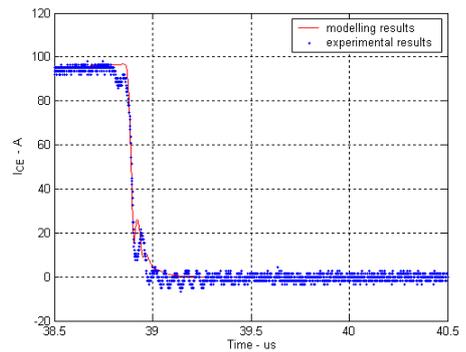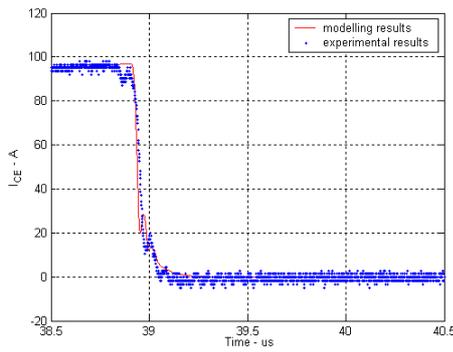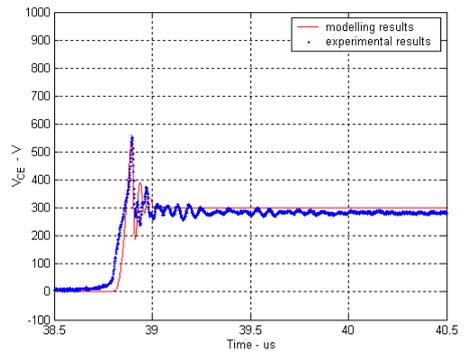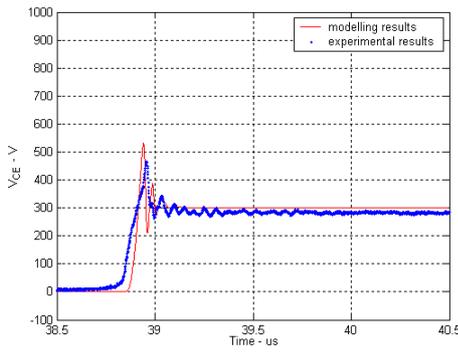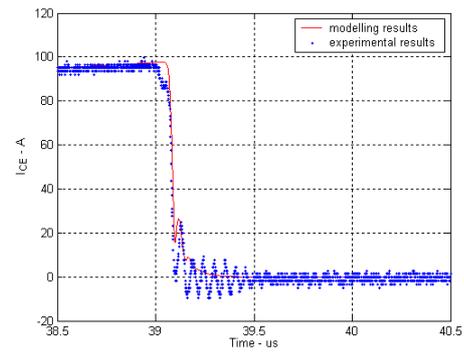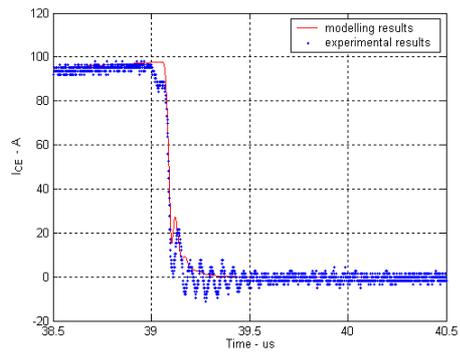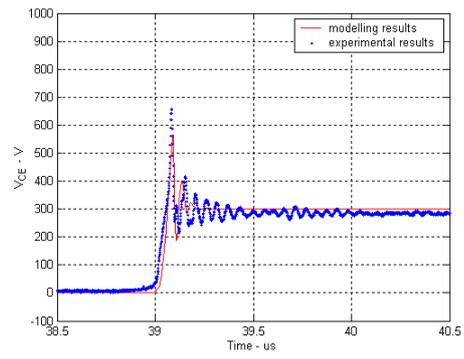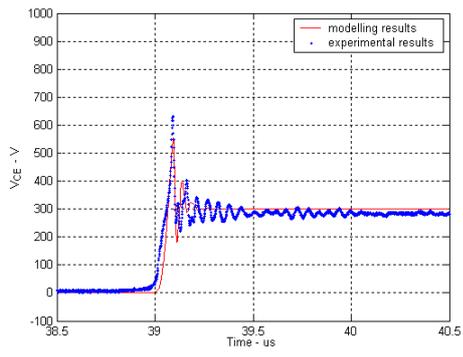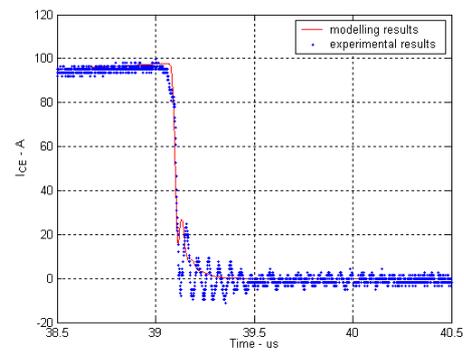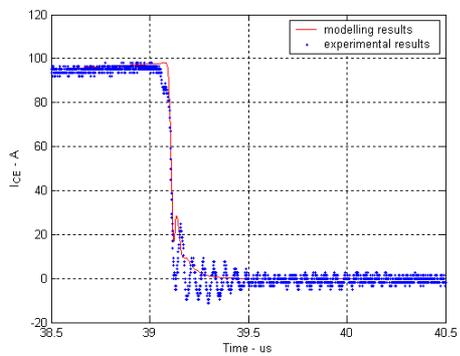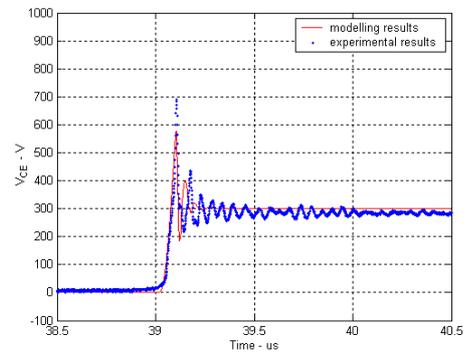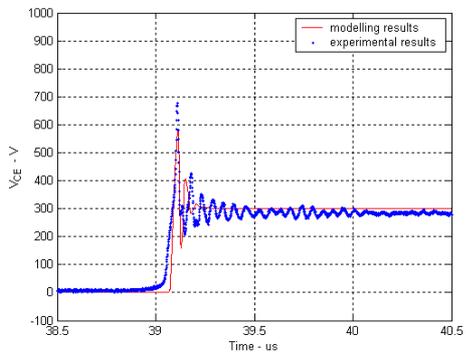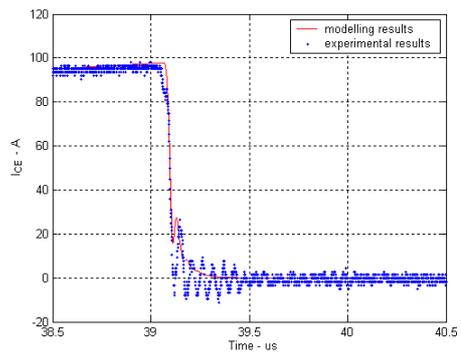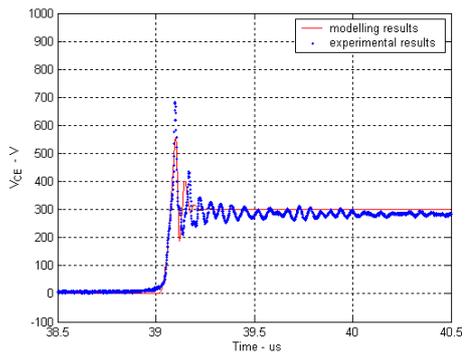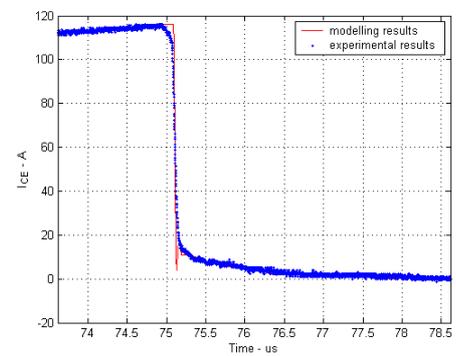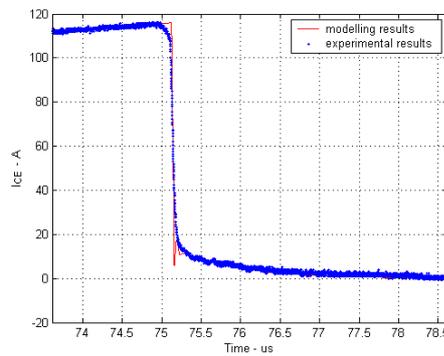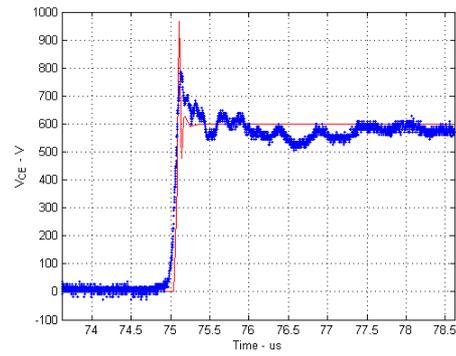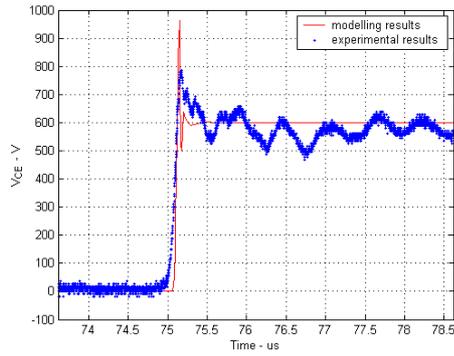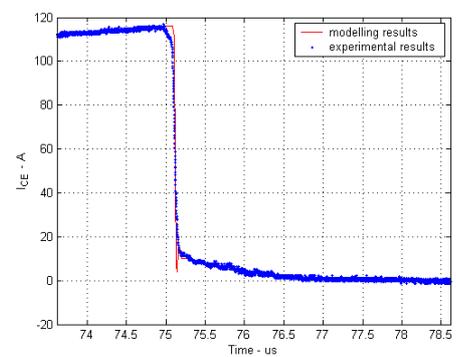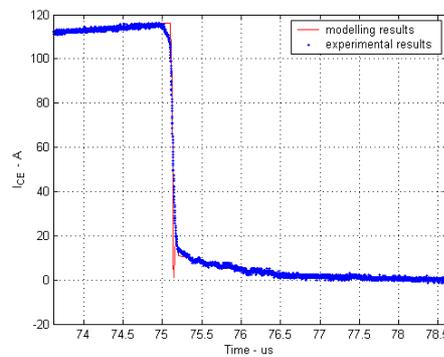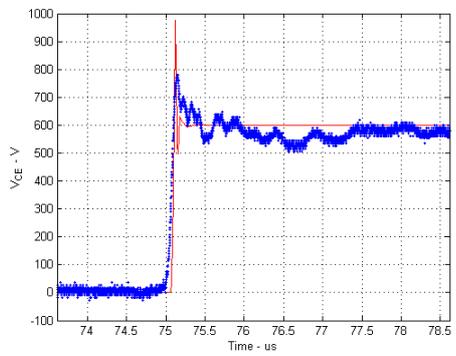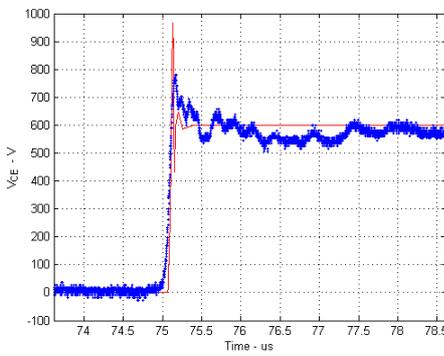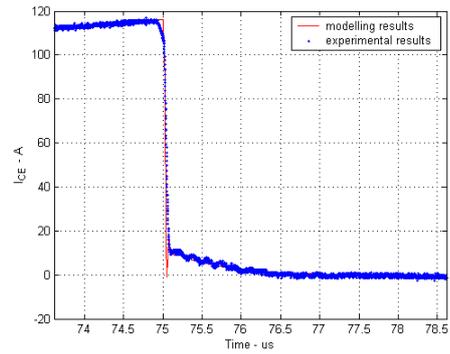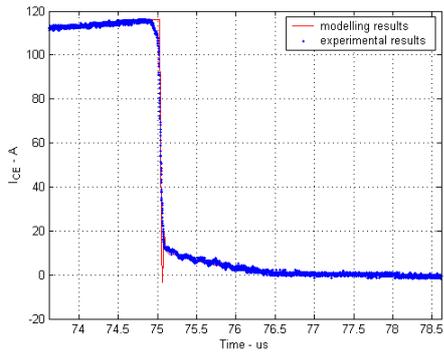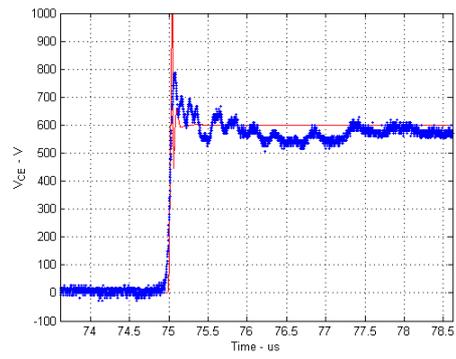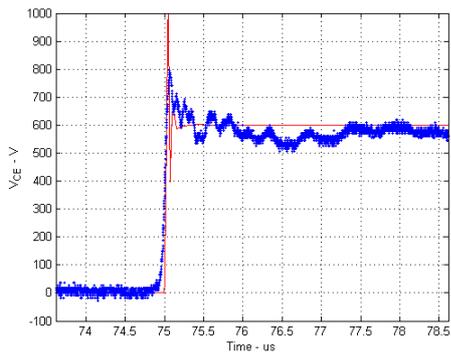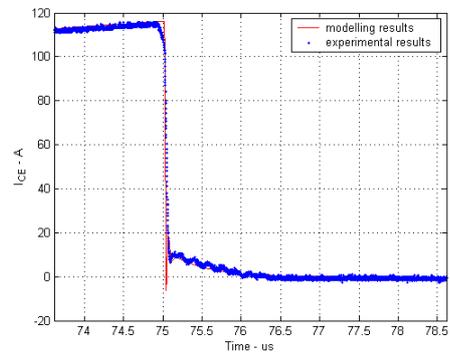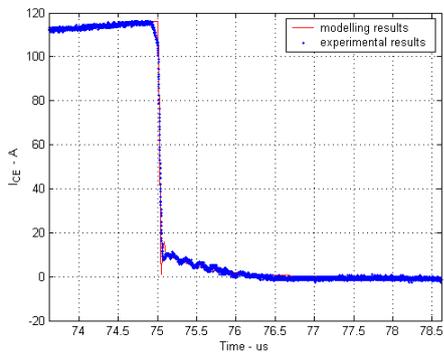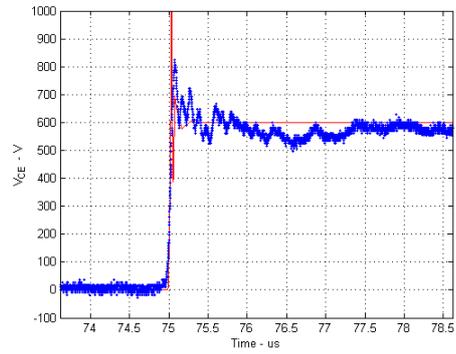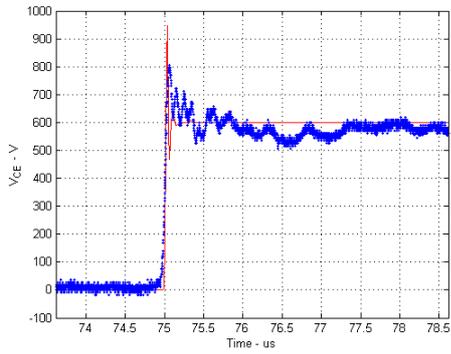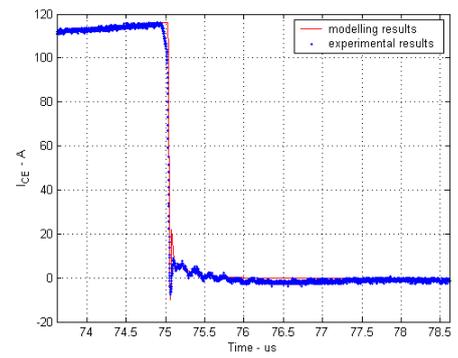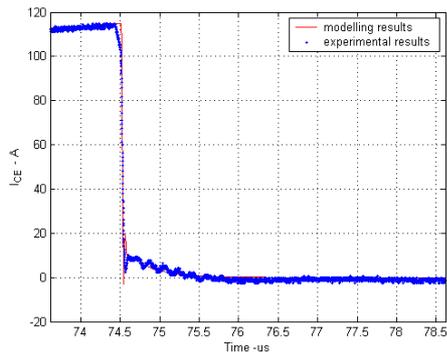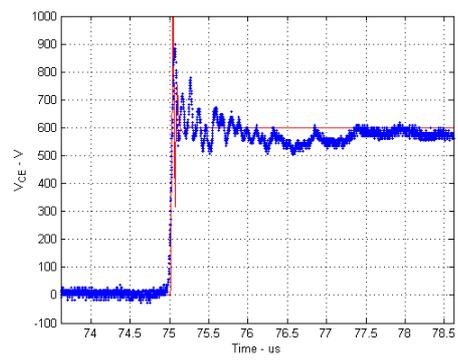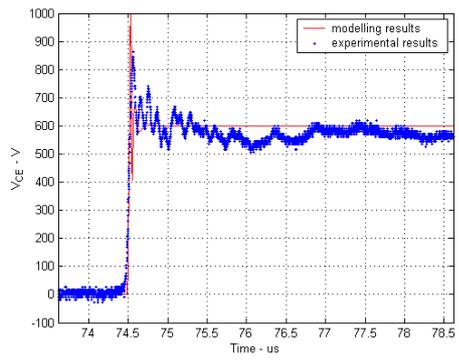
200 K

175 K

150 K

125 K

100 K

75 K

50 K

(3) For the Infineon 1700 V device

293 K

273 K

250 K

225 K

200 K

175 K

150 K

125 K

100 K

75 K

50 K

202