Class E Amplifiers and their Modulation Behaviour

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ABSTRACT

The Class E power amplifier has very high drain efficiency under quasi-static conditions, and is a good candidate for Envelope Elimination and Restoration (EER) or other polar techniques. Unfortunately it has an unusual carrier frequency response, for which no analytic expression was known; this may have limited commercial use of the circuit. Two new steady state analyses are presented, which give the carrier frequency response in simple form, together with expressions for component values. Good agreement with measured data and existing numerical solutions is seen.

Previous attempts at characterising the amplitude modulation (AM) behaviour of this circuit have assumed that it can be modelled as a first order low pass filter. It is shown that Class E AM can be modelled as an equivalent circuit, which behaves as a second order low pass filter. Measurements confirm the analysis.

DEDICATION

This work is dedicated to my parents, Bert and Florrie. It is from them that I received a love of Truth and, by the grace of God, some ability to comprehend certain aspects of it.

ACKNOWLEDGEMENTS

This project would not have been possible without help and support from others. I must start by thanking my supervisor, Dr. Peter Gardner, for his encouragement, wise advice and constructive criticism during the work. He allowed freedom for the research to develop into areas which were quite different from those originally envisaged. The assessor, Dr. Costas Constantinou, provided helpful comments at the formal reporting points of the project. Other members of the Communications Engineering research group contributed in various ways, such as help with equipment and LaTeX text processing software (including the `eethesis` document class, developed by Robert Foster and Greg Reynolds).

There are some special people who did not contribute to the work itself, but supported me during the work. Their friendship, encouragement and prayers helped me when things were difficult, and kept my feet on the ground when things were going well.

Finally I acknowledge, with thanks, financial support provided by the Engineering and Physical Sciences Research Council.

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CHAPTER 1

INTRODUCTION

1.1 Motivation

We seem to be living in an increasingly 'wireless' world[1]. This word was used for many years to describe broadcast amplitude modulated radio but then became regarded as old-fashioned. It now has a new lease of life as a label for personal digital communication. Mass-market wireless terminals (e.g. mobile telephones) have now become fashion items. As a result of this there is great pressure on engineers to hide the technology supporting these everyday objects. Appliances must be small, antennas must be almost invisible, and batteries must have long life between recharging.

There is thus an increased emphasis on high efficiency. High efficiency is desirable in fixed stations because it reduces the power wasted as heat, which reduces costs and increases reliability. High efficiency in mobile equipment brings the possibility of increasing battery life. In any wireless device it is likely that the final radio frequency (RF) power amplifier consumes a significant proportion of the total power, so attention paid to high efficiency there is likely to be worthwhile.

One route to high efficiency is the use of new circuit architectures; the switch-mode circuit known as Class E is considered here. Another technique is to avoid losses in the impedance matching network between the final amplifier and the antenna by eliminating the network altogether. The antenna is engineered to provide the correct impedance so it can couple directly to the active circuit. This may also reduce the total system size.

High efficiency brings with it some new issues. As will be seen below, switch-mode circuits are very non-linear so cannot be used to amplify a modulated signal. Various schemes exist to avoid this problem; these are briefly discussed in Section 1.4. Some of these reintroduce the old

[1]For the sake of clarity, the initial sections do not include references - these appear in subsequent sections.

idea of high-level modulation i.e. the required amplitude of the signal is imposed at the final power amplifier (PA) by varying the drain bias voltage supply. Thus the amplitude modulation (AM) behaviour of the power amplifier becomes important.

1.2 Research Project

1.2.1 Outline of work

The work began by considering the requirements for an efficient transmitter associated with an integrated antenna. Some circuit techniques (e.g. LINC – see Section 1.4 below) require the use of power combiners, but these can be lossy. Up to 50% of the RF power produced can be dissipated in the combiner. This may still be the case if the combiner and antenna are a single structure, with two driving ports. However, this introduces a new complication: the exact power combination may depend on direction, so the required signal might only be generated on boresight. Thus a high efficiency integrated antenna transmitter should avoid power combiners and employ a single port antenna. This requires polar modulation.

A polar modulation system maintains separate paths for the phase and amplitude signals until these are combined in the final power amplifier. In order to ensure correct signal synthesis the time delay in the two paths must be equal. Providing this time equality in the circuit design requires detailed knowledge of the PA response to both phase and amplitude modulation. For example, the baseband frequency response must be known.

It was discovered that there is very little in the literature about the modulation behaviour of Class E. It was decided that this should be the first area to be investigated. As an initial step, the steady-state behaviour was considered in order to arrive at an analytic solution. This was needed because modulation necessarily requires finite Q, but all existing finite-Q treatments used numerical solutions which did not appear to lend themselves to understanding modulation.

The first major item of work was a steady-state power series solution. Circuit parameters were expressed in the form of series in Q^{-1}. Insights into the operation of the Class E circuit gained from this analysis then fed into the second phase. This was the modelling of the drain AM behaviour of Class E via an equivalent circuit.

At this point a simple Class E amplifier was constructed so that measurements could be made, to compare with theoretical predictions. At first some discrepancies were seen, although results were encouraging.

Attention then turned to phase modulation. Measurements were made, and initial attempts

made at a theoretical analysis. It was soon realised that one requirement for this was knowledge of the carrier frequency response. Although the general shape of the response was known from numerical solutions, no general formula was found in the literature. It was decided to attempt at least an approximation, which might be valid at points such as maximum output power or minimum input power. Employing energy conservation seemed a useful path to follow. Rather surprisingly, when combined with existing results from others, this analysis led to a complete carrier frequency response in the form of second-order rational functions in normalised frequency offset.

The energy conservation analysis also clarified the behaviour of the circuit if an 'incorrect' value was used for one of the critical components (the drain shunt capacitance). This allowed a re-examination of the AM frequency response, which reduced the difference between theory and measurements. With the carrier frequency response now known, it was also possible to continue with the analysis of phase modulation but only qualitative agreement with measurement was seen. Further work is needed in this area, but a possible avenue of approach has been identified.

Finally, the AM frequency response analysis was used to predict the intermodulation arising from a polar transmitter. This was compared with measurements, but it was clear that other distortion mechanisms were affecting (sometimes dominating) the results. A clearer understanding of phase modulation will be required before polar modulation can be fully analysed.

Although the original motivation was integrated antenna systems, the integration aspect was not investigated. However, the new theoretical analyses (confirmed by measurement) have made a significant contribution to understanding the modulation behaviour of Class E, and this is needed if successful integrated systems are to be designed.

1.2.2 Structure of thesis

This thesis gives the background to the work, describes the theoretical analyses and practical investigations carried out, and draws conclusions. The major results have been published in peer-reviewed journals; some were presented at a conference [1].

Chapter 1 is the introduction. It gives the motivation for the research, and reviews the published literature. Parts of it are based on an earlier M.Sc. project report [2].

Chapter 2 gives the canonical infinite-Q analysis of the Class E circuit [3]. An understanding of this is a necessary precursor to the later work. The infinite-Q analysis is developed from Chapter 2 of the M.Sc. report, and is based on that given by Raab [4].

Chapter 3 describes two new analyses of the circuit. Both assume steady-state conditions.

The first analysis [5] finds a solution to the differential equations for electric charge, in the form of a power series in Q^{-1}. This gives component values and the frequency response in the vicinity of the design centre frequency. Good agreement with the infinite-Q analytic solution and published numerical results is seen.

The second analysis [6] adopts a different approach. Conservation of energy is used to find the carrier frequency response over a wider bandwidth than the power series solution. This analysis also casts light on the relationship between Class E and the series-tuned Class C circuit often employed in solid-state transmitters.

Chapter 4 considers dynamic behaviour of the Class E power amplifier when undergoing drain amplitude modulation, or phase modulation (PM) via the gate drive signal. It is found that the drain AM response may be modelled via an equivalent circuit [7], which implements a low Q second order low pass filter for baseband frequencies. The investigation of phase modulation was inconclusive, but led to the energy conservation analysis presented in Chapter 4.

Chapter 5 presents measured results from a simple power amplifier. This used a carrier frequency of 2MHz. Measurements include carrier frequency response, AM response and some PM and polar modulation results.

Chapter 6 concludes the main body of the thesis. It contains a summary of findings, and suggestions for further work. Appendices provide information about some of the mathematical techniques used, circuit details, and justification of an approximation and an assertion.

The core original findings of the work are contained in the theoretical analyses of Chapter 3 and the early part of Chapter 4.

1.3 Context

1.3.1 Amplifier classes

Conventional radio frequency power amplifiers operate with the device in active mode in classes A, B or C. Electronics textbooks (for example, [8]) usually describe these in terms of the conduction angle and a trade-off between linearity and efficiency as shown in Table 1.1. In practice, the efficiencies that can be achieved fall short of the theoretical maximum given in the table.

Class A power amplifiers are essentially higher power versions of small signal amplifiers, and are biased within the linear region of the device transfer characteristic – see Figure 1.1. Class B power amplifiers are biased around the cutoff point of the transfer characteristic. It is important to distinguish between audio and RF Class B circuits; or, equivalently, circuits with

Class	Conduction angle	Linearity	Efficiency (maximum)
A	360°	good	50%
B	180°	fair	78%
C	$< 180°$	poor	78-100%

Table 1.1: Active amplifier classes

a load that is independent of frequency or otherwise. Audio Class B requires two devices acting in push-pull so that each takes care of half of the total waveform. An active device usually has a gain transition region at low bias rather than a sharp cutoff. In order to minimise crossover distortion the bias is usually set so that the small signal gain of each device is half the large signal gain of one device. Confusingly, this is sometimes called Class AB operation. Some older books (e.g. [9]) may add a numeric subscript to indicate whether the (thermionic) device draws grid current during signal peaks (1=no, 2=yes). A radio frequency Class B circuit is actually a special case of Class C.

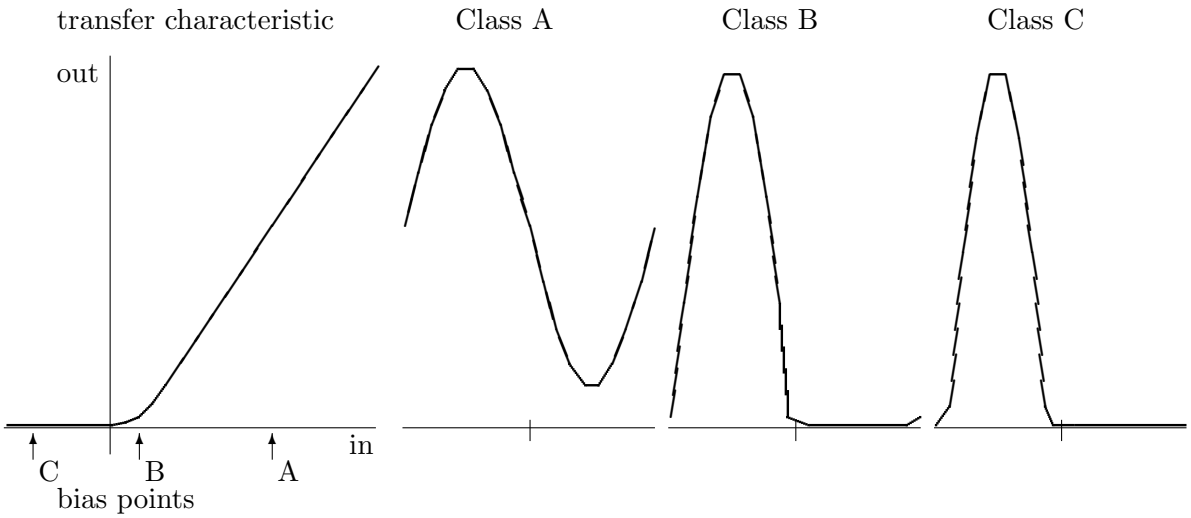

Figure 1.1: Operation of amplifier classes A, B and C

Class C power amplifiers are biased at or below the cutoff point of the transfer characteristic. This means that Class C is unsuitable for audio or other very wideband purposes, as the waveform shape is not preserved; the device current consists of rounded pulses. A parallel tuned circuit in the output restores the missing parts of the sinusoidal wave by what is sometimes called the 'flywheel effect'. Another way of looking at this is that the presented load is resistive at the fundamental frequency and zero at harmonic frequencies. Small conduction angles give an efficiency approaching 100%, but the current pulse becomes very narrow so the device has to

cope with high peak currents which increase resistive losses. A narrow pulse will contain considerable harmonic energy, which will need to be attenuated by output filters thus introducing more losses. For this reason 80% efficiency is about the best that can reasonably be achieved using Class C. In addition, Class C operation may suffer from low stage gain because high input power may be needed in order to support the peak currents in the active device.

Is it possible to do better than Class C? High efficiency requires that all possible inefficiencies are considered and minimised. There are four major loss mechanisms:

overlap If the active device carries simultaneous voltage and current for part or all of the cycle then it will dissipate energy due to normal resistive losses. The solution is to ensure that there is little or no overlap. If possible the device should be used as a switch.

harmonics Any power generated as harmonics is not available at the fundamental frequency, and so is wasted. This can be avoided by keeping waveforms smooth, and by ensuring that harmonic impedances are purely reactive. This typically requires high Q in any tuned circuits.

components No component is perfect. Capacitors suffer dielectric losses. Inductors have resistive losses (made worse by the skin effect), and may have eddy current losses in any core material. These inefficiencies can be minimised by using high quality components, and reducing circulating currents (which requires low Q).

stored energy Some circuits require the discharge of stored energy in capacitors or inductors at some point in the cycle. This usually appears as heat in the active device, and is minimised by careful circuit design.

Class B avoids producing harmonics and does not dissipate significant stored energy, but suffers from considerable overlap. Class C gains its advantage by reducing overlap, but at the expense of generating harmonics.

It is possible to gain higher efficiency by designing on the basis of harmonic impedances rather than conduction angle. There is some inconsistency in the naming of these higher modes of operation; Raab [10] has suggested a useful classification scheme. The reactances seen by the device output at harmonic frequencies are graded according to whether they are higher, lower or similar to the fundamental impedance. It is assumed that only the fundamental impedance contains an appreciable resistive component.

Class C is then the mode in which all the harmonic reactances are very low compared with the fundamental. The device voltage is a sine wave, but the current is a narrow pulse. Using the

letters out of order, Class F has low even-order reactances and high odd-order reactances. The voltage is a square wave, and the current is a half sine wave, so the device does not simultaneously carry voltage and current.

Class D is a push-pull version of Class F, in which each device provides an active even-order termination for the other. However, there is also another Class D used at lower frequencies (such as the audio amplifier in personal stereos); this employs pulse width modulation. Fortunately the context will often make clear which of the two Class D modes is being discussed. Classes G and H appear at low frequencies too [11] and involve modulation of DC supplies.

For each mode there is also an inverse mode. Inverse Class C has high harmonic reactances so the voltage is a narrow pulse but the current is a sine wave. Inverse Class F has high even-order reactances and low odd-order reactances so the voltage is a half sine wave and the current is a square wave.

Class E employs switching, high Q and avoids dissipating stored energy. A full description is given below. In Raab's scheme Class E is characterised as having harmonic reactances which are negative (i.e. capacitive) but similar in magnitude to the fundamental load. There is an Inverse Class E which has inductive reactances. Raab's scheme is summarised in Figure 1.2.

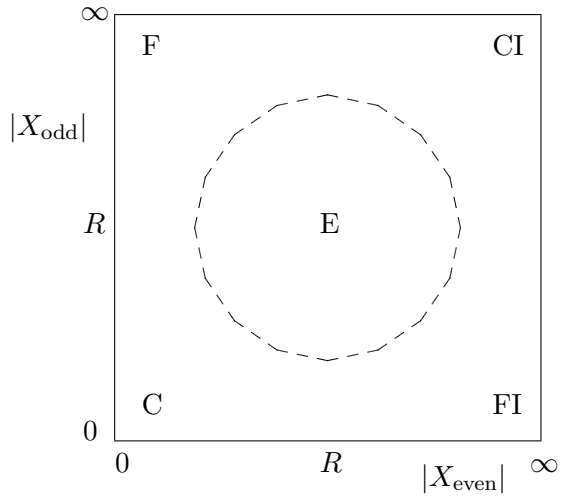

Figure 1.2: Raab amplifier classification scheme (from [10])

1.3.2 Class E

This mode of operation was developed in 1975 [3] by Nathan and Alan Sokal (father and son). It seems to have been little used despite its advantages - perhaps the unusual frequency response

and recently expired patents were a disincentive. It has a theoretical efficiency of 100% even with 180° conduction angle.

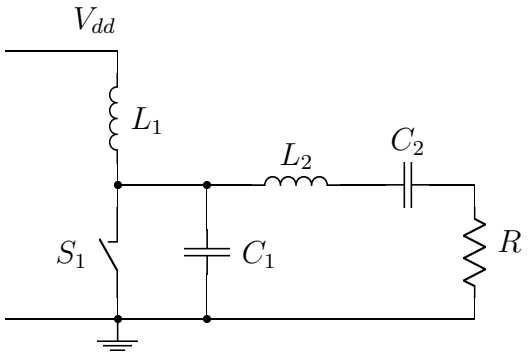

Figure 1.3: Skeleton Class E power amplifier

The circuit (Figure 1.3) has two unusual features. The first is that capacitance (C_1) is deliberately added to the switch, although at higher frequencies most or all of this may be provided by device capacitance. The other is that the output series tuned circuit L_2-C_2 resonates below the operating frequency, so that there is excessive inductive reactance. As a result of this the design centre frequency is a peak in efficiency, rather than power.

When the components have the correct values then the device voltage is not only zero at the point the device turns on but it also has zero slope. This means that no capacitor charge has to be dissipated, and the switch-on can be relatively slow or slightly mistimed without disrupting correct operation.

The paper introducing Class E contained experimental results, but it anticipated a theoretical analysis by Raab [4]. This assumed that the Q of the output circuit is sufficiently high that the only current there is at the fundamental frequency i.e. strictly infinite Q. Raab also assumed that the feed choke L_1 has sufficiently high inductance that it only passes DC. By considering the time domain he was able to find an analytic solution, and confirm the Sokals' measurements. He also showed that for a given device, with limited peak current and voltage capability, the maximum output power obtainable corresponded to a 50% switch duty cycle (i.e. 180° conduction angle). Given a 50% duty cycle, component values and power levels can be calculated. The results of Raab's analysis[2] provide the canonical solution for Class E; they are presented in Table 1.2.

After the initial development of the Class E amplifier, interest turned to investigation of the non-ideal behaviour of real circuits (see Section 1.3.3). Recently there has been much work on

[2]Raab's formula for C_1 (equation 3.25 in his 1977 paper [4], equation 21 in his 2001 paper [10]) omits π from the denominator. His numerical result is correct. His numerical result for peak drain current is 2.84, which is quoted by other authors, but the correct figure is 2.862 as shown in the table.

Parameter	Symbol	Value	Numeric
Shunt capacitive reactance	X_{C1}	$\frac{\pi(\pi^2+4)R}{8}$	$5.4466R$
Excess inductive reactance	$X_{\mathrm{L2\text{-}C2}}$	$\frac{\pi(\pi^2-4)R}{16}$	$1.1525R$
Power	$P_{\mathrm{out}} = P_{\mathrm{in}}$	$\frac{8V_{\mathrm{dd}}^2}{(\pi^2+4)R}$	$\frac{V_{\mathrm{dd}}^2}{1.7337R}$
Peak switch current	I_{pk}	$\left(\frac{\sqrt{\pi^2+4}}{2}+1\right) I_{\mathrm{DC}}$	$2.862I_{\mathrm{DC}}$
Peak switch voltage	V_{pk}	see [4]	$3.56V_{\mathrm{dd}}$

Table 1.2: Canonical Class E solution (after Raab [4])

using Class E amplifiers at microwave frequencies, or modifying the basic circuit.

For example, in [12] the authors compare two different device technologies (GaAs MESFET and InP double heterojunction bipolar transistor) at a frequency of 10GHz. They found similar gain and efficiency, but the MESFET had lower AM–PM so may be more suited to EER techniques (see Section 1.4) than the InP device.

The standard Class E circuit is modified in [13] to allow symmetric operation. This provides cancellation of even harmonics, but at the cost of an increase in odd harmonics. The two halves of the circuit no longer have a resistive load, so the design equations are modified. The authors compared simulations with measured results at 1.2MHz and found good agreement.

1.3.3 Non-ideal behaviour

The standard analysis of Class E assumes that the active device is a perfect switch, the shunt capacitance C_1 is constant and the output circuit Q and supply choke L_1 have very high values. In reality these assumptions are not strictly true, although it turns out that this circuit is surprisingly resilient to parasitic effects.

The effect of relaxing these assumptions is explored below.

Device nonlinear capacitance

At high frequencies a substantial part, possibly all, of C_1 is provided by device internal capacitances arising from semiconductor junctions. The capacitance value varies with the output

voltage in a way that depends on the doping profile of the junction:

$$C_{\mathrm{j}} = \frac{C_{\mathrm{j}\,0}}{(1 + \frac{v}{V_{\mathrm{bi}}})^m} \tag{1.1}$$

where v is the instantaneous voltage, V_{bi} is the junction built-in potential and $C_{\mathrm{j}\,0}$ is the zero-bias capacitance. The exponent m is 0.5 for an abrupt junction or perhaps 0.75 for a hyper-abrupt junction.

Class E with an abrupt junction nonlinear capacitance was analysed by Chudobiak [14] and an analytic solution was found. This work was extended to other junction profiles by Alinikula, Choi and Long [15] but they had to resort to a numerical solution. Their paper implies that a considerable adjustment of the value of the shunt capacitance is required when nonlinearity is taken into account. Their Figure 2 presents the ratio of $C_{\mathrm{j}\,0}$ to the canonical Class E design value C_{d} (which assumes no capacitance change with voltage), and appears to show an adjustment ratio of up to 5. If instead the value of C_{j} at V_{dd} is considered a different picture emerges in which only small adjustment is needed - see Figure 1.4. This plot was produced by reading $C_{\mathrm{j}\,0}$ values off their graph and calculating the corresponding C_{j}; some smoothing has been applied but interpolation errors are inevitable. It can be seen that most of the values lie in the range +5%,-10% from the canonical capacitance. This is likely to be a smaller variation than spreads in device characteristics, and means that Class E design can usually ignore the non-linear nature of the device capacitance. Chan and Toumazou [16] carried out an extension of this work to higher values of m.

A non-linear capacitance requires an adjustment in the value of the excess inductance in the output circuit. Each of the papers cited above contains graphs showing an increase of around 5–15%, depending on the ratio $V_{\mathrm{dd}}/V_{\mathrm{bi}}$ and the doping profile.

As might be expected, a reduction in capacitance with increasing voltage causes a further increase in voltage. The voltage waveform is modified and has a higher peak. Alinikula et al [15] show an increase of the peak voltage from $3.56V_{\mathrm{dd}}$ to around 4.1–$4.8V_{\mathrm{dd}}$.

The current waveforms are not changed by the capacitance non-linearity. Perhaps surprisingly, neither is the power output from a particular supply voltage for a given load resistance. This is because a non-linear capacitance does not introduce a significant loss mechanism so the efficiency remains 100%. The AC to DC current ratio is fixed by the need to remove all charge from the shunt capacitor by the end of the cycle. Given the same AC current then the power output has to be the same for a given resistance.

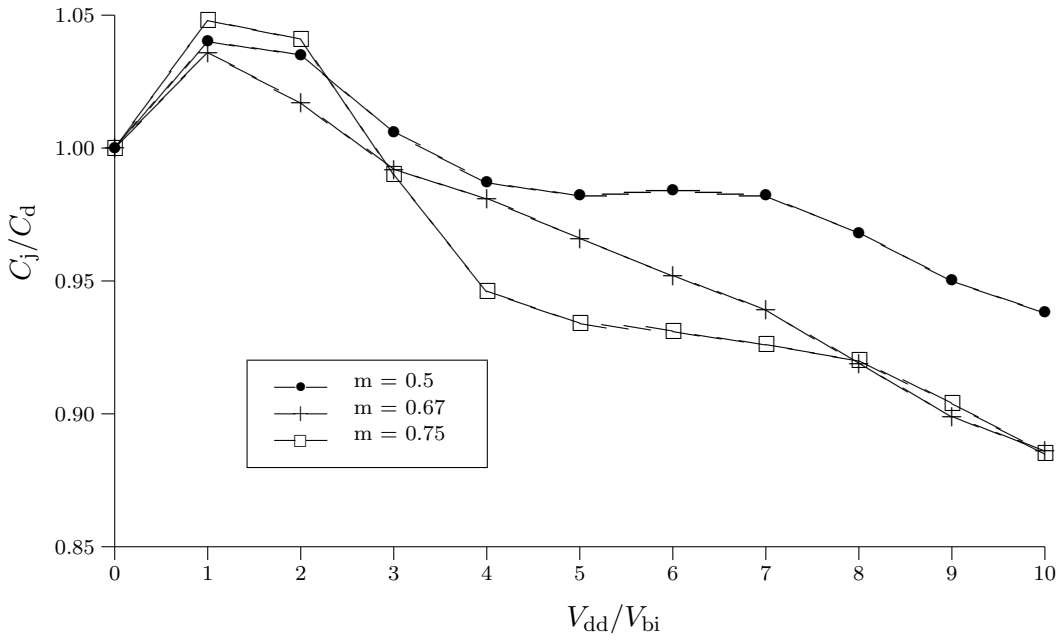

Figure 1.4: Non-linear shunt capacitance adjustment (after [15])

Low inductance, low Q

Various attempts have been made to relax the high-Q, constant-DC assumptions in the canonical analysis. Kazimierczuk and Puczko [17] analysed the Class E circuit for any Q, and at any duty cycle, but still assuming constant DC (i.e. infinite drain choke). They used the Laplace transform method to obtain a set of simultaneous equations; up to this point their analysis has some similarities with that presented in Chapter 3. They found numerical solutions for duty cycles of 25%, 50% and 75%. Their results are presented as graphs and tables, which aids comparison with other work. Good agreement with measured results was seen.

Avratoglou and Voulgaris [18] also assumed constant DC, but at just 50% duty cycle. They solved their equations by using a minimization method, starting from the known Raab solutions. They highlight apparent discrepancies between their results and those obtained by Sokal and Raab. Unfortunately the small scale of their graphs and the absence of tabular results makes further comparison rather difficult. In a later paper [19], with Ioannidou, they considered a lower feed inductance and non-zero switch resistance. Their numerical results were presented as detailed graphs, with some tables for spot values of parameters. They achieved reasonable agreement between measurements and their predictions.

Smith and Zulinski [20] also looked at the low inductance, low Q scenario. They used the Laplace transform, and used matrix algebra in both the s and time domains. They present in an appendix a Matlab subroutine which implements their method. They show predicted and measured switch voltage and current waveforms; good agreement is seen.

Nathan Sokal also found numerical solutions [21] for this scenario. He took account of the effect of finite switch resistance by including a small voltage during the on period; this may be a good approximation for bipolar junction transistors. Unlike all the other authors cited above, he remembered the needs of circuit designers and gave 'best fit' series in Q^{-1} to interpolate between his numerical results. In order to improve the fit for low values of Q he allowed the series to differ slightly from the canonical solution for very high values of Q. Chapter 3 includes a comparison of his numerical results with the new power series solution presented there.

Component tolerance

A good question to ask of any circuit is how it copes with variations in component values or other parameters. Raab investigated this [22] and found that the Class E circuit is "quite tolerant of reasonable circuit variations". A key finding is that under some circumstances the active device voltage and/or current can be negative. This means that a bipolar junction transistor needs to have a diode added to the base or collector circuit in order to support reverse conduction; alternatively an FET can be used as the active device because these support bi-directional current flow.

1.3.4 Carrier frequency response

In addition to considering component variation, Raab [22] also looked at the effect of changing the switching (i.e. carrier) frequency. In two tiny graphs he gave the frequency response of the input and output power, and hence efficiency. These graphs were based on spot solutions to his design equations. They clearly showed that peak efficiency did not coincide with peak output, but the detail of the response was not discernible.

Much later, Cantrell [23] started from Raab's work and obtained equations which could be solved to determine the frequency response. He also gave Spice simulation plots to illustrate his findings. Although already working in the high-Q limit, he failed to spot that in this limit some further approximations could be made which result in simple expressions for frequency response – see Chapter 3. Indeed, he and Davis [24] later bemoaned the fact that "no theoretical equation exists", before presenting an approximation which applies near the centre frequency.

It may be that the known considerable variation in response with frequency, combined with the lack of any simple expression for that response, may have limited the commercial exploitation of the Class E circuit. This difficulty has now been overcome by the energy conservation analysis presented in Chapter 3.

1.4 Modulation

1.4.1 Conventional transmitter architectures

In order to convey information, an RF carrier needs to be modulated. Originally the amplitude was varied, to give either CW (e.g. morse or teleprinter) or AM (e.g. broadcast or aeronautical communications). Then various forms of phase modulation were used, such as FSK (data) or FM (voice). Nowadays it is common to modulate both phase and amplitude (for example, 16-QAM).

Amplitude modulation was originally carried out at the final power amplifier, which could operate in Class C for high efficiency. A Class C PA can also be used to amplify a phase modulated signal. More complex modulation involving amplitude and phase would normally be carried out at a low signal level, after which there would be one or more stages of linear amplification – these would have to use Class A or B.

Amplifier linearity is now a major challenge and research issue. Any departure from perfection carries the risk of degrading the signal and introducing errors, and creating intermodulation interference on adjacent channels. Various techniques have been developed to improve the linearity of an amplifier, or to compensate for remaining nonlinearity, but these are outside the scope of the present study. In general, it is found that improving linearity tends to lead to reduced efficiency. Switching power amplifiers, such as Class E, are very non-linear so cannot be used to amplify a signal which carries amplitude modulation.

1.4.2 High level modulation

An alternative approach is to sidestep the linearity problem by directly generating the required signal at the final power level. This is in some senses a return to the original method used for AM transmitters. Given that the aim is to produce a signal at a given phase and amplitude then there are three basic methods (see the review article [25]):

1. Generate two signals at fixed amplitude, and adjust their phases so that the vector sum is the wanted signal. This is known as LINC[3] or outphasing.

[3]LINC = linear amplification using nonlinear components.

2. Generate two signals at fixed quadrature phase, and adjust their amplitudes and polarity so that the vector sum is the wanted signal. This is the Cartesian method.

3. Generate a single signal with the correct phase and amplitude. This is the polar method, sometimes known as the Kahn technique or EER (envelope elimination and restoration).

These methods are illustrated in Figure 1.5. The first two techniques involve the use of combiner networks, so there is the potential for losses. In particular, the LINC method requires that unwanted power is dumped into a resistance which means that the average efficiency is significantly reduced unless the required amplitude modulation is quite shallow. There is also a fundamental problem with a 3-port combiner: it cannot be simultaneously matched and lossless, so some compromise is needed. Although both methods may be used with a 2-port integrated antenna, there is a risk of incorrect combination off boresight (for example, see [26]) which could lead to spectral regrowth in adjacent channels.

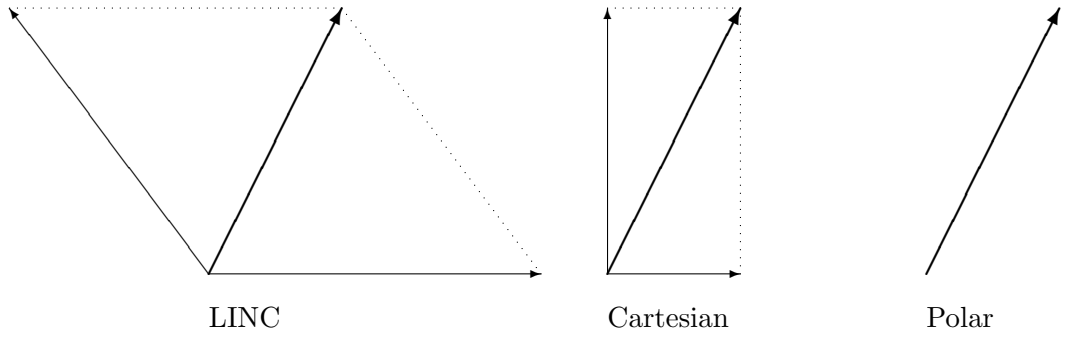

Figure 1.5: High-level modulation methods

The third method, polar modulation, requires no power combining so no new loss mechanisms are introduced. An integrated antenna only needs a single port so there is no problem off boresight. For this reason polar modulation is the method being investigated in the current work. The low-level phase signal may be generated directly by digital processing, or via a Cartesian method from baseband I and Q information. The amplitude is then set by varying the drain bias for the final power amplifier.

1.4.3 Polar modulation and Class E

Under static or quasi-static conditions ideal Class E has perfect modulation characteristics. The output follows the phase of the input gate drive, apart from a frequency-dependent phase shift.

The amplitudes of all currents and voltages in the circuit are proportional to the DC input current or voltage (see analysis in Chapter 2).

Very little work has been done on the dynamic modulation behaviour of Class E. Some measurements or simulations have been made of AM–PM effects (for example, see [27, 28, 29]) due to the device non-linear capacitance. Surprisingly, almost nothing was known about the modulation behaviour of the ideal Class E circuit, so in measuring real circuits one does not know from what ideal case they are deviating.

Kazimierczuk [30] considered AM but made two simplifying assumptions, neither of which are really true. He assumed that the collector/drain voltage waveform could be considered to be generated by a zero impedance voltage source, and then proceeded to calculate the carrier and sideband currents in the off-tune output circuit. In reality, the drain voltage is critically dependent on the surrounding impedances so is anything but a voltage source. He also assumed that the two low-pass filters formed by the feed choke and the finite output circuit Q do not interact. His measurements were consistent with his model, but did not probe the limits of the model so were almost bound to agree.

Polar modulation is very sensitive to the details of the modulation behaviour of the chosen PA circuit. This is illustrated in Figure 1.6, for the case of double-sideband suppressed-carrier modulation. Conventional modulation simply varies the carrier amplitude (including negative values), while keeping the phase constant. The result is of course simply two sidebands, arising from the sum and difference frequencies from the mixing action in the PA.

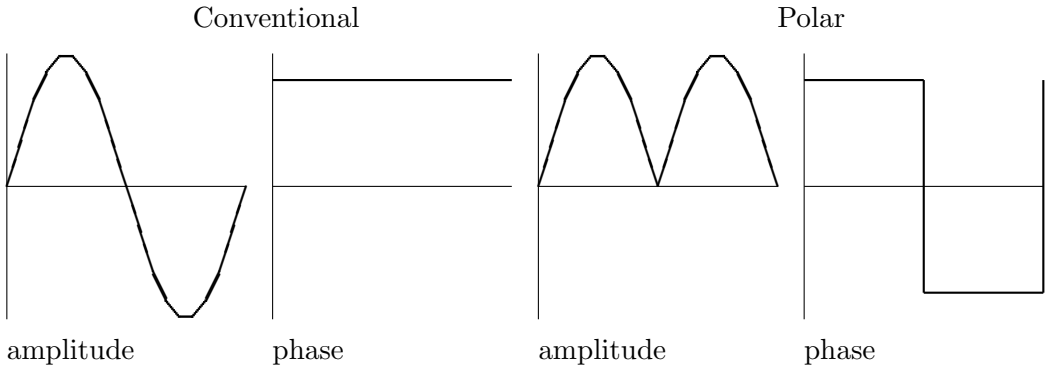

Figure 1.6: Conventional vs. polar modulation

It can be seen that in the case of polar modulation both the amplitude and phase signals have much wider bandwidth than the original baseband signal; in fact an infinite series of harmonics. When combined together in a PA with infinite bandwidth all the unwanted products cancel

out, leaving just the wanted sidebands. In reality, even a near-ideal PA will have a limited bandwidth. Although the higher products will be attenuated, they will also be shifted in phase so cancellation is no longer complete.

This process was investigated by Raab [31]. He considered the results from multiplying together the Fourier series arising from the amplitude and phase channel modulations i.e. full wave rectification and square wave respectively (as shown in Figure 1.6). The finite bandwidth of the modulator was modelled by simply truncating the series for the amplitude signal. With such a gross approximation it is not surprising that only limited agreement was seen between theory and measurement. He also considered time delays.

Raab's work was extended by Milosevic, van der Tang and van Roermund [32], specifically for a Class E PA. They assumed that a Class E circuit has infinite phase bandwidth, and acts as a single pole LP filter for amplitude. These assumptions are reasonably valid for an amplifier with low Q output, and a fairly high drain feed choke value. They obtained expressions for the sideband components in the form of infinite series. As higher order terms are quite small, a sum of the earlier terms provides a good estimate of the ratio of the wanted sideband power vs. the unwanted intermodulation sidebands.

They compared their theoretical result with a simulation of an ideal Class E PA. Agreement was quite good, with the simulation showing slightly better intermodulation. It was suggested that this was because the finite Q of the output circuit was suppressing unwanted sidebands. This is probably correct, given that their theoretical analysis failed to take account of the finite phase bandwidth of the output circuit. The resultant time delay would partly compensate for the lack of time equalisation for the two modulation paths in their study.

It is clear that understanding polar modulation requires a knowledge of the details of the operation of the final power amplifier during amplitude and phase modulation; simple approximations may not be sufficient. However, as a precursor to this it is necessary to establish a good model for steady-state behaviour – this is the subject of the next two chapters.

CHAPTER 2

CLASS E CANONICAL ANALYSIS

2.1 Canonical Analysis

2.1.1 Outline of method

Time domain analysis of Class E operation suffers from the problem that the current and voltage waveforms are inter-dependent so it is not possible simply to specify one and then calculate the other. Analysis proceeds by assuming that the DC feed inductor has sufficiently high reactance that the supply current is constant ('infinite feed choke' assumption), and the output network has sufficiently high reactance at harmonic frequencies that the output current is sinusoidal at the fundamental frequency ('infinite Q' assumption). Then the total current through the switch/shunt capacitor is just the sum (or difference) of these. When the device is on this is the device current and the device voltage is zero. When the device is off this current charges the shunt capacitor, so integrating the current gives the voltage. It will be assumed that the switch is an FET, but other devices can be used.

The requirement for zero volts and zero slope at turn-on (i.e. Class E condition) fixes the ratio between the DC and AC currents and the offset angle for the switching action. The shunt capacitor value is determined by requiring that the average drain voltage be equal to the supply voltage. Finally, the fundamental Fourier components of the drain voltage are calculated and these set the resistive load and excess inductance in the output circuit. Class E waveforms are shown in Figure 2.1; they are normalised to 1V/1A/1W DC supply, with timing based on the switch. It can be seen that the device current and voltage are never simultaneously non-zero (i.e. no overlap), so it dissipates no energy.

The analysis shown here is based on that given by Raab [4], but for the sake of clarity it assumes from the outset a 50% switch duty cycle and operation at the design centre frequency.

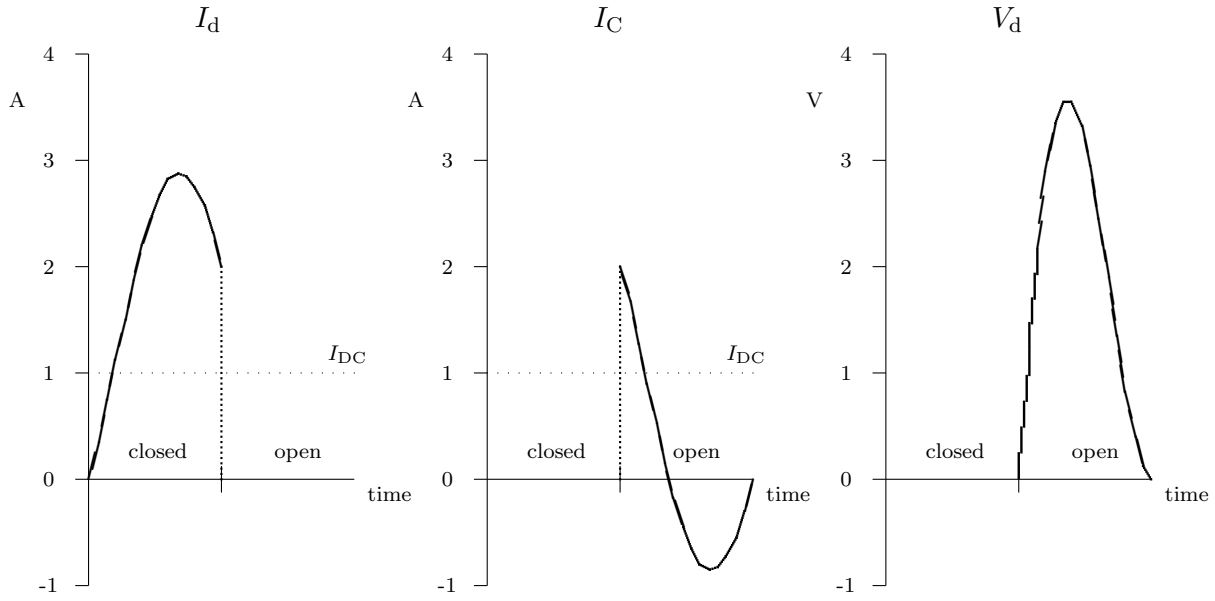

Figure 2.1: Ideal Class E waveforms: drain and capacitor currents, drain voltage

The presentation is developed from that given in an earlier report [2] by the current author.

2.1.2 Current ratio

The analysis starts by considering the DC and AC currents (Figure 2.2). The AC current has a fundamental component only, because of the output series tuned circuit. The total current which flows either in the active device or the shunt capacitor is

$$I = I_{\rm DC} - I_{\rm AC} \sin\theta \tag{2.1}$$

where $\theta = \omega t$.

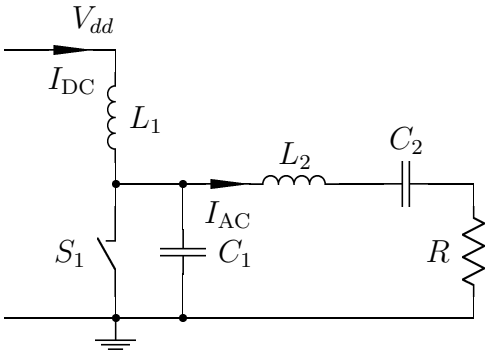

Figure 2.2: Skeleton Class E power amplifier, showing currents

This current charges the shunt capacitor C_1 during the time that the active device is switched off. The Class E condition that the drain/collector voltage be zero, with zero slope, at the point

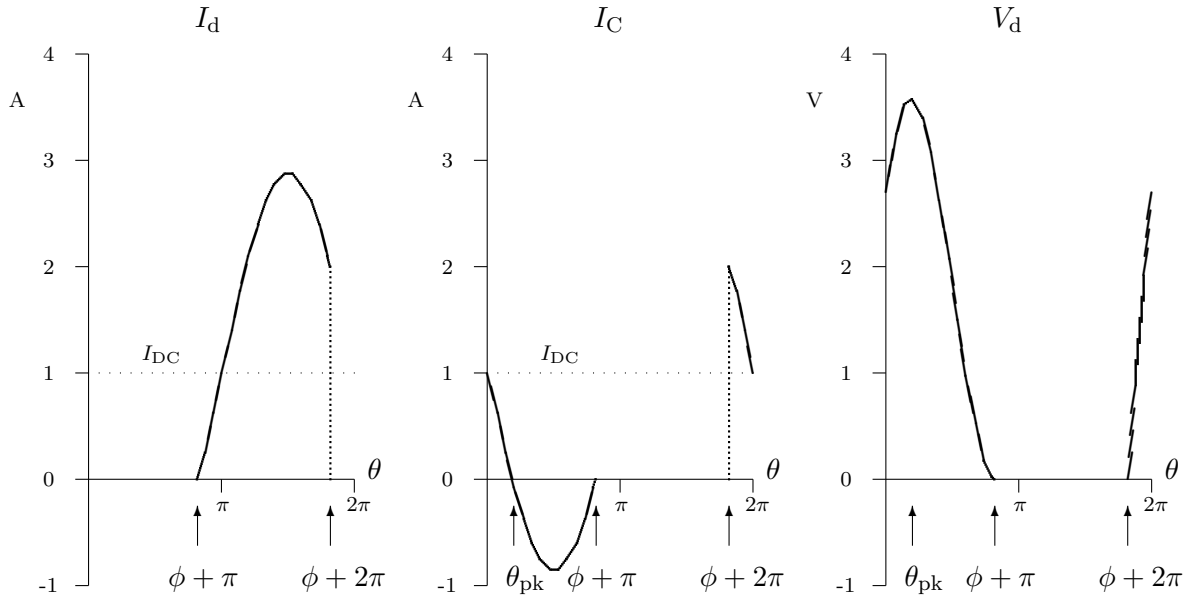

Figure 2.3: Ideal Class E waveforms, relative to AC phase

the device turns on again is equivalent to requiring that the current is zero and the total charge deposited is zero too. This condition is independent of any capacitor non-linearity. All that is necessary is that the capacitor voltage be a monotonic function of charge, starting from zero. If a conduction angle of π is assumed and the point in the cycle where the device switches off is ϕ (Figure 2.3), then the zero current requirement is

$$I_{\rm DC} - I_{\rm AC} \sin(\phi + \pi) = 0 \tag{2.2}$$

so

$$I_{\rm DC} + I_{\rm AC} \sin\phi = 0 \tag{2.3}$$

The zero charge requirement is

$$\int_{\phi}^{\phi+\pi} (I_{\rm DC} - I_{\rm AC} \sin\theta)\, {\rm d}\theta = 0 \tag{2.4}$$

so

$$\pi I_{\rm DC} - 2 I_{\rm AC} \cos\phi = 0 \tag{2.5}$$

Substituting this into (2.3) gives

$$\tan\phi = \frac{-2}{\pi} \tag{2.6}$$

Trigonometry can be used to find

$$\sin\phi = \frac{-2}{\sqrt{\pi^2 + 4}},\ \cos\phi = \frac{\pi}{\sqrt{\pi^2 + 4}} \tag{2.7}$$

and ϕ is usually regarded as a small negative angle (-32.48°). Then using (2.3) gives

$$I_{\mathrm{AC}} = \frac{\sqrt{\pi^2+4}}{2} I_{\mathrm{DC}} = 1.862\, I_{\mathrm{DC}} \tag{2.8}$$

so the peak drain current is $I_{\mathrm{pk}} = 2.862\, I_{\mathrm{DC}}$. The output power is

$$P_{\mathrm{out}} = \frac{1}{2} I_{\mathrm{AC}}^2 R = \frac{\pi^2+4}{8} I_{\mathrm{DC}}^2 R \tag{2.9}$$

2.1.3 Drain voltage

The drain voltage is found by integrating the shunt capacitor current. It will now be assumed that the capacitor is linear i.e. it is constant with respect to voltage. The supply current will remain constant provided that the supply voltage is equal to the average drain voltage. This gives a relationship between V_{dd} and the value of C_1. The peak drain voltage can then be found.

The drain voltage is given by

$$V_{\mathrm{d}}(\theta) = \begin{cases} \frac{1}{2\pi f C_1} \int_{\phi}^{\theta} (I_{\mathrm{DC}} - I_{\mathrm{AC}} \sin x)\, \mathrm{d}x & \text{switch open i.e. } \phi \le \theta \le \phi + \pi \\ 0 & \text{switch closed i.e. } \phi + \pi < \theta < \phi + 2\pi \end{cases} \tag{2.10}$$

Performing the integration, and substituting (2.8) gives (for the 'switch open' period)

$$V_{\mathrm{d}}(\theta) = \frac{I_{\mathrm{DC}}}{2\pi f C_1} \left[\theta - \phi + \frac{\sqrt{\pi^2+4}}{2} (\cos\theta - \cos\phi) \right] \tag{2.11}$$

The DC component (i.e. the mean value) of the drain voltage can now be set equal to the supply voltage:

$$V_{\mathrm{dd}} = \frac{I_{\mathrm{DC}}}{(2\pi)^2 f C_1} \int_{\phi}^{\phi+\pi} \theta - \phi + \frac{\sqrt{\pi^2+4}}{2} (\cos\theta - \cos\phi)\, \mathrm{d}\theta \tag{2.12}$$

Integrating, and using trigonometric function values from (2.7), gives

$$V_{\mathrm{dd}} = \frac{I_{\mathrm{DC}}}{2\pi^2 f C_1} \tag{2.13}$$

Thus

$$\frac{1}{2\pi f C_1} = \frac{\pi V_{\mathrm{dd}}}{I_{\mathrm{DC}}} = \pi R_{\mathrm{DC}} \tag{2.14}$$

where R_{DC} is the resistance seen by the DC power supply.

The peak drain voltage is found by evaluating the drain voltage at the point θ_{pk} where the capacitor current is zero and going negative. Zero current occurs when $\sin\theta_{\mathrm{pk}} = \sin(\phi+\pi)$ (2.2), and by considering the symmetry of the sine function it can be seen that $\theta_{\mathrm{pk}} = -\phi$. Substituting this into (2.11) for V_{d} and using (2.6) and (2.13) gives

$$V_{\mathrm{d\ pk}} = -2\pi\phi\, V_{\mathrm{dd}} = 3.562\, V_{\mathrm{dd}} \tag{2.15}$$

2.1.4 Load network

Finally, the required values for the load network may be found by calculating the in-phase and quadrature Fourier components of the drain voltage at the fundamental frequency. The in-phase component determines the load resistance R, and the quadrature component fixes the net inductance presented by the output series circuit L_2-C_2.

$$V_{\text{AC-i}} = \frac{1}{\pi}\int_0^{2\pi} V_{\text{d}} \sin\theta \,\mathrm{d}\theta,\ V_{\text{AC-q}} = \frac{1}{\pi}\int_0^{2\pi} V_{\text{d}} \cos\theta \,\mathrm{d}\theta \tag{2.16}$$

Using (2.11) and (2.13) gives

$$V_{\text{AC-i}} = V_{\text{dd}} \int_{\phi}^{\phi+\pi} \theta \sin\theta + \frac{\sqrt{\pi^2+4}}{2}\cos\theta\sin\theta - \left(\phi + \frac{\sqrt{\pi^2+4}}{2}\cos\phi\right)\sin\theta \,\mathrm{d}\theta \tag{2.17}$$

The first and second terms can be handled by using integration by parts and a trigonometric identity respectively; the third term is trivial. Then

$$V_{\text{AC-i}} = V_{\text{dd}} \left[\sin\theta - \theta\cos\theta - \frac{\sqrt{\pi^2+4}}{8}\cos 2\theta + \left(\phi + \frac{\sqrt{\pi^2+4}}{2}\cos\phi\right)\cos\theta\right]_{\phi}^{\phi+\pi} \tag{2.18}$$

Substituting trigonometric functions using (2.7) causes most of the terms to cancel, leaving

$$V_{\text{AC-i}} = V_{\text{dd}} \frac{4}{\sqrt{\pi^2+4}} \tag{2.19}$$

Multiplying by (2.8) (and remembering that the AC values are peak, not RMS) gives

$$P_{\text{out}} = \frac{1}{2} V_{\text{AC-i}} I_{\text{AC}} = V_{\text{dd}} I_{\text{DC}} = P_{\text{in}} \tag{2.20}$$

which confirms a drain efficiency of 100%. Dividing (2.19) by (2.8) gives the load resistance:

$$R = \frac{V_{\text{AC-i}}}{I_{\text{AC}}} = \frac{8V_{\text{dd}}}{(\pi^2+4)I_{\text{DC}}} = \frac{8R_{\text{DC}}}{(\pi^2+4)} = \frac{R_{\text{DC}}}{1.7337} \tag{2.21}$$

Performing a similar calculation for the quadrature component yields

$$V_{\text{AC-q}} = V_{\text{dd}} \frac{\pi(\pi^2-4)}{4\sqrt{\pi^2+4}} = V_{\text{AC-i}} \frac{\pi(\pi^2-4)}{16} = 1.152\, V_{\text{AC-i}} \tag{2.22}$$

So the magnitude of the excess inductance presented by the output circuit must be equal to $1.152\,R$.

This completes the canonical analysis.

2.2 Circuit Design

2.2.1 Design procedure

When designing a Class E power amplifier, one will often be given the required load impedance, power level and DC supply voltage. These are related via (2.21), so there is not a free choice. It will be necessary either to carry out an impedance transformation of the load so that R_{DC} is correct for the required power and supply voltage, or modify the supply voltage so that the correct power is available in the given load. If an impedance transformation is used then it is the transformed load value which is used in the Class E calculations.

Having determined R_{DC}, (2.14) can be used to find C_1. Alternatively, (2.14) and (2.21) can be combined to give $X_{\mathrm{C1}} = 5.4466\,R$. Applying (2.22) gives the excess inductive reactance in the output circuit L_2-C_2. If L_2 is determined by the chosen circuit Q ($X_{\mathrm{L2}} = QR$), then C_2 has a smaller reactance to give the correct excess inductance i.e. $X_{\mathrm{C2}} = (Q - 1.152)R$.

2.2.2 Example

A Class E power amplifier is to be designed for a frequency of 2MHz, and load resistance R of 60Ω (see Chapter 5). The supply voltage is 6V, and the output circuit Q should be 13.

The design proceeds thus:

$$R_{\mathrm{DC}} = 1.7337\,R = 104\,\Omega$$

$$X_{\mathrm{C1}} = 5.4466\,R = 327\,\Omega \text{ so } C_1 = 243pF$$

$$X_{\mathrm{L2}} = QR = 780\,\Omega \text{ so } L_2 = 62\mu H$$

$$X_{\mathrm{C2}} = (Q - 1.152)R = 711\,\Omega \text{ so } C_2 = 112pF$$

Using the calculated value of R_{DC} with the specified supply voltage gives a power input (and output) of 346mW.

CHAPTER 3

NEW CLASS E STEADY-STATE ANALYSES

3.1 Power Series Analysis

3.1.1 Background and motivation

The canonical analysis of the Class E power amplifier assumes infinite Q in the output circuit. A real circuit will have finite Q, possibly in the region of 10-15. The feed choke L_1 may need to have a small inductance in order to support fast amplitude modulation. A more general analysis starts by obtaining expressions for the circuit charges/currents, typically by using the Laplace transform. Numerical solutions are then obtained [17, 18, 19, 20], with results presented in the form of tables and/or graphs. These are not ideal for a circuit designer, so Sokal [21] performed a curve fit to his solution in order to obtain design equations in terms of Q. All these solutions assume steady-state conditions.

The aim of the present work is to investigate the phase and amplitude modulation characteristics of the Class E circuit. This requires finite Q and some form of analytic solution from which the transient behaviour can be determined. As a first step, a steady-state solution is needed: this provides a foundation for the subsequent work, and also allows a comparison to be made with numerical solutions as a way of validating the method.

A standard technique used by physicists is perturbation theory. In essence, the solution for a difficult problem is expressed as a deviation from the known solution of a simpler problem in the form of a power series in some small parameter – typically a coupling constant. The most successful example of this is quantum electrodynamics (QED - see, for example [33]) which deals with the electromagnetic interactions of electrons.

For Class E a 'simple' solution already exists for infinite Q, and in most practical cases Q is sufficiently large that Q^{-1} is a good candidate for an expansion parameter. Thus it was decided

to attempt to obtain a Class E solution in the form of at least the first few terms of a power series in Q^{-1}. In the high Q limit this should give the canonical solution, while for lower values of Q it should agree with existing numerical solutions found in the literature.

This analysis [1, 5] uses the Heaviside operational calculus (see Appendix A) to obtain general expressions for the charge and current in the output circuit, although the Laplace transform could have been used instead. The Class E conditions of zero charge and current at the switching point are applied, together with the steady-state requirement that the solution should be periodic. On the assumption that the Q is not too small, circuit parameters are then obtained in the form of power series in Q^{-1}.

3.1.2 General solution

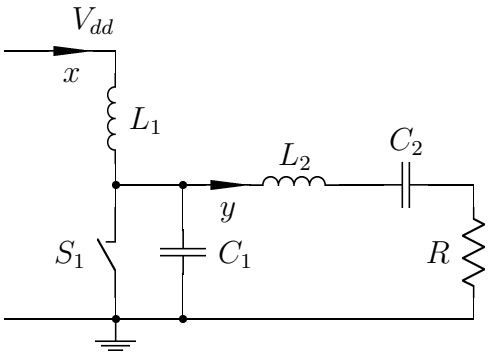

Figure 3.1: Skeleton Class E power amplifier, showing charge

Let x and y be the charge in the feed and output circuits respectively (Figure 3.1). Then the equations of motion are:

switch closed

$$L_1\ddot{x} = V_{\rm dd} \tag{3.1}$$

$$L_2\ddot{y} + \frac{1}{C_2}y + R\dot{y} = 0 \tag{3.2}$$

switch open

$$L_1\ddot{x} + \frac{1}{C_1}(x-y) = V_{\rm dd} \tag{3.3}$$

$$L_2\ddot{y} + \frac{1}{C_2}y + R\dot{y} + \frac{1}{C_1}(y-x) = 0 \tag{3.4}$$

where the dot denotes differentiation with respect to time. Any transient current arising from the discharge of C_1 when the switch closes is ignored. The inductors in the feed and output circuits guarantee continuity of current across the switching transition, as a current discontinuity would require infinite voltage. Continuity of current then guarantees continuity of charge.

Consider first the 'switch open' case. The Heaviside operator p is introduced and initial conditions are included (see Section A.1.3 on page A-3). The result is that equations (3.3) and (3.4) become

$$\left(L_1 p^2 + \frac{1}{C_1}\right) x - \frac{1}{C_1} y = V_{dd} + L_1 p^2 x_0 + L_1 p x_0' \tag{3.5}$$

$$\left(L_2 p^2 + Rp + \frac{1}{C_1} + \frac{1}{C_2}\right) y - \frac{1}{C_1} x = (L_2 p^2 + Rp) y_0 + L_2 p y_0' \tag{3.6}$$

where x_0, x_0' are the charge and current at the start of the 'switch open' interval; similarly for y. The convention adopted is that objects with subscripts $_0$ or $_1$ are constants, with a prime denoting a rate of change. These simultaneous equations can be solved for x and y:

$$x = \frac{\left\{\begin{array}{l} p^4 x_0 + \left(\dfrac{R}{L_2} x_0 + x_0'\right) p^3 \\ \quad + \left[\dfrac{1}{L_2}\left(\dfrac{1}{C_1} + \dfrac{1}{C_2}\right) x_0 + \dfrac{1}{L_1} V_{\mathrm{dd}} + \dfrac{R}{L_2} x_0' + \dfrac{1}{L_1 C_1} y_0\right] p^2 \\ \quad + \left[\dfrac{1}{L_2}\left(\dfrac{1}{C_1} + \dfrac{1}{C_2}\right) x_0' + \dfrac{R}{L_1 L_2} V_{\mathrm{dd}} + \dfrac{R}{L_1 L_2 C_1} y_0\right] p \\ \quad + \dfrac{1}{L_1 L_2}\left(\dfrac{1}{C_1} + \dfrac{1}{C_2}\right) V_{\mathrm{dd}} \end{array}\right\}}{p^4 + \dfrac{R}{L_2} p^3 + \left[\dfrac{1}{L_2}\left(\dfrac{1}{C_1} + \dfrac{1}{C_2}\right) + \dfrac{1}{L_1 C_1}\right] p^2 + \dfrac{R}{L_1 L_2 C_1} p + \dfrac{1}{L_1 L_2 C_1 C_2}} \tag{3.7}$$

$$y = \frac{\left\{\begin{array}{l} p^4 y_0 + \left(\dfrac{R}{L_2} y_0 + y_0'\right) p^3 \\ \quad + \left(\dfrac{1}{L_2 C_1} x_0 + \dfrac{1}{L_1 C_1} y_0\right) p^2 \\ \quad + \left(\dfrac{1}{L_2 C_1} x_0' + \dfrac{1}{L_1 C_1} y_0' + \dfrac{R}{L_1 L_2 C_1} y_0\right) p + \dfrac{1}{L_1 L_2 C_1} V_{\mathrm{dd}} \end{array}\right\}}{p^4 + \dfrac{R}{L_2} p^3 + \left[\dfrac{1}{L_2}\left(\dfrac{1}{C_1} + \dfrac{1}{C_2}\right) + \dfrac{1}{L_1 C_1}\right] p^2 + \dfrac{R}{L_1 L_2 C_1} p + \dfrac{1}{L_1 L_2 C_1 C_2}} \tag{3.8}$$

If a straightforward factorisation of the denominator was possible then these expressions could be written as partial fractions, and the solution obtained. Roughly speaking, L_1 resonates with C_1 and C_2 in parallel, while L_2 resonates with C_1 and C_2 in series. With typical Class E component values, the second mode is at a higher frequency and is more highly damped than the first.

Simplification can be achieved by assuming that L_1 is large, so terms involving its inverse can be ignored. The validity of this approximation is explored in Section D.1 of Appendix D.

Equation (3.7) then becomes

$$x = \frac{\left\{ \begin{array}{l} p^4 x_0 + \left(\dfrac{R}{L_2} x_0 + x_0' \right) p^3 \\ \quad + \left[\dfrac{1}{L_2} \left(\dfrac{1}{C_1} + \dfrac{1}{C_2} \right) x_0 + \dfrac{R}{L_2} x_0' \right] p^2 + \dfrac{1}{L_2} \left(\dfrac{1}{C_1} + \dfrac{1}{C_2} \right) x_0' p \end{array} \right\}}{p^4 + \dfrac{R}{L_2} p^3 + \dfrac{1}{L_2} \left(\dfrac{1}{C_1} + \dfrac{1}{C_2} \right) p^2} \tag{3.9}$$

Collecting terms in the numerator gives

$$x = \frac{\left[p^4 + \dfrac{R}{L_2} p^3 + \dfrac{1}{L_2} \left(\dfrac{1}{C_1} + \dfrac{1}{C_2} \right) p^2 \right] x_0 + \left[p^3 + \dfrac{R}{L_2} p^2 + \dfrac{1}{L_2} \left(\dfrac{1}{C_1} + \dfrac{1}{C_2} \right) p \right] x_0'}{p^4 + \dfrac{R}{L_2} p^3 + \dfrac{1}{L_2} \left(\dfrac{1}{C_1} + \dfrac{1}{C_2} \right) p^2} \tag{3.10}$$

which simplifies to

$$x = \frac{p x_0 + x_0'}{p} \tag{3.11}$$

Applying Heaviside's rule $p^{-1} \rightarrow t$ then gives the result

$$x = x_0 + x_0' t \tag{3.12}$$

which simply says that the current in L_1 remains constant, as expected.

With L_1 large, equation (3.8) for y becomes

$$y = \frac{p^3 y_0 + \left(\dfrac{R}{L_2} y_0 + y_0' \right) p^2 + \dfrac{x_0}{L_2 C_1} p + \dfrac{x_0'}{L_2 C_1}}{p \left[p^2 + \dfrac{R}{L_2} p + \dfrac{1}{L_2} \left(\dfrac{1}{C_1} + \dfrac{1}{C_2} \right) \right]} \tag{3.13}$$

If the circuit is under-damped then the quadratic factor in the denominator has complex conjugate roots at $\dfrac{-1}{\tau} \pm j\omega_0$, where

$$\tau = \frac{2L_2}{R} \tag{3.14}$$

and

$$\omega_0^2 = \frac{1}{L_2} \left(\frac{1}{C_1} + \frac{1}{C_2} \right) - \frac{1}{\tau^2} \tag{3.15}$$

Equation (3.13) can be rewritten as

$$y = \frac{p^3 y_0 + \left(\dfrac{2y_0}{\tau} + y_0' \right) p^2 + \dfrac{1}{L_2 C_1} (x_0 p + x_0')}{p \left(p + \dfrac{1}{\tau} + j\omega_0 \right) \left(p + \dfrac{1}{\tau} - j\omega_0 \right)} \tag{3.16}$$

This now needs to be expressed using the method of partial fractions. The term corresponding to the pole at the origin is easily obtained by using the 'cover up' rule i.e. cover up the single p in the denominator and set $p = 0$ elsewhere. The result is

$$\frac{x_0'}{L_2 C_1} \frac{1}{\frac{1}{\tau^2} + \omega_0^2} \frac{1}{p} = \frac{C_2}{C_1 + C_2} \frac{x_0'}{p} = \frac{r_0}{p} \tag{3.17}$$

where r_0 is the residue at the pole.

It is convenient to keep the two conjugate poles together. The expression can be written as

$$y = \frac{r_0}{p} + F(p) \tag{3.18}$$

where r_0 is given by equation (3.17) and $F(p)$ is the part still to be determined, so

$$F(p) = y - \frac{r_0}{p} \tag{3.19}$$

Substituting equation (3.16) for y allows $F(p)$ to be calculated. After some straightforward but tedious algebra the full result is

$$y = \frac{C_2 x_0'}{C_1 + C_2}\frac{1}{p} + \frac{p^2 y_0 + \left(\dfrac{2y_0}{\tau} + y_0' - \dfrac{C_2}{C_1 + C_2}x_0'\right)p + \dfrac{x_0}{L_2 C_1} - \dfrac{C_2}{C_1 + C_2}\dfrac{2x_0'}{\tau}}{\left(p + \dfrac{1}{\tau}\right)^2 + \omega_0^2} \tag{3.20}$$

This now needs to be written as an explicit function of time by using the Heaviside rules given in Table A.1 on page A-3. Then

$$\begin{aligned} y =& \frac{IC_2}{C_1 + C_2}\left[t - e^{-t/\tau}\left(\frac{\sin\omega_0 t}{\omega_0} - \frac{2}{\tau(\frac{1}{\tau^2} + \omega_0^2)}\left(\cos\omega_0 t + \frac{\sin\omega_0 t}{\tau\omega_0}\right)\right) - \frac{2}{\tau(\frac{1}{\tau^2} + \omega_0^2)}\right] \\ &+ \frac{y_0 C_2}{C_1 + C_2}\left[1 - e^{-t/\tau}\left(\cos\omega_0 t + \frac{\sin\omega_0 t}{\tau\omega_0}\right)\right] \\ &+ e^{-t/\tau}\left[y_0\left(\cos\omega_0 t + \frac{\sin\omega_0 t}{\tau\omega_0}\right) + \frac{y_0'\sin\omega_0 t}{\omega_0}\right] \end{aligned} \tag{3.21}$$

where $I = x_0'$ (i.e. the current through L_1), and x_0 has been replaced by y_0.

The latter substitution can be performed because the 'switch open' state starts with zero volts on C_1 (i.e. zero charge) as the switch was previously closed. With the sign convention used here (see Figure 3.1) the charge on C_1 is $x - y$, so $x_0 = y_0$.

A similar calculation for the 'switch closed' state gives

$$y = e^{-t/\tau}\left[y_1\left(\cos\omega_1 t + \frac{\sin\omega_1 t}{\tau\omega_1}\right) + \frac{y_1'\sin\omega_1 t}{\omega_1}\right] \tag{3.22}$$

where

$$\omega_1^2 = \frac{1}{C_2 L_2} - \frac{1}{\tau^2} \tag{3.23}$$

The decay time constant τ has the same value as for the 'switch open' state - see equation (3.14). There are several ways to define circuit Q, but it seems that the most natural is the ratio of the reactance of L_2 at the design frequency to the load resistance R as this relates directly to τ – see equation (3.26) below.

In principle, equations (3.14), (3.15), (3.21), (3.22) and (3.23) contain a full description of the operation of the ideal infinite-L_1 finite-Q Class E amplifier. They describe the time evolution of the charge in the output circuit during a particular switch state.

Differentiation gives expressions for current:

$$\begin{aligned}\dot{y}_{\text{open}} =& \frac{IC_2}{C_1+C_2} + \left(y_0' - \frac{IC_2}{C_1+C_2}\right) e^{-t/\tau}\cos\omega_0 t \\ &+ \left[y_0\left(\frac{C_2}{C_1+C_2}-1\right)\left(\omega_0+\frac{1}{\tau^2\omega_0}\right) - \frac{y_0'}{\tau\omega_0} - \frac{IC_2}{C_1+C_2}\right] e^{-t/\tau}\sin\omega_0 t\end{aligned} \tag{3.24}$$

$$\dot{y}_{\text{closed}} = y_1' e^{-t/\tau}\cos\omega_1 t - \left[y_1\left(\omega_1+\frac{1}{\tau^2\omega_1}\right) + \frac{y_1'}{\tau\omega_1}\right] e^{-t/\tau}\sin\omega_1 t \tag{3.25}$$

3.1.3 Steady-state Class E solution

A steady-state (i.e. periodic) solution is found by letting the final values of the charge/current become the initial values for the opposite switch state. If a 50% switching duty cycle is assumed then at the switching times

$$\frac{t}{\tau} = \frac{1}{2f_{\text{d}}}\frac{R}{2L_2} = \frac{\pi R}{4\pi f_{\text{d}} L_2} = \frac{\pi}{2Q} \tag{3.26}$$

where $Q = 2\pi f_{\text{d}} L_2/R$ and f_{d} is the design frequency.

It is likely that the two resonant frequencies will be near the design frequency, so let

$$\begin{aligned}\omega_0 &= 2\pi(1+a)f_{\text{d}} \\ \omega_1 &= 2\pi(1+b)f_{\text{d}}\end{aligned} \tag{3.27}$$

where a and b are small. It is expected that, to lowest order, these will vary as Q^{-1} i.e.

$$a = \sum_{i=1}^{\infty} a_i Q^{-i}, \qquad\qquad b = \sum_{i=1}^{\infty} b_i Q^{-i} \tag{3.28}$$

With these substitutions it is possible to find the solution as a series in Q^{-1}. For the sake of clarity only the first order calculation is described in detail.

Working to first order

$$e^{-t/\tau} = 1 - \frac{\pi}{2Q} \tag{3.29}$$

$$\sin\omega_0 t = \sin\frac{2\pi(1+a)f_{\text{d}}}{2f_{\text{d}}} = \sin\pi(1+a) = -\pi a \tag{3.30}$$

similarly

$$\sin\omega_1 t = -\pi b \tag{3.31}$$

$$\cos\omega_0 t = \cos\omega_1 t = -1 \tag{3.32}$$

These are substituted into equation (3.22) to find the charge at the end of the 'switch closed' state, to first order,

$$y_0 = \left(1 - \frac{\pi}{2Q}\right)\left(-y_1 - \frac{b}{2f_\mathrm{d}}y_1'\right) \tag{3.33}$$

and into (3.25) to get the current

$$y_0' = \left(1 - \frac{\pi}{2Q}\right)\left(-y_1' + 2\pi^2 b f_\mathrm{d} y_1\right) \tag{3.34}$$

The Class E conditions require that the total charge and current at C_1 are both zero at the point the switch closes. The charge delivered through L_1 during the 'switch open' phase must therefore be equal to the change in charge in the output circuit i.e.

$$y_1 = y_0 + \frac{I}{2f_\mathrm{d}} \tag{3.35}$$

The current in L_1 must be equal to the current in the output circuit as the switch closes i.e. $y_1' = I$. Equations (3.33) and (3.34) then give

$$\begin{aligned} y_0 &= \frac{I}{4f_\mathrm{d}}\left(-1 - b + \frac{\pi}{4Q}\right) \\ y_1 &= \frac{I}{4f_\mathrm{d}}\left(1 - b + \frac{\pi}{4Q}\right) \\ y_0' &= -I\left(1 - \frac{\pi}{2Q} - \frac{\pi^2 b}{2}\right) \\ y_1' &= I \end{aligned} \tag{3.36}$$

Equation (3.21) gives the charge at the end of the 'switch open' state

$$\begin{aligned} y_1 = &\left(1 - \frac{\pi}{2Q}\right)\left(-y_0 - \frac{a}{2f_\mathrm{d}}y_0'\right) \\ &+ \frac{I}{2f_\mathrm{d}}\left(\frac{C_2}{C_1 + C_2}\right)(1 + a) + \left(\frac{C_2}{C_1 + C_2}\right)y_0 \end{aligned} \tag{3.37}$$

Dividing (3.23) by (3.15), and using the definition of a and b (3.27), gives (to first order)

$$\frac{1 + 2b}{1 + 2a} = 1 + 2b - 2a = \frac{C_1}{C_1 + C_2} \tag{3.38}$$

Subtracting unity from each side provides

$$\left(\frac{C_2}{C_1 + C_2}\right) = 2(a - b) \tag{3.39}$$

Substituting (3.36) and (3.39) into equation (3.37) then gives

$$a + b = \frac{\pi}{2Q} \tag{3.40}$$

Making first order substitutions (e.g. (3.29) and (3.30)) in equation (3.24) gives

$$y_1' = \left(1 - \frac{\pi}{2Q}\right)(-y_0' + 2\pi^2 a f_\mathrm{d} y_0) + \frac{IC_2}{C_1 + C_2}\left(2 - \frac{\pi}{2Q}\right) \tag{3.41}$$

Substituting equations (3.36) and (3.39) then gives

$$a - b = \frac{\pi}{4Q} + \frac{\pi^2}{8}(a + b) = \frac{\pi(\pi^2 + 4)}{16Q} \tag{3.42}$$

From (3.40) and (3.42) the first-order coefficients for a and b are

$$\begin{aligned} a_1 &= \frac{\pi(\pi^2 + 12)}{32} \\ b_1 &= -\frac{\pi(\pi^2 - 4)}{32} \end{aligned} \tag{3.43}$$

This procedure can be carried out to higher orders by retaining further terms in the expansion of exp, sin and cos, and when substituting in the expressions. In each case it is found that the expression for charge gives $a + b$, and the expression for current gives $a - b$. Second and third order results have been obtained by using the Symbolic Toolkit in MATLAB; details are given in Appendix B:

$$\begin{aligned} a_2 &= \frac{1}{2} + \frac{15\pi^2}{64} + \frac{\pi^4}{64} - \frac{5\pi^6}{1024} - \frac{\pi^8}{2048} \\ b_2 &= \frac{1}{2} - \frac{\pi^2}{64} - \frac{3\pi^4}{64} - \frac{\pi^6}{1024} + \frac{\pi^8}{2048} \\ a_3 &= \frac{13\pi}{32} + \frac{39\pi^3}{256} - \frac{25\pi^5}{1024} - \frac{119\pi^7}{8192} - \frac{29\pi^9}{32768} + \frac{21\pi^{11}}{131072} + \frac{7\pi^{13}}{524288} \\ b_3 &= \frac{3\pi}{32} - \frac{95\pi^3}{768} - \frac{173\pi^5}{3072} + \frac{15\pi^7}{8192} + \frac{61\pi^9}{32768} - \frac{\pi^{11}}{131072} - \frac{7\pi^{13}}{524288} \end{aligned} \tag{3.44}$$

Intermediate expressions can be very large, and it was not possible to go beyond third order. Nevertheless, the fact that a solution can be found confirms that exact Class E conditions are possible for finite Q. Evaluating the coefficients gives, to third order:

$$\begin{aligned} a &= 2.14704Q^{-1} - 4.99215Q^{-2} + 14.17831Q^{-3} \\ b &= -0.57625Q^{-1} - 0.52605Q^{-2} - 0.76518Q^{-3} \end{aligned} \tag{3.45}$$

3.1.4 Component values

The inductance of L_2 is determined by (or determines) the circuit Q: $\omega_\mathrm{d} L_2 = QR$, where $\omega_\mathrm{d} = 2\pi f_\mathrm{d}$.

An expression for C_2 can be obtained by rewriting equation (3.23) for ω_1 in terms of b, and using the above value of L_2 in (3.14) to express τ as $2Q/\omega_\mathrm{d}$. Then

$$\omega_\mathrm{d}^2\left((1 + b)^2 + \frac{1}{4Q^2}\right) = \frac{1}{L_2 C_2} \tag{3.46}$$

so

$$\begin{aligned}\frac{1}{\omega_{\rm d}C_2} &= \omega_{\rm d}L_2\left(1+2b+b^2+\frac{1}{4Q^2}\right)\\ &= RQ\left(1+2b+b^2+\frac{1}{4Q^2}\right)\end{aligned} \tag{3.47}$$

In numerical terms this is, to third order,

$$\frac{1}{\omega_{\rm d}C_2} = R(Q-1.1525-0.4700Q^{-1}-0.9241Q^{-2}) \tag{3.48}$$

An infinite-Q analysis gives the first two terms, but usually in the form of an excess inductive reactance in L_2 of $1.1525R$. It can be seen that higher order corrections are quite small.

Q	high Q	After [17]	After [21]	Equation (3.48)
20.597	1.05927	1.0605		1.06063
20	1.06115		1.0626	1.06260
10.621	1.12172	1.1280		1.12797
10	1.13026		1.1375	1.13749
5.673	1.25495	1.2872		1.28670
5	1.29954		1.3462	1.34534
3.750	1.44369	1.5623		1.55831
3	1.62381		1.9040	1.88899

Table 3.1: Output tuning: QR/X_{C2}

An expression for C_1 is found as follows:

$$\frac{1}{\omega_{\rm d}C_1} = \frac{1}{\omega_{\rm d}C_2}\frac{C_2}{C_1} = \frac{1}{\omega_{\rm d}C_2}\left(\frac{C_1+C_2}{C_1}-1\right) \tag{3.49}$$

but, using (3.15) and (3.23)

$$\frac{C_1+C_2}{C_1} = \frac{\omega_0^2+\frac{1}{\tau^2}}{\omega_1^2+\frac{1}{\tau^2}} = \frac{(1+a)^2+\frac{1}{4Q^2}}{(1+b)^2+\frac{1}{4Q^2}} \tag{3.50}$$

so

$$\begin{aligned}\frac{1}{\omega_{\rm d}C_1} &= RQ\left((1+a)^2+\frac{1}{4Q^2}-(1+b)^2-\frac{1}{4Q^2}\right)\\ &= RQ(2(a-b)+a^2-b^2)\end{aligned} \tag{3.51}$$

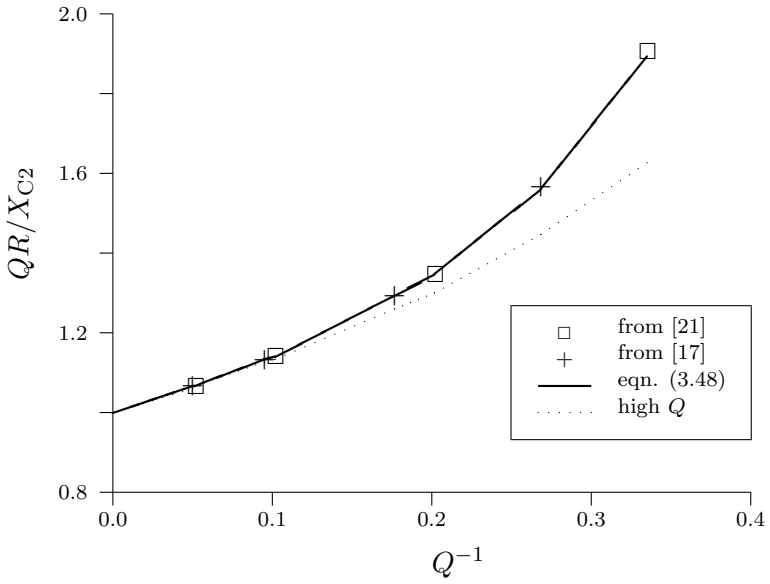

Figure 3.2: Output tuning: QR/X_{C2}

In numerical terms this is, to third order[1],

$$\frac{1}{\omega_d C_1} = R(5.4466 - 4.6545Q^{-1} + 7.8440Q^{-2}) \tag{3.52}$$

An infinite-Q analysis gives the first term only. Unlike C_2, higher order corrections for C_1 are significant for likely values of Q, which typically lies in the range 5–15. For example, a Q of 10 causes a C_1 correction of 7.1%, but only 0.6% for C_2, when compared with the values given by the infinite-Q analysis. It should be noted that (3.47) for C_2 and (3.51) for C_1 are exact, although in practice constrained because only the first few terms of a and b are known.

Component reactance values given by equations (3.48) and (3.52) are compared in Table 3.1/Figure 3.2 and Table 3.2/Figure 3.3 with those given by the infinite-Q analysis [4] and numerical results [17, 21]. Note that [17] uses a definition of Q that is different from the one used here and by Sokal [21].

Alternatively, the output circuit could be considered in terms of its series resonant frequency ω_1 and load resistance R. This may be convenient if an integrated antenna is used. A sufficiently high impedance would need to be presented by the output circuit at harmonic frequencies. Viewing the output circuit in terms of resonant frequency may also provide a convenient way to accommodate a finite L_1 inductance.

[1]The third order result (3.52) appears to be second order, because there is no zeroth order term within the brackets in (3.51) and the expression has been multiplied by Q. Expansion order is a useful concept, but it cannot be reliably determined from the final result if any leading or trailing coefficients happen to be zero.

Q	high Q	From [17]	From [21]	Equation (3.52)
20.597	0.18360	0.1909		0.19087
20	0.18360		0.19111	0.19108
10.621	0.18360	0.1971		0.19693
10	0.18360		0.19790	0.19765
5.673	0.18360	0.2067		0.20535
5	0.18360		0.20907	0.20706
3.750	0.18360	0.2150		0.20994
3	0.18360		0.21834	0.20979

Table 3.2: Drain capacitance: R/X_{C1}

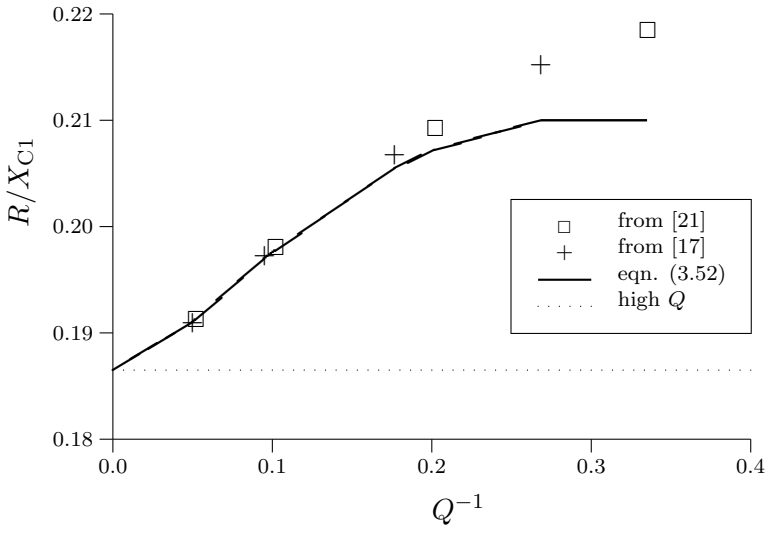

Figure 3.3: Drain capacitance: R/X_{C1}

3.1.5 Power and efficiency

Input power

If it is assumed that L_1 is lossless, then the input DC power is the product of the input current I and the mean drain voltage $V_{\mathrm{d\ avg}}$ (on C_1). C_1 receives charge from both the input and output circuits:

$$V_{\mathrm{d}} = \begin{cases} \dfrac{x_0 + It - y}{C_1} & \text{switch open} \\ 0 & \text{switch closed} \end{cases} \tag{3.53}$$

Substituting for y from equation (3.21), using $x_0 = y_0$, and rearranging to clarify the time dependence gives

$$V_{\mathrm{d\ open}} = \frac{1}{C_1}\left[\begin{array}{l} y_0\left(1 - \dfrac{C_2}{C_1+C_2}\right) + \dfrac{IC_2}{C_1+C_2}\dfrac{2}{\tau(\frac{1}{\tau^2}+\omega_0^2)} \\ + It\left(1 - \dfrac{C_2}{C_1+C_2}\right) + \left(\dfrac{IC_2}{C_1+C_2} - y_0'\right)e^{-t/\tau}\dfrac{\sin\omega_0 t}{\omega_0} \\ + \left(y_0\left(\dfrac{C_2}{C_1+C_2} - 1\right) - \dfrac{IC_2}{C_1+C_2}\dfrac{2}{\tau(\frac{1}{\tau^2}+\omega_0^2)}\right)e^{-t/\tau}\left(\cos\omega_0 t + \dfrac{\sin\omega_0 t}{\tau\omega_0}\right) \end{array}\right] \tag{3.54}$$

Assuming 50% duty cycle

$$V_{\mathrm{d\ avg}} = f\int_0^{\frac{1}{2f}} V_{\mathrm{d\ open}}\mathrm{d}t \tag{3.55}$$

Integration by parts gives

$$V_{\mathrm{d\ avg}} = \frac{1}{C_1}\left[\begin{array}{l} \left(\dfrac{y_0}{2} + \dfrac{I}{8f}\right)\left(1 - \dfrac{C_2}{C_1+C_2}\right) + \dfrac{IC_2}{C_1+C_2}\dfrac{1}{\tau\left(\frac{1}{\tau^2}+\omega_0^2\right)} \\ + f\dfrac{\dfrac{IC_2}{C_1+C_2} - y_0'}{\frac{1}{\tau^2}+\omega_0^2}\left\{1 - e^{-\frac{1}{2f\tau}}\left[\cos\left(\dfrac{\omega_0}{2f}\right) + \dfrac{1}{\tau\omega_0}\sin\left(\dfrac{\omega_0}{2f}\right)\right]\right\} \\ + f\dfrac{y_0\left(\dfrac{C_2}{C_1+C_2} - 1\right) - \dfrac{IC_2}{C_1+C_2}\dfrac{2}{\tau\left(\frac{1}{\tau^2}+\omega_0^2\right)}}{\frac{1}{\tau^2\omega_0}+\omega_0} \\ \times\left\{\dfrac{2}{\tau\omega_0} + e^{-\frac{1}{2f\tau}}\left[\dfrac{-2}{\tau\omega_0}\cos\left(\dfrac{\omega_0}{2f}\right) + \left(1 - \dfrac{1}{\tau^2\omega_0}\right)\sin\left(\dfrac{\omega_0}{2f}\right)\right]\right\} \end{array}\right] \tag{3.56}$$

If known expressions for y_0 etc. are substituted (e.g. equation (3.36)) together with the Class E values for a and b then the result, to second order, is

$$V_{\mathrm{d\ avg}} = \frac{IR(\pi^2+4)}{8}\left(1 + \left(\frac{3\pi}{4} - \frac{\pi^3}{16}\right)Q^{-1} + \left(\frac{1}{2} + \frac{7\pi^2}{96} - \frac{7\pi^4}{64} - \frac{\pi^6}{256} + \frac{3\pi^8}{2048}\right)Q^{-2}\right) \tag{3.57}$$

Expressing this numerically as an equivalent DC resistance ($P_{\mathrm{in}} = I^2 R_{\mathrm{DC}}$):

$$R_{\mathrm{DC}} = 1.73370R(1 + 0.41830Q^{-1} + 0.70933Q^{-2}) \tag{3.58}$$

An infinite-Q analysis gives the first term. Values from equation (3.58) are compared in Table 3.3/Figure 3.4 with numerical results [17, 21].

Q	high Q	From [17]	From [21]	Equation (3.58)
20.597	0.57680	0.5644		0.56439
20	0.57680		0.56402	0.56400
10.621	0.57680	0.5514		0.55161
10	0.57680		0.54974	0.54990
5.673	0.57680	0.5249		0.52639
5	0.57680		0.51659	0.51869
3.750	0.57680	0.4916		0.49639
3	0.57680		0.46453	0.47347

Table 3.3: Input power: R/R_{DC}

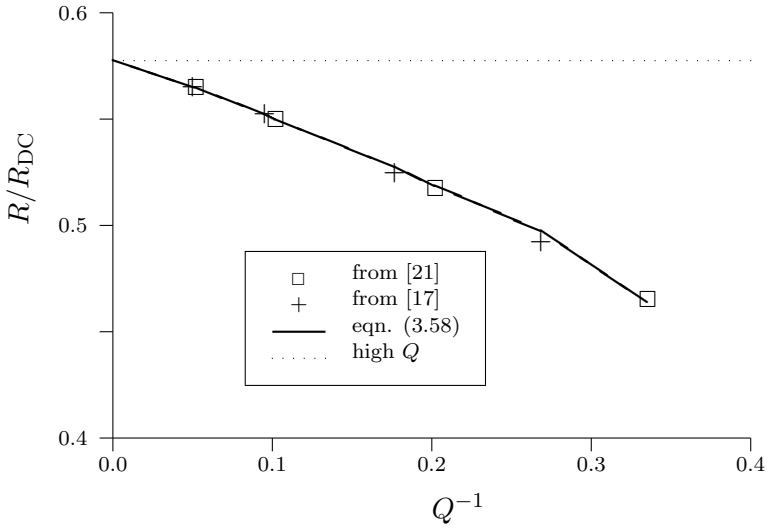

Figure 3.4: Input power: R/R_{DC}

The input power (and hence output power) of a Class E circuit varies with frequency (for example, see [23] or Figure 3.6). Away from the design frequency the Class E conditions no longer hold true, but a solution can still be found to the simultaneous equations for the charge and current (e.g. third order versions of (3.33), (3.34), (3.37) and (3.41), but with design frequency f_{d} now replaced where appropriate by operating frequency $f = f_{\mathrm{d}} + \Delta f$). If the Class E values for a and b are used (from (3.43) and (3.44)), and the charge and current are substituted into equation (3.56) then the frequency response of the input power can be obtained. The result, to

second order in Q^{-1} and normalised frequency offset X, is

$$V_{\mathrm{d\ avg}} = \frac{IR(\pi^2+4)}{8}\left[\begin{array}{l} 1+\left(\frac{3\pi}{4}-\frac{\pi^3}{16}\right)Q^{-1}+\left(\frac{1}{2}+\frac{7\pi^2}{96}-\frac{7\pi^4}{64}-\frac{\pi^6}{256}+\frac{3\pi^8}{2048}\right)Q^{-2} \\ +\frac{X}{\pi^2+4}\left[8\pi+\left(12+\pi^2-\frac{3\pi^4}{4}+\frac{\pi^6}{16}\right)Q^{-1}\right] \\ +X\pi(\pi^2-4)\left(-\frac{9}{16}+\frac{13\pi^2}{128}+\frac{3\pi^4}{512}-\frac{\pi^6}{1024}\right)Q^{-2} \\ +\frac{X^2}{(\pi^2+4)^2} \\ \times\left[\begin{array}{l} -32+32\pi^2+2\pi^4+\pi\left(136+2\pi^2-\frac{7\pi^4}{2}+\frac{\pi^6}{8}\right)Q^{-1} \\ +\left(104-\frac{85\pi^2}{6}-\frac{65\pi^4}{6}-\frac{97\pi^6}{48}+\frac{\pi^8}{4}+\frac{5\pi^{10}}{512}\right)Q^{-2} \end{array}\right] \end{array}\right] \tag{3.59}$$

where

$$X = \frac{\Delta f}{f_{\mathrm{d}}}Q \tag{3.60}$$

Expressing this numerically in the form of the equivalent DC resistance gives

$$R_{\mathrm{DC}}(X) = 1.73370R\left[\begin{array}{l} 1+0.41830Q^{-1}+0.70933Q^{-2} \\ +X(1.81207+0.64166Q^{-1}+1.32364Q^{-2}) \\ +X^2(2.48820-1.06185Q^{-1}+1.31402Q^{-2}) \end{array}\right] \tag{3.61}$$

Alternatively, this can be expressed in terms of input power from a constant voltage supply:

$$P_{\mathrm{in}}(X) = \frac{V_{\mathrm{dd}}^2}{1.73370R}\left[\begin{array}{l} 1-0.41830Q^{-1}-0.53435Q^{-2} \\ +X(-1.81207+0.87433Q^{-1}+0.83267Q^{-2}) \\ +X^2(0.79541+1.34835Q^{-1}-1.22818Q^{-2}) \end{array}\right] \tag{3.62}$$

Cantrell suggested [23] that the undesirable power variation with frequency of a Class E amplifier can be minimised by using a DC power supply with a source resistance equal to R_{DC}. Equations (3.61) and (3.62) allow the use of a programmable power supply as an alternative, so that the relatively flat efficiency spectrum can be exploited despite the steep slope of the power spectrum.

Output power

The output power at the fundamental frequency can be found by Fourier analysis of the output current, which is given by equations (3.24) and (3.25) for 'switch open' and 'switch closed' respectively.

The sine and cosine components of the fundamental current are

$$I_s = 2f\left(\int_0^{\frac{1}{2f}} \dot{y}_{\text{open}} \sin\omega t \mathrm{d}t - \int_0^{\frac{1}{2f}} \dot{y}_{\text{closed}} \sin\omega t \mathrm{d}t\right) \tag{3.63}$$

and

$$I_c = 2f\left(\int_0^{\frac{1}{2f}} \dot{y}_{\text{open}} \cos\omega t \mathrm{d}t - \int_0^{\frac{1}{2f}} \dot{y}_{\text{closed}} \cos\omega t \mathrm{d}t\right) \tag{3.64}$$

Following integration (see Appendix A), the solutions for y_0 etc. are substituted, then

$$P_{\text{out}} = \frac{1}{2}(I_s^2 + I_c^2)R \tag{3.65}$$

It was found that zeroth-order terms cancelled, so a third-order calculation gave a result which appears to be second-order. The output power, as a function of Q and X, is

$$\begin{aligned} P_{\text{out}}(X) = {} & \frac{I^2R(\pi^2+4)}{8} \\ & \times \left[\begin{array}{l} 1 + \left(\frac{3\pi}{4} - \frac{\pi^3}{16}\right)Q^{-1} + \left(\frac{93}{48} + \frac{161\pi^2}{384} - \frac{95\pi^4}{768} - \frac{43\pi^6}{6144} + \frac{17\pi^8}{12288}\right)Q^{-2} \\ + \frac{X}{\pi^2+4}\left[\begin{array}{l} 8\pi + \left(12 + \pi^2 - \frac{3\pi^4}{4} + \frac{\pi^6}{16}\right)Q^{-1} \\ + \pi\left(9 - \frac{25\pi^2}{16} - \frac{61\pi^4}{96} + \frac{89\pi^6}{768} + \frac{\pi^8}{192} - \frac{\pi^{10}}{1024}\right)Q^{-2} \end{array}\right] \\ + \frac{X^2}{(\pi^2+4)^2} \\ \times \left[\begin{array}{l} -48 + 40\pi^2 + \pi^4 + \pi\left(188 - 7\pi^2 - \frac{23\pi^4}{4} + \frac{7\pi^6}{16}\right)Q^{-1} \\ + \left(127 - \frac{1319\pi^2}{24} - \frac{1093\pi^4}{48} - \frac{185\pi^6}{192} + \frac{671\pi^8}{768} - \frac{13\pi^{10}}{2048} - \frac{55\pi^{12}}{12288}\right)Q^{-2} \end{array}\right] \end{array}\right] \end{aligned} \tag{3.66}$$

Expressed numerically

$$P_{\text{out}}(X) = 1.73370I^2R\left[\begin{array}{l} 1 + 0.41830Q^{-1} + 0.42480Q^{-2} \\ + X(1.81207 + 0.64166Q^{-1} + 0.24024Q^{-2}) \\ + X^2(2.30911 - 0.33613Q^{-1} - 0.00585Q^{-2}) \end{array}\right] \tag{3.67}$$

Drain efficiency

The drain efficiency may be found from (3.61) and (3.67):

$$\eta_{\text{D}}(X) = 1 - (0.28453 + 0.56781X)Q^{-2} - (0.17910 - 0.80064Q^{-1} - 0.20915Q^{-2})X^2 \tag{3.68}$$

The loss terms roughly correspond to harmonics (Q^{-2}) and stored charge in C_2 (X^2). Note that there are no purely linear terms; hence an infinite-Q analysis yields useful results for a practical

circuit. At the centre frequency (i.e. exact Class E conditions) there are no switch losses so all the lost power appears as harmonics in the load. The harmonic power is

$$P_{\text{harm.total}} = -5.46 - 20\log Q + 10\log(1 + 2X) \text{ dBc} \tag{3.69}$$

This is in good agreement (Table 3.4) with the numerical results for harmonic current (up to 10th) obtained by Sokal and Raab [34]. The second harmonic dominates, so (3.69) gives a good estimate of this too.

Q	3	4	5	7.5	10
P_2 dBc (after [34])	-15.19	-17.86	-19.83	-23.49	-26.04
P_{2-10} dBc (after [34])	-15.04	-17.71	-19.69	-23.36	-25.91
$P_{\text{harm.total}}$ dBc (3.69)	-15.00	-17.50	-19.44	-22.96	-25.46

Table 3.4: Harmonic output power

For finite Q the point of maximum efficiency is just below the centre frequency (Figure 3.5). As the frequency reduces, harmonic power reduces faster than stored charge losses increase. This is because the phase of the AC current shifts to give a smaller slope in drain voltage at the point of switch-off.

$$\eta_{\text{D max}} = 1 - 0.28453Q^{-2} + 0.45005Q^{-4} \tag{3.70}$$

at

$$X_{\text{max effy}} = -1.585Q^{-2} - 7.087Q^{-3} \tag{3.71}$$

A slightly lower frequency will give even smaller harmonic power, but at the cost of reduced efficiency. However, it is likely that these effects will be negligible in a non-ideal physical circuit.

3.1.6 Domain of applicability

Any power series solution must be accompanied by some consideration of the domain of applicability. As this is a physical system, well attested by numerical solutions and experimental implementations, it can be assumed that the series will converge within some domain of Q^{-1} and normalised frequency offset X about zero. Given only the first few terms, over what domain do the series give useful results?

For engineering design an accuracy of a few percent should be sufficient. The likely error can be assumed to be equal to the lowest order omitted term. Most of the series have coefficients

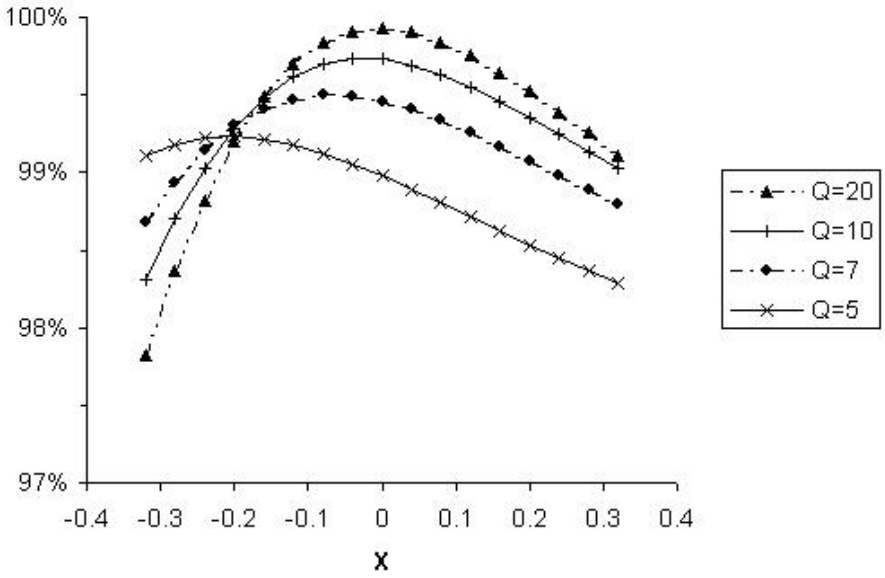

Figure 3.5: Drain efficiency frequency response

which are around 1 for the lower order terms. If it is assumed that this remains true for higher order terms, then the likely error from omitting the nth order term is simply x^n. Thus for second order expressions (e.g. power, efficiency) the error should be no more than 3% for $|X|$, $Q^{-1} < 0.31$. However, almost all results depend on a and b (3.45) and the series for a has rising coefficients. If no assumption is made about the sign of higher coefficients then $Q^{-1} < 0.12$ for 3% error. If it is assumed that the sign continues to oscillate then $Q^{-1} < 0.15$ (for example, see Figure 3.3).

To summarise, it appears that the expressions given will give useful results for $|X|$ up to about 0.3, for Q values above 6. For the purpose of comparison, it may be useful to remember that the -3dB bandwidth of a single tuned circuit corresponds to $|X| \leq 0.5$.

3.2 Energy Balance Analysis

3.2.1 Introduction

The canonical analysis [4] provides a spot solution at the design frequency. Unfortunately Class E shows considerable power variation with frequency and this has limited the usefulness of the circuit as a power amplifier. Cantrell [23], following Raab [22], explored variations in component values and operating frequency away from the optimum. Their expressions involved both load angle ψ and AC phase ϕ, but a relation between these was obtained - (13) in [23]. The load angle is set by the series tuned output circuit C_2-L_2-R (Figure 3.1) and is determined

by the ratio of the net reactance to the resistance. The net reactance depends on the carrier frequency. Thus in principle the frequency response of the Class E circuit was obtained, and graphs based on numerical calculations were presented.

However, Cantrell and Davis [24] later said "no theoretical equation exists to predict the amount of frequency shift needed" to get a specified power output from a Class E power amplifier. They were exploiting the frequency response to produce a high efficiency DC-DC converter for use as an amplitude modulator. The envelope signal was used to modulate the switching frequency of the converter.

A knowledge of the frequency response is a vital ingredient in understanding the phase modulation response, at least in the quasi-static case. Given that no expression could be found in the literature, an attempt was made to estimate the response for the power input maximum and minimum by using conservation of energy. The hope was that something like a linear interpolation could perhaps be used to estimate the response at other points, and hence determine the first-order behaviour during phase modulation. Conservation of energy proved to be unexpectedly useful, and a full frequency response was obtained in a much simpler form than anticipated. The analysis [6] is given below.

The power series expression for Class E frequency response obtained in Section 3.1 is valid only near the design frequency. Ideally an expression valid out to at least $|X| \sim 1$ is needed. Thus there remains a need for an analysis giving the frequency response of Class E over a wider bandwidth. The work presented here fills this gap. It also provides a new way to explore the effect of variations in the shunt capacitance C_1.

It is known [22, 23] that the canonical Class E solution is not the only one giving 100% efficiency; varying frequency (i.e. AC phase) or C_1 each lead to alternative spot solutions but the relationship between them has not been clear. Allowing both AC phase and C_1 to vary provides a family of solutions, and also casts light on series-tuned Class C.

3.2.2 Power balance

By using conservation of energy it is possible to obtain expressions for power and efficiency which depend only on the AC phase. Combining these with a formula for AC phase as a function of normalised frequency offset, it was found that the final expressions were simple rational functions. This result was unexpected! High Q is assumed, but the results should still provide useful approximations for lower Q circuits.

Conservation of energy requires that under static or quasi-static conditions

$$P_{\text{in}} = P_{\text{out}} + P_{\text{loss}} \tag{3.72}$$

High Q means that the only currents are DC and fundamental AC i.e. no power is converted to harmonics. The only loss mechanism is due to stored energy in C_1, which is dissipated when the switch closes. It is assumed that the switch is ideal - infinitesimally small 'closed' resistance, infinite 'open' resistance. The stored energy is lost via resistive heating of the switch. A perfect switch with zero resistance would still dissipate the stored energy, but via radiation, as C_1 and the inductance of the switch connections would form a tuned circuit with finite size and therefore non-zero radiation resistance.

$$\begin{aligned} P_{\text{in}} &= I_{\text{DC}} V_{\text{d\_avg}} \\ P_{\text{out}} &= \frac{1}{2} I_{\text{AC}}^2 R \\ P_{\text{loss}} &= \frac{1}{2} f C_1 V_{\text{d\_sw}}^2 \end{aligned} \tag{3.73}$$

where $V_{\text{d\_avg}}$ is the average drain voltage, and $V_{\text{d\_sw}}$ is the drain voltage at the instant the switch closes.

The instantaneous AC current flowing out through R is given by

$$I_{\text{AC}} \sin(2\pi f t + \phi) = I_{\text{AC}}[\cos(2\pi f t) \sin\phi + \sin(2\pi f t) \cos\phi] \tag{3.74}$$

where f is the signal frequency and ϕ is the AC phase relative to the switching cycle.

Switching loss

At 50% duty cycle the total charge deposited in the drain capacitor C_1 is

$$\begin{aligned} q &= \int_0^{\frac{1}{2f}} [I_{\text{DC}} - I_{\text{AC}}(\cos(2\pi f t) \sin\phi + \sin(2\pi f t) \cos\phi)] \mathrm{d}t \\ q &= \frac{I_{\text{DC}}}{2f} - \frac{I_{\text{AC}} \cos\phi}{\pi f} \end{aligned} \tag{3.75}$$

Then from (3.73) and $V_{\text{d\_sw}} = q/C_1$

$$P_{\text{loss}} = \frac{1}{2fC_1} \left(\frac{I_{\text{DC}}}{2} - \frac{I_{\text{AC}} \cos\phi}{\pi} \right)^2 \tag{3.76}$$

but the standard Class E solution gives (to lowest order – see (3.42) and (3.51))

$$\frac{1}{2\pi f_{\text{d}} C_1} = \frac{\pi(\pi^2 + 4)}{8} R \tag{3.77}$$

and with high Q and assuming the frequency is in the vicinity of the centre, $f \simeq f_{\text{d}}$ so

$$P_{\text{loss}} = \frac{(\pi^2 + 4)}{32} (\pi I_{\text{DC}} - 2 I_{\text{AC}} \cos\phi)^2 R \tag{3.78}$$

Input power

The average drain voltage $V_{\text{d\_avg}}$ is found by integrating the charge on C_1.

$$\begin{aligned} V_{\text{d\_avg}} &= \frac{f}{C_1}\int_0^{\frac{1}{2f}} [I_{\text{DC}}t - \frac{I_{\text{AC}}}{2\pi f}(\sin(2\pi ft)\sin\phi + (1-\cos(2\pi ft))\cos\phi)]\text{d}t \\ &= \frac{1}{fC_1}\left[\frac{1}{8}I_{\text{DC}} - \frac{I_{\text{AC}}}{4\pi^2}(2\sin\phi + \pi\cos\phi)\right] \end{aligned} \tag{3.79}$$

Using (3.77) gives

$$V_{\text{d\_avg}} = \frac{\pi^2+4}{16}\left[\frac{\pi^2}{2}I_{\text{DC}} - I_{\text{AC}}(2\sin\phi + \pi\cos\phi)\right]R \tag{3.80}$$

Magnitude of AC current

The AC current can now be found by using the power balance equation (3.72) with (3.73) and (3.80)

$$I_{\text{DC}}V_{\text{d\_avg}} = \frac{1}{2}I_{\text{AC}}^2R + \frac{(\pi^2+4)}{32}(\pi I_{\text{DC}} - 2I_{\text{AC}}\cos\phi)^2R \tag{3.81}$$

Then it is found that the terms in I_{DC}^2 cancel, a common factor of $I_{\text{AC}}R$ can be removed, and the final result is

$$I_{\text{AC}} = \frac{\pi\cos\phi - 2\sin\phi}{\frac{8}{\pi^2+4} + 2\cos^2\phi}I_{\text{DC}} \tag{3.82}$$

Power and efficiency

Output power is easily obtained from (3.82):

$$P_{\text{out}} = \frac{1}{2}I_{\text{DC}}^2R\left(\frac{\pi\cos\phi - 2\sin\phi}{\frac{8}{\pi^2+4} + 2\cos^2\phi}\right)^2 \tag{3.83}$$

Input power is found by substituting (3.82) into (3.80)

$$\begin{aligned} P_{\text{in}} &= I_{\text{DC}}^2R\frac{\pi^2+4}{16}\left[\frac{\pi^2}{2} + \left(\frac{2\sin\phi - \pi\cos\phi}{\frac{8}{\pi^2+4} + 2\cos^2\phi}\right)(2\sin\phi + \pi\cos\phi)\right] \\ &= I_{\text{DC}}^2R\frac{\pi^2+4}{16}\left[\frac{\pi^2}{2} - \frac{(\pi^2+4)\cos^2\phi - 4}{\frac{8}{\pi^2+4} + 2\cos^2\phi}\right] \\ &= I_{\text{DC}}^2R\frac{\pi^2+4}{8}\left[\frac{\pi^2 + (\pi^2+4)\sin^2\phi}{4 + (\pi^2+4)\cos^2\phi}\right] \end{aligned} \tag{3.84}$$

It can be seen that P_{in} is even in ϕ.

Drain efficiency is simply $P_{\text{out}}/P_{\text{in}}$ using (3.83) and (3.84)

$$\eta = \frac{(\pi^2+4)(\pi\cos\phi - 2\sin\phi)^2}{[\pi^2 + (\pi^2+4)\sin^2\phi][4 + (\pi^2+4)\cos^2\phi]} \tag{3.85}$$

Canonical solution

One could solve $\eta = 1$ to find the AC phase for 100% efficiency, but the solutions are already well known. The standard Class E solution (point A in [23]) is given by $\phi = \arctan(-2/\pi)$ i.e. $\sin\phi = -2/\sqrt{\pi^2+4}$, $\cos\phi = \pi/\sqrt{\pi^2+4}$. Substituting these values gives

$$P_{\text{out}} = P_{\text{in}} = \frac{\pi^2+4}{8} I_{\text{DC}}^2 R \quad , \quad \eta = 1 \tag{3.86}$$

as expected.

There is an alternative (higher frequency) solution (point D in [23]) which also gives 100% efficiency. This has previously been found numerically [22, 23] to correspond to $\psi = 64.3948°$, but from (3.85) it is given by $\phi = \arctan(-\pi/2)$, $\sin\phi = -\pi/\sqrt{\pi^2+4}$, $\cos\phi = 2/\sqrt{\pi^2+4}$. This gives

$$P_{\text{out}} = P_{\text{in}} = \frac{\pi^2(\pi^2+4)}{32} I_{\text{DC}}^2 R \quad , \quad \eta = 1 \tag{3.87}$$

Whether this second solution gives higher or lower power depends on whether the PA has constant voltage or constant current power supply. For phases between these two solutions the efficiency remains close to 100%.

3.2.3 Frequency response

It is clear that the AC phase ϕ is closely related to the load angle ψ. Cantrell, following Raab, gives an expression (equation (13) in [23]):

$$\phi(\psi) = \arctan\left(\frac{\pi}{2} - \frac{32+8\pi^2}{\pi^3+12\pi-16\tan\psi}\right) \tag{3.88}$$

This is derived by considering the fundamental Fourier component of the voltage at the switch.

The load angle depends on the Q and frequency. In general

$$\tan\psi = \frac{2\pi f L_2 - \frac{1}{2\pi f C_2}}{R} \tag{3.89}$$

The canonical Class E analysis gives an excess inductive reactance at the design frequency of

$$\frac{\pi(\pi^2-4)}{16} R = 1.1525R \tag{3.90}$$

so with Q defined by the reactance of L_2 at the design frequency (3.89) becomes

$$\tan\psi = Q\frac{f}{f_{\text{d}}} - \left(Q - \frac{\pi(\pi^2-4)}{16}\right)\frac{f_{\text{d}}}{f} \tag{3.91}$$

For sufficiently high Q and near the design frequency a good approximation is

$$\tan\psi = 2X + \frac{\pi(\pi^2-4)}{16} \tag{3.92}$$

where $X = Q\Delta f/f_{\rm d}$. Substituting this into (3.88) gives

$$\begin{aligned}\phi(X) &= \arctan\left(\frac{\pi}{2} - \frac{32+8\pi^2}{\pi^3+12\pi-32X-\pi(\pi^2-4)}\right)\\ \phi(X) &= \arctan\left(-\frac{2+\pi X}{\pi-2X}\right)\end{aligned} \tag{3.93}$$

The correct quadrant is obtained by using

$$\sin\phi = -\frac{2+\pi X}{\sqrt{(\pi^2+4)(1+X^2)}} \tag{3.94}$$

$$\cos\phi = \frac{\pi-2X}{\sqrt{(\pi^2+4)(1+X^2)}} \tag{3.95}$$

The frequency offset for the second 100% point D can be found using (3.93).

$$\begin{aligned}-\frac{\pi}{2} &= \left(-\frac{2+\pi X}{\pi-2X}\right)\\ X &= \frac{\pi^2-4}{4\pi}\end{aligned} \tag{3.96}$$

Substituting (3.94) and (3.95) into (3.84), (3.83) and (3.85) respectively give

$$P_{\rm in}(X) = I_{\rm DC}^2 R\frac{\pi^2+4}{8}\left(\frac{1+\frac{4\pi X}{\pi^2+4}+\frac{2\pi^2X^2}{\pi^2+4}}{1-\frac{4\pi X}{\pi^2+4}+\frac{8X^2}{\pi^2+4}}\right) \tag{3.97}$$

$$P_{\rm out}(X) = I_{\rm DC}^2 R\frac{\pi^2+4}{8}\frac{1+X^2}{\left(1-\frac{4\pi X}{\pi^2+4}+\frac{8X^2}{\pi^2+4}\right)^2} \tag{3.98}$$

$$\eta(X) = \frac{1+X^2}{\left(1+\frac{4\pi X}{\pi^2+4}+\frac{2\pi^2X^2}{\pi^2+4}\right)\left(1-\frac{4\pi X}{\pi^2+4}+\frac{8X^2}{\pi^2+4}\right)} \tag{3.99}$$

The expressions for power can alternatively be written in terms of DC supply voltage:

$$P_{\rm in}(X) = \frac{8V_{\rm dd}^2}{(\pi^2+4)R}\left(\frac{1-\frac{4\pi X}{\pi^2+4}+\frac{8X^2}{\pi^2+4}}{1+\frac{4\pi X}{\pi^2+4}+\frac{2\pi^2X^2}{\pi^2+4}}\right) \tag{3.100}$$

$$P_{\rm out}(X) = \frac{8V_{\rm dd}^2}{(\pi^2+4)R}\frac{1+X^2}{\left(1+\frac{4\pi X}{\pi^2+4}+\frac{2\pi^2X^2}{\pi^2+4}\right)^2} \tag{3.101}$$

In each case the result is shown in the form *canonical result* $\times f(X)$, where $f(0) = 1$. These expressions are plotted in Figure 3.6, normalised to a load of 1Ω and DC supply of 1V. Efficiency

remains high for X from -0.3 to 0.8, but there is a large variation in power over this frequency range.

Comparisons at the specific points ABCDE highlighted by Cantrell [23] show excellent agreement. Cantrell expressed these points (in his Table 1) in terms of load angle and phase angle, determined by numerical root-finding. Table 3.5 gives the value of normalised frequency X for each of them. For all except point B these are easily obtained from (3.92) or (3.93). Point B was obtained by differentiating (3.101), setting the numerator equal to zero, then (numerically) solving the resultant cubic equation in X. The X values were then substituted into the expressions derived above; the results are shown in Table 3.6.

pt.	description	X expression	X value
E	peak input	$\frac{-2}{\pi}$	-0.6366
C	series resonance	$\frac{-\pi(\pi^2-4)}{32}$	-0.5763
B	peak output	$\frac{\mathrm{d}P_{\mathrm{out}}}{\mathrm{d}X}=0$	-0.4296
A	optimum	0	0
D	alternative	$\frac{\pi}{4}-\frac{1}{\pi}$	0.4671

Table 3.5: Comparison with Cantrell [23] - determination of X values

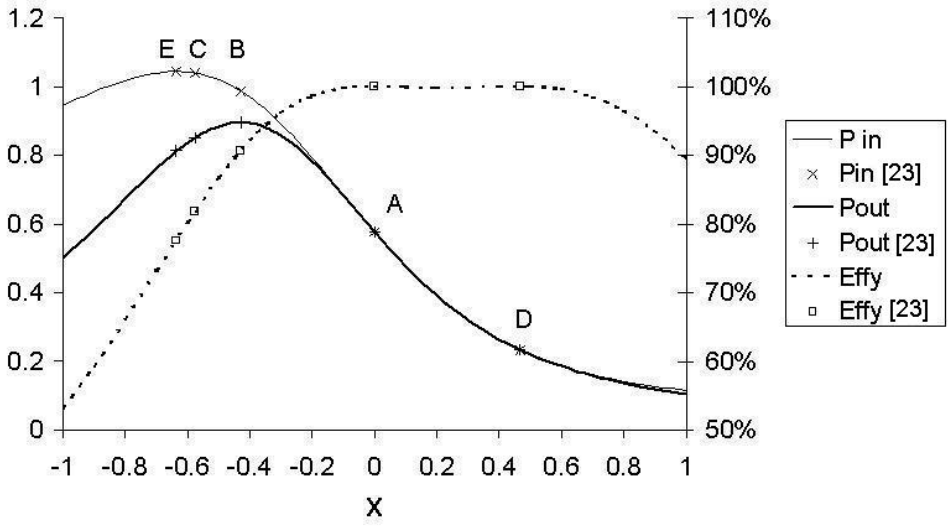

Figure 3.6: Normalised frequency response of power and drain efficiency

	P_{in}		P_{out}		efficiency	
pt.	[23]	(3.100)	[23]	(3.101)	[23]	(3.99)
E	1.81	1.8106	1.41	1.4053	77.6%	77.62%
C	1.803	1.8029	1.474	1.4745	81.8%	81.78%
B	1.712	1.7124	1.553	1.5528	90.7%	90.68%
A	1.000	1.0000	1.000	1.0000	100.0%	100.00%
D	0.405	0.4053	0.405	0.4053	100.0%	100.00%

Table 3.6: Comparison with Cantrell [23] - results

3.2.4 Comparison with power series results

The results from the energy balance analysis ought to agree with those obtained from the power series analysis, in the high Q limit. For example, consider P_{in} from (3.59) and (3.97).

By expressing the denominator as a power series, equation (3.97) can be re-written as

$$P_{\text{in}}(X) = I_{\text{DC}}^2 R \frac{\pi^2+4}{8}\left(1+\frac{4\pi X}{\pi^2+4}+\frac{2\pi^2X^2}{\pi^2+4}\right)\left(1+\frac{4\pi X}{\pi^2+4}-\frac{8X^2}{\pi^2+4}+\frac{16\pi^2X^2}{(\pi^2+4)^2}+\ldots\right) \tag{3.102}$$

Multiplying out the brackets and collecting terms up to second order in X gives

$$P_{\text{in}}(X) = I_{\text{DC}}^2 R \frac{\pi^2+4}{8}\left(1+\frac{8\pi X}{\pi^2+4}+\frac{2(\pi^2-4)X^2}{\pi^2+4}+\frac{32\pi^2X^2}{(\pi^2+4)^2}\right) \tag{3.103}$$

This can be rewritten as

$$P_{\text{in}}(X) = I_{\text{DC}}^2 R \frac{\pi^2+4}{8}\left(1+\frac{8\pi X}{\pi^2+4}+\frac{2X^2(\pi^4+16\pi^2-16)}{(\pi^2+4)^2}\right) \tag{3.104}$$

which can now be compared with (3.59) in the high Q limit.

The two analyses cover overlapping domains:

power series X small – typically $|X| < 0.3$, Q finite – typically $Q > 6$.

energy balance X larger – typically $|X| < 1$, Q infinite.

Given that the two analyses agree where they are both valid, it might be possible to produce hybrid expressions, taking the X dependence from the energy balance analysis and adding at least the first order Q dependence from the power series analysis. Alternatively, some of the approximations could be improved. For example, equation (3.92) could be modified to include a first-order Q term, and the expression for C_1 could include the known Q dependence. However, a finite-Q version of (3.88) would be required too, so this has not been pursued.

3.2.5 Shunt capacitance

Analysis

The effect of varying C_1 can be explored by repeating the calculations in Section 3.2.2, but with (3.77) replaced by

$$\frac{1}{2\pi f_{\rm d} C_1} = c\frac{\pi(\pi^2+4)}{8}R \tag{3.105}$$

so the canonical Class E model is given by $c = 1$. Then (3.78), (3.82), (3.83), (3.84), (3.85) respectively become

$$\begin{aligned}
P_{\rm loss} &= c\frac{(\pi^2+4)}{32}(\pi I_{\rm DC} - 2I_{\rm AC}\cos\phi)^2 R && (3.106)\\
I_{\rm AC} &= \frac{\pi\cos\phi - 2\sin\phi}{\frac{8}{(\pi^2+4)c} + 2\cos^2\phi} I_{\rm DC} && (3.107)\\
P_{\rm out} &= \frac{1}{2} I_{\rm DC}^2 R \left(\frac{\pi\cos\phi - 2\sin\phi}{\frac{8}{(\pi^2+4)c} + 2\cos^2\phi}\right)^2 && (3.108)\\
P_{\rm in} &= I_{\rm DC}^2 Rc\frac{\pi^2+4}{8}\left[\frac{\pi^2 + c(\pi^2+4)\sin^2\phi}{4 + c(\pi^2+4)\cos^2\phi}\right] && (3.109)\\
\eta &= \frac{c(\pi^2+4)(\pi\cos\phi - 2\sin\phi)^2}{[\pi^2 + c(\pi^2+4)\sin^2\phi][4 + c(\pi^2+4)\cos^2\phi]} && (3.110)
\end{aligned}$$

The input and output power can alternatively be expressed as

$$\begin{aligned}
P_{\rm in} &= \frac{8V_{\rm dd}^2}{(\pi^2+4)Rc}\left[\frac{4 + c(\pi^2+4)\cos^2\phi}{\pi^2 + c(\pi^2+4)\sin^2\phi}\right] && (3.111)\\
P_{\rm out} &= \frac{8V_{\rm dd}^2}{R}\left[\frac{(\pi\cos\phi - 2\sin\phi)^2}{[\pi^2 + c(\pi^2+4)\sin^2\phi]^2}\right] && (3.112)
\end{aligned}$$

AC phase

Equation (3.93) relating ϕ to X only applies when $c = 1$. However a more general expression can be derived. Cantrell gives expressions for Raab's g and h – these are (8) and (9) respectively in [23]. g and h both give the ratio of the peak AC output current to the DC supply current, and so must be equal. They are found by considering the in-phase and quadrature fundamental components of the drain/collector voltage – see [4]. A change in shunt capacitance leaves g unchanged

$$g = \frac{\pi\sin(\phi+\psi) + 2\cos(\phi+\psi)}{2\cos\phi\sin(\phi+\psi) + (\pi/2)\cos\psi} \tag{3.113}$$

but h is modified (compare with (10) in [23]):

$$h = \frac{\pi\cos(\phi+\psi) - 2\sin(\phi+\psi)}{\frac{8\sec\psi}{(\pi^2+4)c} - \frac{\pi}{2}\sin\psi + 2\cos\phi\cos(\phi+\psi)} \tag{3.114}$$

Setting $g = h$ and simplifying gives

$$\phi(\psi, c) = \arctan\left(\frac{\pi}{2} - \frac{4(1+c)(\pi^2+4)}{\pi^3 + 4(2+c)\pi - 16\tan\psi}\right) \tag{3.115}$$

Substituting (3.92) for $\tan\psi$ gives an expression for ϕ in terms of X and c:

$$\phi(X, c) = \arctan\left(\frac{(\pi^2/32)(\pi^2-4)(c-1) - \pi X - (1+c)}{(\pi/16)(\pi^2+4)(c-1) + \pi - 2X}\right) \tag{3.116}$$

Combining (3.116) with (3.110) and (3.111) respectively, efficiency and input power are plotted in Figures 3.7 and 3.8. The efficiency moves from a single peak to a double-hump response as c increases. The general shape of the input power response is independent of c, but there is an inversion of plot order with respect to c when comparing the central region with the frequency extremes.

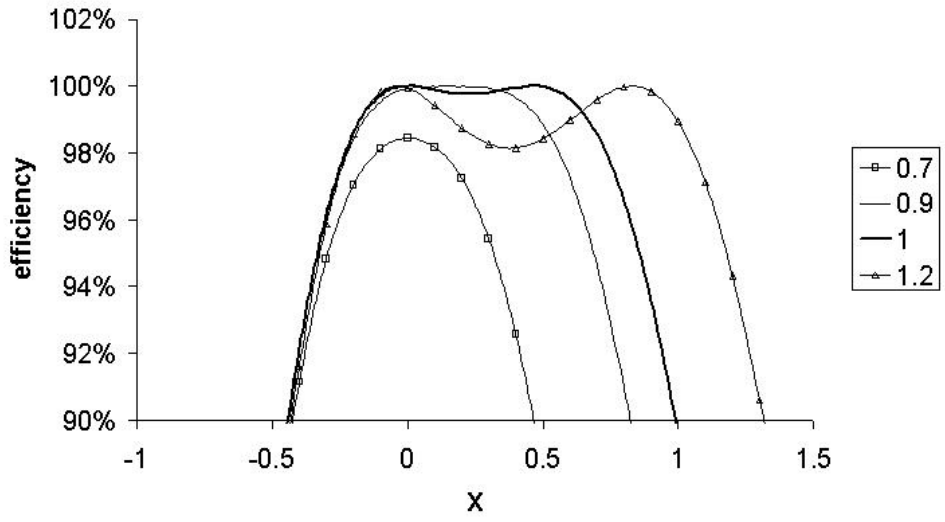

Figure 3.7: Efficiency frequency response (with c as a parameter)

100% efficiency

From (3.106) it can be seen that the condition for zero loss is

$$\pi I_{\mathrm{DC}} = 2I_{\mathrm{AC}}\cos\phi \tag{3.117}$$

Substituting for I_{AC} from (3.107), simplifying and using a double angle formula gives

$$\sin 2\phi + \frac{4\pi}{(\pi^2+4)c} = 0 \tag{3.118}$$

A solution is possible only if

$$|c| \geq \frac{4\pi}{\pi^2+4} = 0.90604 \tag{3.119}$$

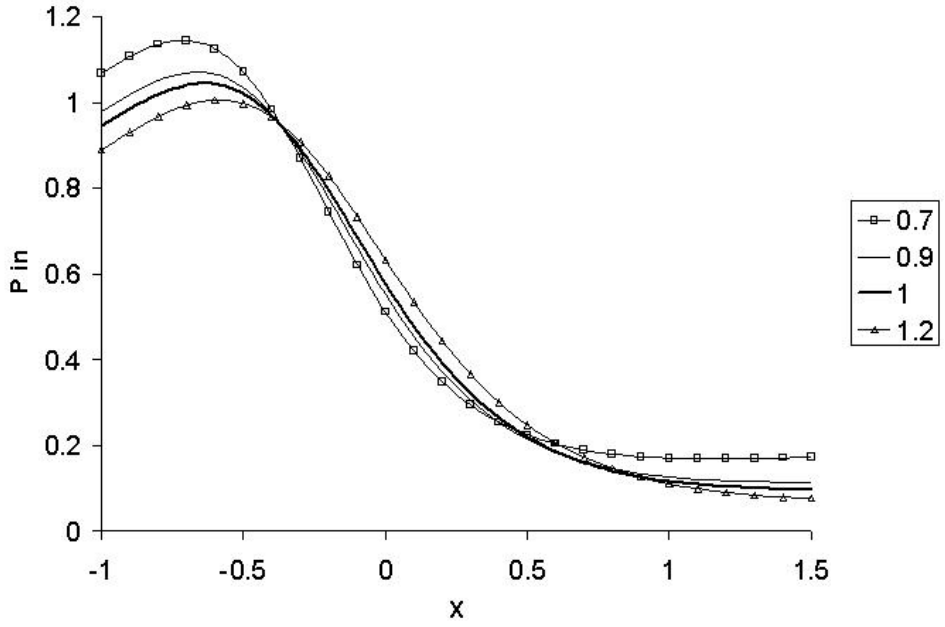

Figure 3.8: Input power frequency response (with c as a parameter)

which combined with (3.105) means

$$\frac{1}{2\pi f_{\mathrm{d}} C_1} \geq \frac{\pi^2 R}{2} \tag{3.120}$$

This is a known limit (see [35], where the limit was obtained by considering the voltage slope at the 'switch on' point). If the total capacitance at the drain exceeds the canonical Class E value by more than 10.4% then lossless operation is not possible for the usual case of 50% duty cycle. For a given capacitance and load, this imposes an upper frequency limit.

At lower capacitances (3.118) has two solutions. The one with smaller $|\phi|$ is usually of most interest to RF engineers, as this will be nearer the series resonance of the output circuit and gives greater power under the usual voltage power supply conditions.

Too low capacitance (i.e. c high) will result in large voltage excursions [22] at the drain but provided that (3.118) can be satisfied then lossless operation is still possible. Raab speculated [4] that 'solid-state series-tuned Class C' power amplifiers might operate in a similar way to Class E. The present analysis seems to support this, although in most cases such amplifiers will probably be tuned for maximum output rather than maximum efficiency. This is considered in the next section.

The power level for 100% efficiency can be found from (3.109) and (3.118) by using the

trigonometric double angle formulae:

$$\cos^2\phi = \frac{1}{2}(1+\cos 2\phi) \tag{3.121}$$

$$\sin^2\phi = \frac{1}{2}(1-\cos 2\phi) \tag{3.122}$$

$$\cos 2\phi = \sqrt{1-\sin^2 2\phi} \tag{3.123}$$

Then the input power is given by

$$P_{\text{in}} = \frac{8V_{\text{dd}}^2}{(\pi^2+4)Rc}\left[\frac{8+(\pi^2+4)c+\sqrt{(\pi^2+4)^2c^2-16\pi^2}}{2\pi^2+(\pi^2+4)c-\sqrt{(\pi^2+4)^2c^2-16\pi^2}}\right] \tag{3.124}$$

This is plotted in Figure 3.9, together with the normalised frequency offset for zero loss (calculated by inverting (3.116)). It can be seen that the power level for lossless operation varies rapidly with c in the region of the canonical Class E solution $c = 1$, but more slowly elsewhere. As c increases (i.e. C_1 becomes smaller) the power increases. The frequency for lossless operation at first remains near $X = 0$ but then increases too. There are two points where lossless operation is possible at $X = 0$. One is the canonical $c = 1$ solution. The other occurs at about $c = 1.6$, and corresponds to Raab's second solution for shunt susceptance [22] of approximately $0.1144/R$.

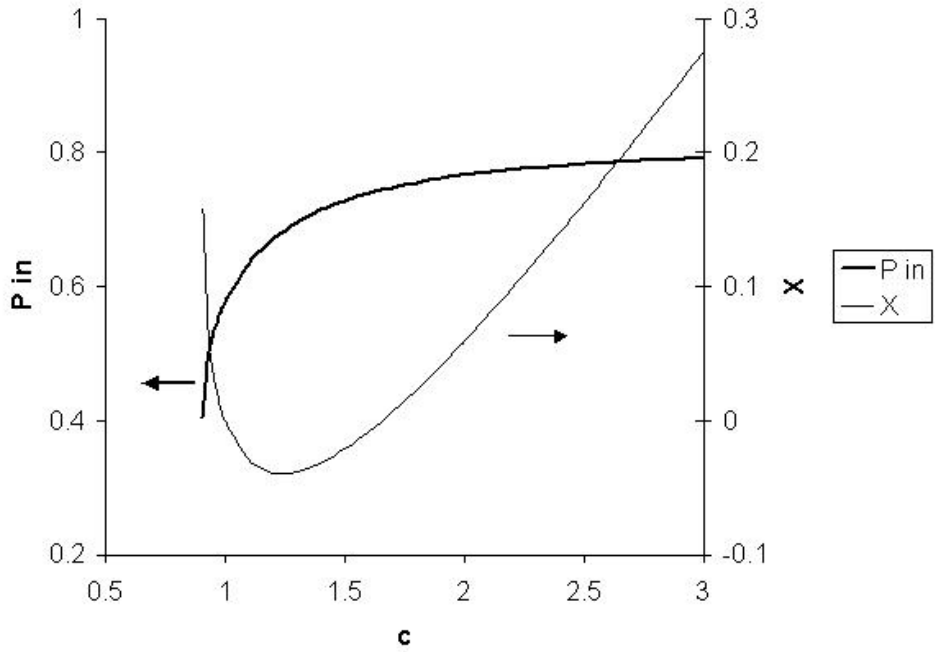

Figure 3.9: Input power and frequency for 100% efficiency as a function of c

3.2.6 Peak tuning

Power amplifiers are usually tuned for maximum output power, even if this degrades efficiency. The peak is found by differentiating (3.112) with respect to ϕ, and setting the result equal to zero. In practice the calculation is simplified by using the square root of (3.112), and remembering that only the numerator of the differential is required. The result is

$$\sin^2\phi - \frac{2\pi\sin\phi}{\pi\sin\phi + 2\cos\phi} - \frac{\pi^2}{c(\pi^2+4)} = 0 \tag{3.125}$$

This was solved numerically, and the resultant phase angle used with (3.116), (3.112) and (3.110) to give the results shown in Figure 3.10. This shows that quite good efficiencies are obtainable from peak tuning, provided that drain capacitance is rather smaller than the Class E value. This may often be the case if device internal capacitances are the main contributor to C_1. Comparing Figures 3.9 and 3.10, it can be seen that the difference in power level between peak efficiency and peak output reduces as C_1 becomes smaller.

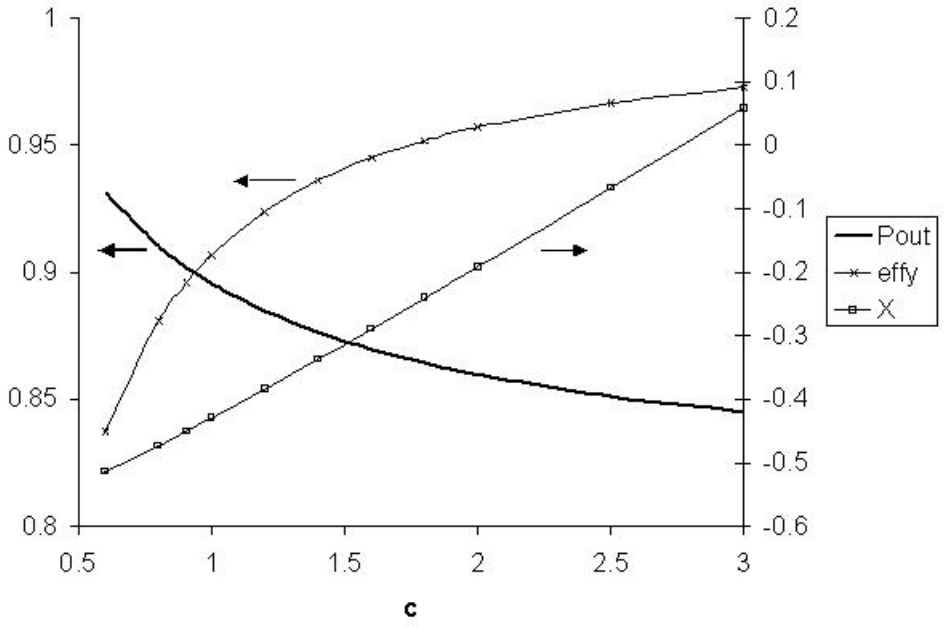

Figure 3.10: Peak output, efficiency and frequency as a function of c

The Class E circuit (Figure 3.1) may be considered to be representative of series-tuned Class C too, if C_1 is wholly provided by device capacitance. Thus high efficiency is possible with 50% duty cycle, unlike the classic parallel-tuned Class C which requires a short conduction angle. It is usually found that a shorter conduction angle produces a higher level of unwanted harmonics. It may be possible to reduce filtering requirements by remaining at 50% duty cycle and obtaining high efficiency by careful design based on the current analysis, but the issue of

harmonics has not been explored. It must be remembered that harmonic generation represents an additional loss mechanism.

Figure 3.10 assumes fixed load resistance R, and variable shunt capacitance C_1. In reality it may be that the shunt capacitance is fixed by device parameters, while the effective load resistance can be altered via a matching network. In this case higher c corresponds to lower R, and hence higher power until resistive losses become significant.

3.2.7 Implementation

A simple power amplifier was constructed to test the results of the power balance analysis. This operated at a frequency of 2MHz, in order to reduce the effect of device parasitic reactances.

Good agreement was achieved for the power frequency spectrum. Full details are given in Chapter 5.

3.3 Discussion

3.3.1 Power series solution

New expressions have been obtained, for component values and the central region of the power frequency spectrum of the Class E power amplifier, in the form of the first few terms of power series in Q^{-1}. These show good agreement with existing numerical solutions.

Under static conditions it is found that the drain feed choke L_1 simply acts as a lossless constant current source. Class E operation can be described fully by reference to the DC supply current alone, rather than the supply voltage. Energy storage in L_1 plays no part. However, the current through L_1 is such that the mean drain voltage becomes equal to the DC supply voltage. The insight that the Class E circuit could be regarded, under quasi-static conditions, as simply presenting a resistance to an incoming current led to the AM equivalent circuit analysis described in Chapter 4.

The techniques used in the power series analysis could be employed for other similar circuits such as the 25% duty cycle Class E doubler [36]. The main requirement is that simple power series expansions of trigonometric functions are available. This probably limits the method to switching points that occur at low integer sub-multiples of a complete cycle.

3.3.2 Energy balance analysis

By using conservation of energy new expressions for the high Q Class E circuit have been obtained. Combining these with published results from others gives the frequency response in the form of low order rational functions. This result, perhaps surprising, allows prediction of the response of high Q Class E power amplifiers, and at least provides a starting point for characterising lower Q circuits. It facilitates the design of wider band Class E power amplifiers and provides a firm basis for high efficiency Class E modulators. The absence of transcendental functions in the result allows for fast real-time evaluation: for example, in a DSP driving a modulator as part of an EER system.

The new analysis also exhibits the family of lossless solutions for the circuit in Figure 3.1, of which the standard Class E is a particular member characterised by 'soft switching'. This may assist the design of series-tuned Class C power amplifiers. It may be that 'series-tuned Class C' should be regarded as an amplifier class distinct from the classic low conduction angle parallel-tuned Class C, as it appears to have more in common with a detuned Class E circuit.

CHAPTER 4

CLASS E MODULATION

4.1 Introduction

4.1.1 Background

Under quasi-static conditions the Class E circuit exhibits linear AM characteristics via the DC supply, so it is a good candidate for Envelope Elimination and Restoration (EER) or other polar techniques. However, very little attention seems to have been paid to dynamic modulation behaviour of the ideal circuit.

A reasonably accurate prediction of the drain AM frequency response of a Class E PA is needed if polar modulation is to be employed. The effect of phase modulation of the gate drive must also be known. It is important to achieve equal time delays in the phase and amplitude channels, if signal distortion and spectral regrowth are to be avoided. These two channels may need a bandwidth which is many times higher than the original baseband signal. In addition, if negative feedback is used, then the issue of loop stability arises.

Kazimierczuk [30] considered the effect of the off-tune output circuit on AM. By making the simplifying assumption that the drain/collector voltage acts as a zero-impedance voltage source driving the output circuit, he obtained results for frequency response and non-linear envelope distortion. He then assumed that the effect of L_1 was to insert a single pole low pass (LP) filter in the modulation path. This ignores interactions between the DC feed and the output circuit, but is a good approximation when the value of L_1 is large. He obtained measurements which were consistent with his analysis, but they did not probe the boundaries of his model.

Polar modulation brings together the effects of both amplitude and phase modulation. Attempts have been made [31, 32] to predict the intermodulation distortion arising from polar modulation, but both of these made oversimplified assumptions (see Chapter 1) about the fre-

quency response of the amplitude and phase channels.

4.1.2 Current work

By considering the dynamic behaviour of the Class E circuit during drain amplitude modulation, it is possible to obtain an equivalent circuit (see Section 4.2) which models the frequency response, modulator load and excess dissipation of the power amplifier. This allows the design and simulation of the baseband part of a transmitter to be separated from that of the PA.

The effect of gate phase modulation was also considered. Some tentative conclusions were reached, but the analysis did not proceed as far as the AM work. A brief description of the phase analysis is given in Section 4.3, for the sake of completeness.

The expected intermodulation distortion arising from polar modulation has been calculated by using the technique described in [32], but using the AM frequency response theory described below instead of the single pole filter assumed by the original authors. This is briefly described in Section 4.4.

Early results from the AM work were presented at a conference [1]. A more detailed version, including the effect of carrier frequency, has been published as a journal paper [7].

4.2 Drain Amplitude Modulation

4.2.1 Low pass filters

There are two LP filters affecting modulation frequencies, but as will be seen below these interact to form a second-order filter. One LP filter comes from the finite Q of the output circuit C_2-L_2-R (Figure 1.3). The other is formed from L_1 and the effective DC resistance of the Class E circuit (see Chapter 3) as shown in Figure 4.1. The effective DC resistance is the ratio of the average drain voltage and the DC supply current.

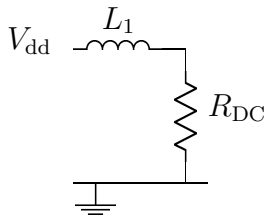

Figure 4.1: DC feed low pass filter

The drain voltage comes from the charge accumulated on shunt capacitance C_1 during the time the switch is open. A duty cycle of 50% at the design centre frequency will be assumed,

as this corresponds to the canonical analysis of the Class E circuit. The average drain voltage has two components, arising from the DC current through L_1 and the AC current in the output circuit. In the static case the AC current is proportional to the DC current and the net effect is as though a resistance of R_{DC} is present. Under ideal Class E conditions (i.e. high Q, correct component values, carrier at design centre frequency) this is given by (2.21) from Chapter 2:

$$R_{\mathrm{DC}} = \frac{\pi^2 + 4}{8} R = 1.7337R \tag{4.1}$$

This can be separated into components arising from the DC current through L_1 and the AC current in the ouput circuit:

$$R_{\mathrm{DC}} = R_{\mathrm{dc}} + R_{\mathrm{ac}} \tag{4.2}$$

The DC component of the average drain voltage is simply the mean value of the voltage arising from the DC current[1] I applied for half the time to C_1:

$$R_{\mathrm{dc}} I = \frac{I}{8 f C_1} \tag{4.3}$$

but the standard Class E analysis ((2.14) together with (4.1) above) gives

$$\frac{1}{2\pi f_{\mathrm{d}} C_1} = \frac{\pi(\pi^2 + 4)}{8} R \tag{4.4}$$

so provided that the carrier frequency f is near the design frequency f_{d}

$$R_{\mathrm{dc}} = \frac{\pi^2(\pi^2 + 4)}{32} R = 4.2887R \tag{4.5}$$

Then the AC-derived component is negative:

$$R_{\mathrm{ac}} = R_{\mathrm{DC}} - R_{\mathrm{dc}} = \frac{16 - \pi^4}{32} R = -2.5440R \tag{4.6}$$

The finite Q of the output circuit means that the AC amplitude lags behind changes in the DC current. The lag can be modelled by adding a (negative value) capacitor C_{Q} in parallel with R_{ac}, so that

$$\tau_{\mathrm{ac}} = R_{\mathrm{ac}} C_{\mathrm{Q}} \tag{4.7}$$

where τ_{ac} is the time constant of the AC (i.e. output) circuit. The equivalent circuit is shown in Figure 4.2. In this circuit L_1 is a real component; all the other components are modelling the behaviour of the switch and output circuit at modulation frequencies.

[1] I is used here rather than I_{DC} because, strictly, it is not DC but varies at baseband frequencies.

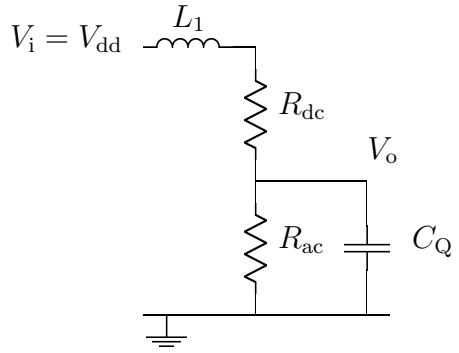

Figure 4.2: AM LP filter equivalent circuit

4.2.2 AC time constant

At first sight it might be thought that the AC time constant for the output circuit is given by (3.14) on page 3-4

$$\tau_\mathrm{ac} = \frac{2L_2}{R} = \frac{Q}{\pi f_\mathrm{d}} \tag{4.8}$$

where

$$Q = \frac{2\pi f_\mathrm{d} L_2}{R}$$

but this only takes account of power dissipated in the final load R. In addition, under dynamic conditions, the switch dissipates power because of stored charge in C_1. Under static conditions there is no stored charge at the end of the cycle because the supply current I exactly matches the required current I_0 set by conditions in the output circuit. This is no longer true under modulation. The excess voltage left at C_1 just before the switch closes is

$$V_\mathrm{sw} = \frac{I - I_0}{2fC_1} \tag{4.9}$$

so the extra power loss is

$$P_\mathrm{sw} = \frac{(I - I_0)^2}{8fC_1} = (I - I_0)^2 R_\mathrm{dc} \tag{4.10}$$

where (4.3) has been used. When calculating circuit time constants one may ignore voltage or current offsets. For a justification of this see Section D.2 in Appendix D. Thus for the purpose of determining dynamic behaviour (4.10) can be simplified to

$$P_\mathrm{sw} = I^2 R_\mathrm{dc} \tag{4.11}$$

In general, Q is given by

$$Q = 2\pi \frac{\textit{stored energy}}{\textit{energy dissipated per cycle}} \tag{4.12}$$

so

$$Q' = 2\pi f \frac{\frac{1}{2}L_2 I_{\rm AC}^2}{\frac{1}{2}RI_{\rm AC}^2 + I^2 R_{\rm dc}} \tag{4.13}$$

where Q' is the effective Q for the purpose of determining the behaviour under amplitude modulation, and $I_{\rm AC}$ is the circulating current in the output circuit. Then

$$\tau'_{\rm ac} = \frac{Q'}{\pi f} \tag{4.14}$$

If the circuit is operating in the high efficiency region then

$$R_{\rm DC} I^2 = \frac{1}{2} R I_{\rm AC}^2 \tag{4.15}$$

so

$$\begin{aligned} \tau'_{\rm ac} &= 2\frac{L_2}{R}\frac{R_{\rm DC}I^2}{R_{\rm DC}I^2 + R_{\rm dc}I^2} \\ \tau'_{\rm ac} &= \frac{\tau_{\rm ac}}{1 + (R_{\rm dc}/R_{\rm DC})} \end{aligned} \tag{4.16}$$

For the case of a Class E circuit operating at design centre frequency (4.1) and (4.5) give

$$R_{\rm dc} = \frac{\pi^2}{4} R_{\rm DC} \tag{4.17}$$

so $\tau'_{\rm ac}$ then simplifies to

$$\tau'_{\rm ac,0} = \frac{\tau_{\rm ac}}{1 + (\pi^2/4)} \tag{4.18}$$

Alternative derivation

It is possible to obtain (4.18) by a first-order calculation from the power series analysis described in Chapter 3. Assume that the circuit has been operating for some time with a constant supply current I_0. Then the charge and current at the end of the 'switch closed' period are given by (3.36):

$$\begin{aligned} y_0 &= \frac{I_0}{4f_{\rm d}}\left(-1 - b + \frac{\pi}{4Q}\right) \\ y'_0 &= -I_0\left(1 - \frac{\pi}{2Q} - \frac{\pi^2 b}{2}\right) \end{aligned}$$

The supply current is changed to I, and (3.41) is used to find the circuit current at the end of the 'switch open' period:

$$\begin{aligned} y'_1 &= \left(1 - \frac{\pi}{2Q}\right)(-y'_0 + 2\pi^2 a f_{\rm d} y_0) + \frac{IC_2}{C_1 + C_2}\left(2 - \frac{\pi}{2Q}\right) \\ y'_1 &= I_0\left(1 - \frac{\pi}{Q} - \frac{\pi^2}{2}(a+b)\right) + \frac{2IC_2}{C_1 + C_2} \\ y'_1 &= I_0\left(1 - \frac{\pi}{Q}\left(1 + \frac{\pi^2}{4}\right)\right) + I\frac{\pi}{Q}\left(1 + \frac{\pi^2}{4}\right) \end{aligned} \tag{4.19}$$

where (3.39), (3.40) and (3.42) have been used. It can be seen that this result is in the form of a first-order approximation to an exponential decay from I_0 plus a driving term in I. Comparing with (3.29) which is for half a cycle, one might expect a decay given by

$$1 - \frac{\pi}{Q} \tag{4.20}$$

but the decay rate is larger by a factor of $(1 + \pi^2/4)$ as shown in (4.18) above.

4.2.3 Frequency response

The output RF envelope is proportional to the voltage V_o at R_ac (Figure 4.2). Applying normal circuit theory gives

$$\frac{V_\mathrm{o}}{V_\mathrm{i}} = \frac{1}{1 + (R_\mathrm{dc} + j\omega L_1)(\frac{1}{R_\mathrm{ac}} + j\omega C_\mathrm{Q})} \tag{4.21}$$

Normalising to a low frequency gain of unity, and re-arranging the denominator:

$$\mathrm{gain} = \frac{1}{1 + j\omega(\frac{L_1}{R_\mathrm{dc}+R_\mathrm{ac}} + \frac{R_\mathrm{dc}}{R_\mathrm{dc}+R_\mathrm{ac}} R_\mathrm{ac} C_\mathrm{Q}) - \omega^2 \frac{L_1}{R_\mathrm{dc}+R_\mathrm{ac}} R_\mathrm{ac} C_\mathrm{Q}} \tag{4.22}$$

This can be rewritten using time constants as

$$\mathrm{gain} = \frac{1}{1 + j\omega(\tau_\mathrm{dc} + \frac{R_\mathrm{dc}}{R_\mathrm{DC}} \tau'_\mathrm{ac}) - \omega^2 \tau_\mathrm{dc} \tau'_\mathrm{ac}} \tag{4.23}$$

where

$$\tau_\mathrm{dc} = \frac{L_1}{R_\mathrm{DC}} \tag{4.24}$$

This is a second order LP filter with corner frequency and Q given by

$$\omega_\mathrm{m} = \frac{1}{\sqrt{\tau_\mathrm{dc} \tau'_\mathrm{ac}}} \tag{4.25}$$

$$\frac{1}{Q_\mathrm{m}} = \sqrt{\frac{\tau_\mathrm{dc}}{\tau'_\mathrm{ac}}} + \frac{R_\mathrm{dc}}{R_\mathrm{DC}} \sqrt{\frac{\tau'_\mathrm{ac}}{\tau_\mathrm{dc}}} \tag{4.26}$$

For the ideal Class E case, at centre carrier frequency, (4.17) applies so Q_m has a broad peak such that

$$Q_\mathrm{m} \leq \frac{1}{\pi} \tag{4.27}$$

with equality occuring if

$$\frac{\tau_\mathrm{dc}}{\tau'_\mathrm{ac}} = \frac{\pi^2}{4} \tag{4.28}$$

If the two LP filters acted independently then Q_m would instead have a peak value of 0.5 when $\tau_\mathrm{dc} = \tau'_\mathrm{ac}$.

A simplistic calculation based on output circuit Q (thus ignoring excess switching loss during modulation) and independent LP filters (ignoring interaction) would underestimate the corner frequency, and overestimate the Q, of the modulation frequency response. However, these two errors would to some extent compensate for each other at lower modulation frequencies. A simple calculation would provide a useful first step for checking a design, or might be sufficient in uncritical situations.

Single pole equivalent

At low frequencies a low Q second order LP filter behaves like a single pole filter, with the corner frequency given by $\omega_{\rm equiv} = \omega_{\rm m} Q_{\rm m}$. So combining (4.25) and (4.26):

$$\omega_{\rm equiv} = \frac{1}{\tau_{\rm dc} + \dfrac{R_{\rm dc}}{R_{\rm DC}} \tau'_{\rm ac}} \tag{4.29}$$

$$= \frac{1}{\tau_{\rm dc} + \dfrac{\tau_{\rm ac}}{1 + (R_{\rm DC}/R_{\rm dc})}} \tag{4.30}$$

$$\omega_{\rm equiv} \simeq \frac{1}{\tau_{\rm dc} + 0.7\tau_{\rm ac}} \tag{4.31}$$

A naive calculation would have replaced the 0.7 in the denominator by unity. This confirms that ignoring excess switching losses and filter interaction are reasonable approximations when only low modulation frequencies are used, or when $\tau_{\rm dc}$ dominates (i.e. large L_1).

On the other hand, if $\tau_{\rm dc}$ is small or can be eliminated (e.g. by using extra active devices as current shunts [37]) then (4.31) suggests that the AM bandwidth of Class E is about 1.4 times larger than might be expected from considering the output circuit Q alone.

4.2.4 Alternative equivalent circuit

Figure 4.2 models the impedance seen by the modulator and gives the modulation frequency response, but it contains negative value components. An alternative circuit is shown in Figure 4.3. This uses normal components. It also separates power in the load R_1 from switching losses in R_2.

The component values are given by

$$\begin{aligned} R_1 &= R_{\rm DC} \\ R_2 &= R_{\rm dc} \\ CR_1 &= \frac{L}{R_2} = \tau'_{\rm ac} \end{aligned} \tag{4.32}$$

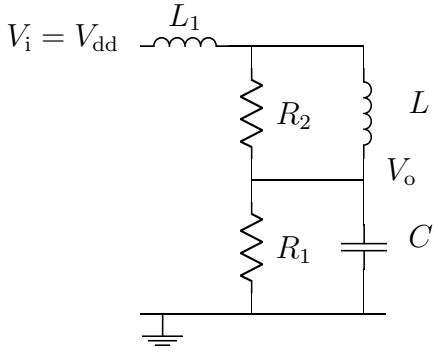

Figure 4.3: AM LP filter alternative equivalent circuit

All the equivalent circuit parameters depend on the carrier frequency, but R_dc varies sufficiently slowly when compared to R_DC and τ'_ac that it can be regarded as constant for operation near the design centre frequency.

Although at first sight Figure 4.3 looks like a third-order circuit, the two loops have the same time constant so the result is a second-order response.

Excess dissipation

At low modulation frequencies the modulator load is just R_1 and there is little dissipation in the switch. At high modulation frequencies most of the modulator power is lost in the switch, represented by R_2. The voltage developed across R_2 is given by

$$\frac{V_\mathrm{R2}}{V_\mathrm{i}} = \frac{j\omega \frac{R_\mathrm{dc}}{R_\mathrm{DC}} \tau'_\mathrm{ac}}{1 + j\omega(\tau_\mathrm{dc} + \frac{R_\mathrm{dc}}{R_\mathrm{DC}}\tau'_\mathrm{ac}) - \omega^2 \tau_\mathrm{dc}\tau'_\mathrm{ac}} \tag{4.33}$$

which can be compared to (4.23). The peak voltage, and hence the worst case for excess switch dissipation due to modulation, occurs at a frequency of ω_m – see (4.25). Then

$$\frac{V_\mathrm{R2}}{V_\mathrm{i}} = \frac{R_\mathrm{dc}}{R_\mathrm{DC}} Q_\mathrm{m} \sqrt{\frac{\tau'_\mathrm{ac}}{\tau_\mathrm{dc}}} \tag{4.34}$$

For ideal Class E conditions at the centre carrier frequency (4.17) applies, and Q_m is likely to be around $1/\pi$ (4.27), so

$$\frac{V_\mathrm{R2}}{V_\mathrm{i}} \simeq \frac{\pi}{4} \sqrt{\frac{\tau'_\mathrm{ac}}{\tau_\mathrm{dc}}} \tag{4.35}$$

If (4.28) is approximately true, then

$$\frac{V_\mathrm{R2}}{V_\mathrm{i}} \simeq \frac{1}{2} \tag{4.36}$$

This voltage is developed across $R_2 \simeq \pi^2 R/4$ (4.17) so for normal 100% AM (i.e. no preemphasis) the extra dissipation will be $1/(2\pi^2)$ (about 5%) of the DC input power.

If L_1, and hence τ_{dc}, have particularly low values then

$$\frac{V_{R2}}{V_i} \simeq 1 \tag{4.37}$$

and the extra dissipation will be $2/\pi^2$ (i.e. 20.3%) of the DC power. This could create difficulties unless taken into account during thermal design of the PA. It also implies that any attempt to achieve very fast AM with Class E [37] will degrade its high efficiency.

4.2.5 Practical difficulties

An equivalent circuit (Fig. 4.3) has been obtained which models the AM behaviour of a Class E power amplifier. From this the frequency response, modulator load and excess switch dissipation can be calculated. The problem is that, for a real PA design, some of the relevant input parameters for the model are likely to be poorly defined.

A significant fraction (or possibly all) of C_1 will be contributed by device parasitic capacitance. This is subject to manufacturing spreads, and will include some non-linearity. The value and degree of linearity of C_1 affects both R_{dc} and R_{DC}. An effective (i.e. linear equivalent) value can be used, however. The excess switch dissipation depends on the low voltage value of C_1, which is likely to be somewhat higher than the linear equivalent value across the whole drain voltage range.

One of the peculiarities of Class E is that R_{DC} (and hence the power level) varies considerably across the carrier frequency range. This affects both τ'_{ac} and τ_{dc}, and hence ω_m and Q_m. However, in the case of ω_m the changes in the time constants tend to operate in opposite directions so the main effect is a variation of Q_m with carrier frequency. New expressions for the carrier frequency response have been obtained (Chapter 3), but these still rely on a knowledge of the exact centre frequency. Unlike other amplifier types, the Class E centre frequency is marked by a peak in efficiency rather than power so is in practice poorly defined.

In some cases it may be necessary to measure R_{DC} and drain efficiency for a range of carrier frequencies. If the value of C_1 is not known, then R_{dc} can be estimated by using $(\pi^2/4)R_{DC}$ at the carrier frequency which gives highest drain efficiency. Other parameters, such as the value of L_1 and the Q of the output circuit, will usually be fairly well defined by component values.

4.3 Gate Phase Modulation

Phase modulation may be applied to a Class E power amplifier via the gate signal. Under static or quasi-static conditions the output signal phase is directly controlled by the gate phase, apart

from a phase shift which depends on the carrier frequency.

Under dynamic conditions the output phase modulation will lag the gate phase modulation because of the memory effect in the output tuned circuit. As a first step in modelling, this can be considered to be acting as a first order filter at modulation frequencies. When modelling AM behaviour above, it was found that extra switching losses meant that the output circuit was much more highly damped than might be expected; a factor of 3.5 is typical. Is there a similar effect for PM?

One of the features of Class E operation is that the net current charging the drain shunt capacitor is zero at the point the switch closes. This ensures that the capacitor voltage remains near zero even if the switch time varies a little, thus allowing the use of slow switching devices. A change in switch time is equivalent to a shift in phase so PM should not give rise to extra switch losses. Another way of looking at this is to remember that PM is simply the integral of frequency modulation (FM), and Class E efficiency remains high for carrier frequencies near the design centre frequency. The initial expectation is that the bandwidth, or delay time constant, resulting from the output circuit can be simply determined from the design frequency and circuit Q:

$$\mathrm{bw}_{\mathrm{PM}} = \frac{f_{\mathrm{d}}}{2Q} \tag{4.38}$$

and

$$\tau_{\mathrm{ac}} = \frac{Q}{\pi f_{\mathrm{d}}} \tag{4.39}$$

However, a change in carrier frequency causes a change in power i.e. a change in DC supply current for a given DC supply voltage. This is because the phase of the AC current depends on frequency, and the AC phase in turn affects the voltage developed on the drain shunt capacitor. Under quasi-static conditions all that happens is that the supply current through the drain feed choke adjusts itself so that the mean drain voltage matches the supply voltage. Under dynamic conditions the incoming supply current and the circulating output current may be temporarily out of balance, and this can give rise to extra switch dissipation. This is the same effect as was seen for AM, but for a different reason. In addition, this can cause transient PM-to-AM distortion.

A further complication arises because the ratio of DC to AC current depends on carrier frequency. This means that under dynamic PM conditions, the AC current (decaying due to dissipation in the load) and the DC current (replenishing the lost energy) are, in effect, operating from different bases. This can modify the effective time constant/bandwidth, depending on

which direction the phase is changing. Thus a non-linearity is introduced; inverting the input PM does not exactly invert the output PM.

Finally, the output circuit is operating 'off-tune' in Class E. This means that when changes occur, the exponentially decaying transient and the forced signal are at different frequencies. Their relative phase will shift – in phasor terms, the transient rotates as it dies. This can cause beats to occur, and may be another source of non-linearity.

Thus the behaviour of a Class E PA undergoing phase modulation is more complicated than at first appears. It was hoped that some progress could be made by considering the effect of changing carrier frequency. The general shape of the power spectrum was known from numerical results (e.g. [23]), and the central region near the design frequency had been found from the power series analysis (first part of Chapter 3) but no expressions were known for a wider bandwidth. At first it was hoped that an approximation (or at least some bounds) could be found by considering energy conservation at particular points such as maxima and minima, but it became apparent that this approach could give the whole spectrum and in a surprisingly elegant form. The result appears in Chapter 3.

It was hoped that something analogous to the AM equivalent circuit analysis could be carried out for PM, but this has not been possible. In the absence of an analytic approach, a spreadsheet was developed which attempted to incorporate the phenomena outlined above, and predict the outcome of PM and PM-to-AM. In effect, this treated the output circuit as two separate low pass filters handling I and Q signals respectively, with the I circuit reacting back on the supply current via the drain shunt capacitor. The magnitude of the supply current varied with the instantaneous frequency at the gate, using the results of the energy conservation model developed in Chapter 3. The results were encouraging, in that the general shape of the plots were similar to the measured data, but it was not possible to achieve good agreement as there remained significant timing errors. For example, see Figure 4.4, which compares the spreadsheet model with measured amplitude data (Section 5.4.3 in Chapter 5) resulting from a 90° phase change – the time axis shows elapsed time since the input phase transition.

In order to proceed any further with this analysis, it is necessary to find a method for estimating the effective Q of the output circuit and hence the AC time constant. However, it has been demonstrated that an even an ideal Class E circuit suffers from significant transient PM-to-AM effects.

To sum up, phase modulation of Class E can be considered in three baseband frequency zones, set by the drain supply frequency response:

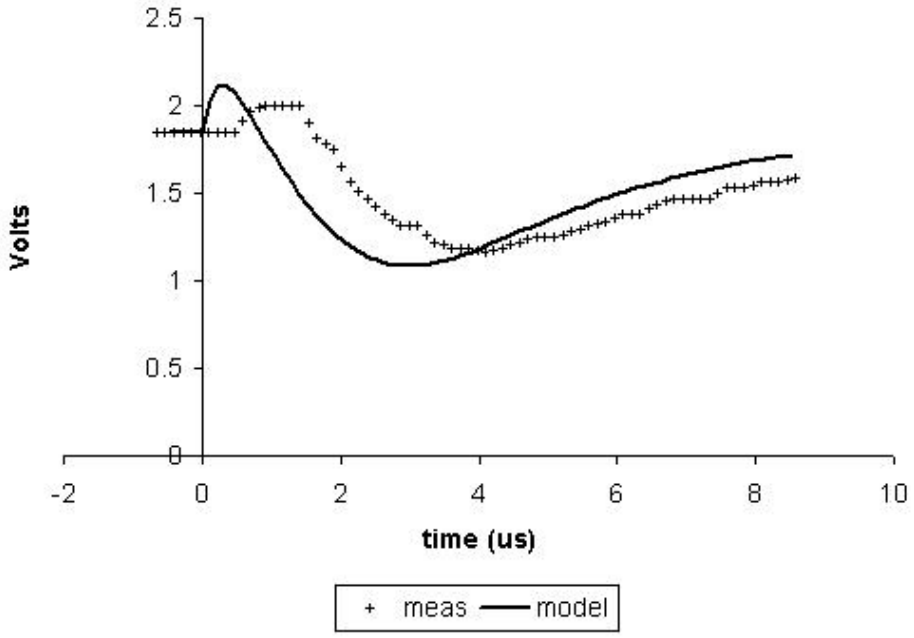

Figure 4.4: PM-to-AM for 90° phase change: model vs. measurements

low Slow PM can be treated by using the time differential of the baseband signal as FM.

mid At intermediate frequencies it is necessary to take into account the effect of the output circuit on the drain supply current.

high Very fast PM does not give time for the drain choke current to vary, so one simply has to consider the 'off-tune' output circuit although it is unclear what the effect of extra switch damping may be.

The various effects described above are likely to be less important than the extra damping which takes place during AM. It is expected that (4.38) and (4.39) should provide approximate predictions for circuit behaviour. For example, a step change in phase of 180° at the input should appear at the output after a delay of no more than

$$\tau_{\text{step}} = \ln 2\, \tau_{\text{ac}} = 0.693\, \tau_{\text{ac}} \tag{4.40}$$

4.4 Polar Modulation

Polar modulation needs both the amplitude and phase of the required signal to be set, via the drain bias supply and gate drive signals respectively. The details of the resultant output signal,

in particular the levels of unwanted intermodulation products, then depend on the frequency response of the amplitude and phase channels.

In [32] Milosevic et al assumed that the amplitude channel behaves as a single pole low pass filter, determined by the drain feed inductor and the effective DC resistance of the power amplifier. As has been demonstrated above, the Class E PA behaves as a double pole LP filter. At low baseband frequencies a single pole equivalent filter may be considered as a useful approximation, but with a corner frequency which depends to some extent on the Q of the output circuit. The authors assumed that the phase channel has infinite bandwidth.

The phase channel also behaves as a low pass filter, and there are subtle interactions between the two modulation channels. In the absence of a detailed model, what can be achieved?

It was decided to use the mathematical model from [32], but with the following assumptions:

- The amplitude channel has the frequency response given by the analysis of Section 4.2.
- The phase channel has two effects: a time delay given by (4.40), and an overall first order bandwidth restriction given by (4.38) which is applied to the resultant signals at the end of the calculation.
- The two channels are independent.
- Other components (such as RF decoupling, impedance matching) merely add a time delay to the relevant channel.

The first and last assumptions are likely to be reasonably valid, the second one may be only qualitatively correct, while the third assumption may be approximately true for sufficiently low modulation frequencies.

A spreadsheet was constructed to perform the calculation. The results are given in Chapter 5, and compared with measurements. It appears that other distortion mechanisms may be swamping the effects of finite amplitude and phase channel bandwidths.

4.5 Conclusion

It has been shown that the feed choke and finite output circuit Q of a Class E power amplifier combine to form a second order low pass filter for drain amplitude modulation. Expressions for filter corner frequency and Q have been derived, which take account of the effect of carrier frequency. An equivalent circuit allows easy calculation of modulator load, frequency response

and excess switch dissipation during fast AM. This facilitates the design of polar modulation systems, including those employing a feedback loop. Good agreement with measured data is seen (see Chapter 5).

A full theory of Class E gate phase modulation has not been obtained, but some of the likely complications have been identified. Key predictions are that there will be transient PM-to-AM effects, and that these will give rise to some extra output circuit damping (but this is expected to be much less significant than for AM). In addition, some asymmetry of response is expected between advancing and lagging phase changes. Measurements provide qualitative confirmation of these predictions.

Some thought has been given to polar modulation, and calculations made using more realistic assumptions than are currently available in the literature.

CHAPTER 5

LOW FREQUENCY IMPLEMENTATION

5.1 LF Power Amplifier and Modulator

A frequency of 2MHz was used for this implementation, in the expectation that near-ideal behaviour would result. This allows for comparison with theoretical predictions, without too much disturbance from device parasitic capacitance and finite switching time.

In outline, the circuit consisted of gate drive logic, the PA itself, and a modulator. The gate logic simply converted the carrier from an RF signal generator into a square wave. The PA was very similar to the skeleton circuit shown in earlier chapters, except for the presence of RF decoupling components. The modulator consisted of an operational amplifier, augmented by an emitter follower. Full details of the circuit are given in Appendix C.

Figure 5.1 gives a partial circuit diagram, showing the PA and decoupling components. The loss resistance of the output inductor L_5 was measured and regarded as part of the load.

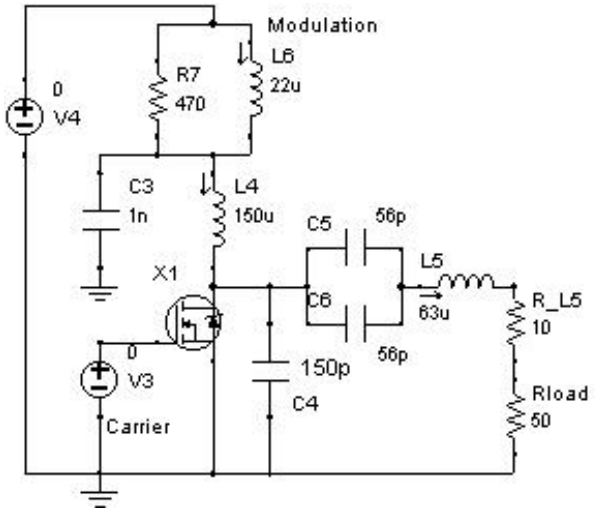

Figure 5.1: 2MHz Class E power amplifier

5.2 Steady-State Measurements

5.2.1 Carrier frequency response

The carrier frequency response was measured. The raw data is shown in Table 5.1; note that in this and Table 5.3 below the final column giving efficiency includes a correction for the loss resistance of L_5. The results were normalised to a load of 1Ω and DC supply of 1V. The measured response is shown in Figures 5.2 and 5.3, together with the best fit calculation obtained from the energy conservation analysis (Chapter 3).

freq MHz	V_{dd}	I_{DC} mA	P_{in} mW	R_{DC} Ω	$V_{pk\text{-}pk}$	P_{out} mW	efficiency %
1.90	6.00	102	612	58.8	3.516	309	60.6
1.92	6.00	104	624	57.7	3.828	366	70.4
1.94	6.01	103	619	58.3	4.094	419	81.2
1.96	6.01	95.6	575	62.9	4.094	419	87.5
1.98	6.01	82.2	494	73.1	3.875	375	91.1
2.00	6.02	66.0	397	91.1	3.516	309	93.4
2.02	6.02	50.6	305	119	3.078	237	93.2
2.04	6.03	38.3	231	157	2.719	185	96.1
2.06	6.04	29.5	178	205	2.375	141	95.0
2.08	6.04	23.5	142	257	2.109	111	93.8
2.10	6.04	19.9	120	304	1.890	89	89.0

Table 5.1: 2MHz PA: carrier response (raw data)

The fit was improved by including some DC loss resistance in series with the power supply; this provides an approximate model for losses in the feed choke (L_4 in Figure 5.1) and the effect of finite switch resistance. The best fit parameters are compared with the original design intent in Table 5.2. The most significant difference is that the drain shunt capacitance is larger than expected.

parameter	design	best fit
centre frequency	2.0MHz	2.018MHz
Q	13.3	14.4
shunt capacitance ratio c	1 (i.e. Class E)	0.788
loss resistance	zero	0.0425Ω

Table 5.2: 2MHz PA: design vs. best fit

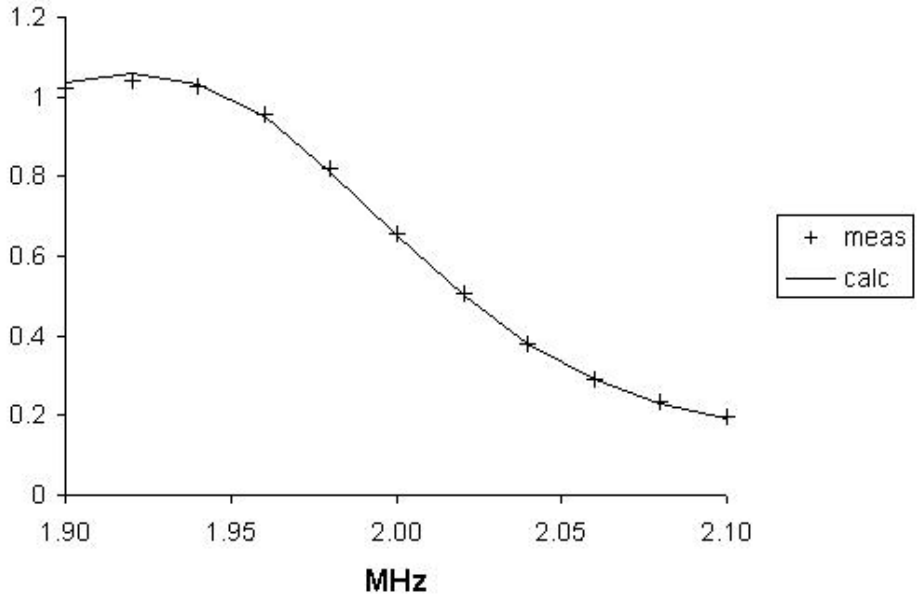

Figure 5.2: 2MHz PA: normalised power input

The design centre frequency and Q were determined by measuring the series impedance of the output circuit L_5-C_5 at and near resonance, and assuming that C_5 and C_6 (silver mica) correspond to their marked value. Approximately half of the shunt capacitance was contributed by the drain capacitance taken from the device data sheet; this is likely to have quite a wide tolerance. The agreement between measurement and calculation is quite good, given the uncertainties inherent in real circuits.

5.2.2 Static amplitude modulation

The variation of RF output power with supply voltage was measured. Raw data is shown in Table 5.3. It shows, as expected, a linear response down to quite low voltages. It can be seen that both R_{DC} and drain efficiency are almost independent of supply voltage.

The measurements do show a small rise in both R_{DC} and efficiency at low bias voltages. This could be due to measurement error. However, it is also possible that both effects arise from gate–drain feedthrough due to device capacitance (see Section 5.5.2 below). A current injected into the drain circuit from the gate could increase the amplitude of the AC current, thus increasing the output power, and modify the AC phase so that the input power was reduced. Such an effect would be more significant at low drain bias voltages.

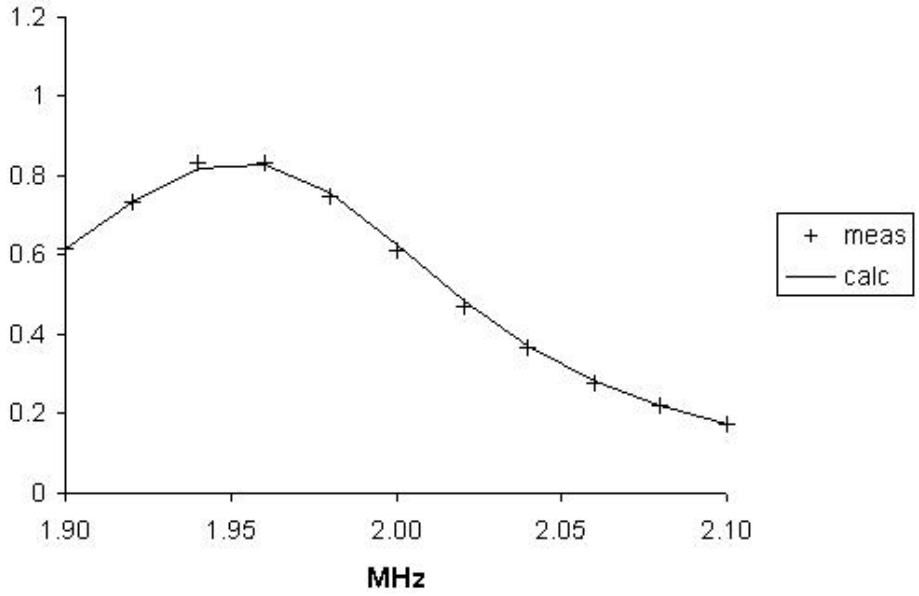

Figure 5.3: 2MHz PA: normalised power ouput

freq MHz	V_{dd}	I_{DC} mA	P_{in} mW	R_{DC} Ω	$V_{\text{pk-pk}}$	P_{out} mW	efficiency %
2.00	1.07	11.6	12.4	92.2	0.65	10.6	102.6
2.00	2.21	23.6	52.2	93.6	1.312	43.0	98.9
2.00	3.62	39.0	141	92.8	2.109	111	94.7
2.00	4.97	54.1	269	91.9	2.906	211	94.1
2.00	6.01	66.0	397	91.1	3.500	306	92.5
2.00	7.06	77.7	549	90.1	4.190	439	96.0
2.00	10.06	111.7	1124	90.1	5.937	881	94.1

Table 5.3: 2MHz PA: static AM response (raw data)

5.3 Dynamic Amplitude Modulation

5.3.1 Modulation frequency response

The AM frequency response was measured at three carrier frequencies: 1.96, 2.0 and 2.04MHz. A high speed digital oscilloscope was used to view the modulation input and RF output envelope waveforms. The voltages at the envelope maxima and minima give the modulation index and hence AM gain, while the corresponding times allow calculation of the AM phase. The measured results (Figs 5.5 and 5.6) were compared with Spice simulations of the equivalent circuit (e.g. Fig. 5.4, which includes RF decoupling components). The parameters used to calculate the equivalent circuit were taken from the measured carrier frequency response – see Section 5.2.1.

The overall carrier response was used to obtain the actual shunt capacitance ratio (see Table 5.2) and hence determine $R_{\rm dc}$:

$$R_{\rm dc} = 0.788\frac{\pi^2(\pi^2+4)}{32}60 = 202\Omega \tag{5.1}$$

The carrier frequency response also gives a Q of 14.4, slightly higher than the design value of 13.3. The measured DC resistance at each carrier frequency was then used to calculate the equivalent circuit parameters – see Table 5.4. The AM frequency response results show reasonable agreement with the equivalent circuit model.

carrier	$R_{\rm DC}$	$\tau_{\rm dc}$	$\tau'_{\rm ac}$	C	L	f_m	Q_m
1.96MHz	63Ω	$2.38\mu s$	$0.545\mu s$	8.65nF	$110\mu H$	140kHz	0.276
2.0MHz	91Ω	$1.65\mu s$	$0.712\mu s$	7.82nF	$144\mu H$	147kHz	0.336
2.04MHz	157Ω	$0.955\mu s$	$1.00\mu s$	6.37nF	$202\mu H$	163kHz	0.436

Table 5.4: 2MHz PA: AM equivalent circuit parameters

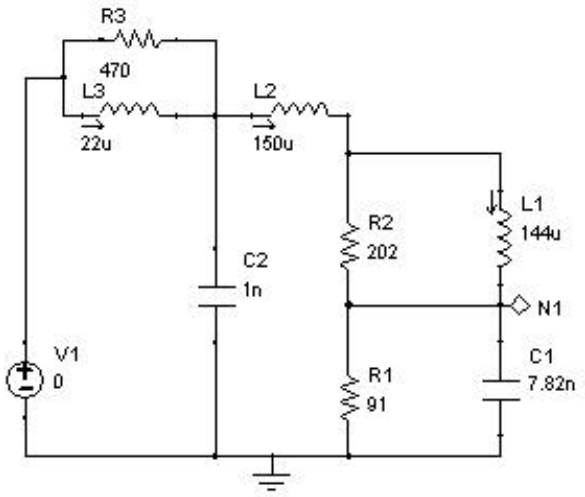

Figure 5.4: 2MHz PA: AM equivalent circuit (2MHz carrier)

5.3.2 Modulator load impedance

The impedance seen by the modulator was measured at a carrier frequency of 2.0MHz. This includes the effect of RF decoupling components. Results are shown in Figures 5.7 and 5.8, in the form of magnitude and phase. For the purposes of comparison, the graphs also show the expected impedance from a naive calculation, which assumed that the Class E PA simply retains its DC impedance for all modulation frequencies. There is good agreement between measurements and the model for impedance magnitude, but less so for phase. The rapid change

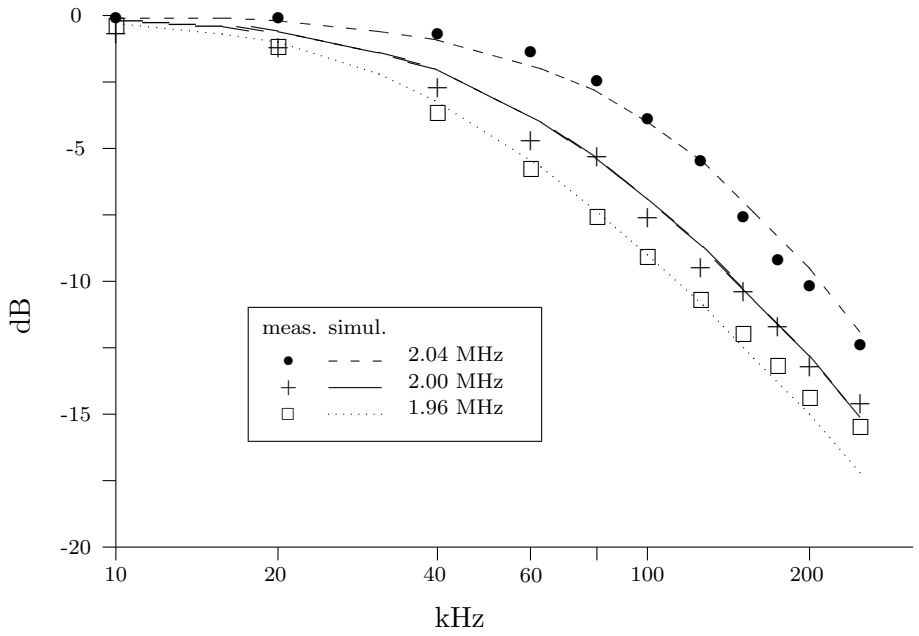

Figure 5.5: 2MHz PA AM frequency response: gain

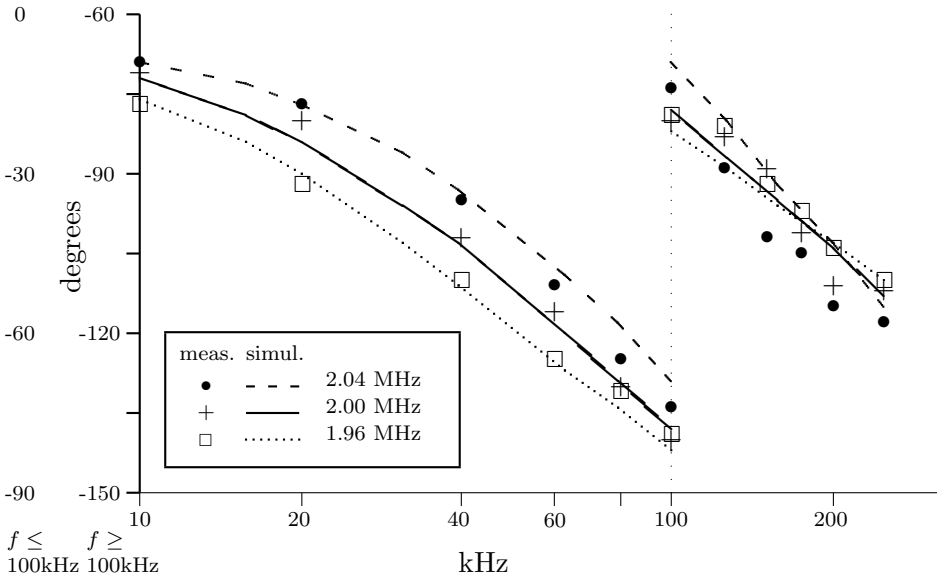

Figure 5.6: 2MHz PA AM frequency response: phase – with split y-axis to give some vertical expansion

of phase in the region of 300kHz is due to a resonance between the feed choke (150μH) and a decoupling capacitor (1nF). Some residual 2MHz RF reduced the accuracy of measurements at the higher modulation frequencies.

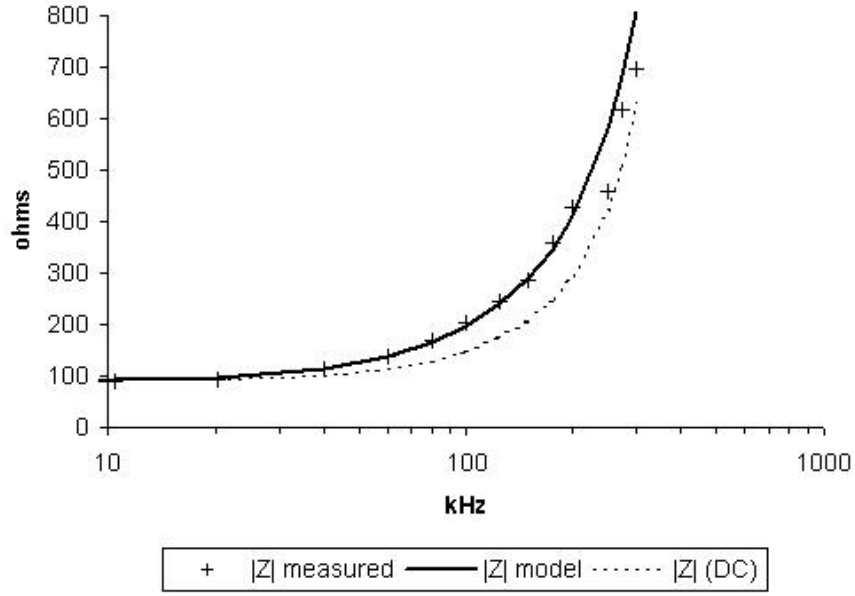

Figure 5.7: Modulator load impedance: magnitude

5.4 Phase Modulation

5.4.1 Phase modulator

A simple phase modulator was constructed using HCMOS logic. In order to provide a stationary display on a fast oscilloscope to view the results, the modulation frequency was derived by binary division of the carrier frequency i.e. $f_{\mathrm{m}} = f_{\mathrm{c}}/2^n$. The phase modulation could be switched between $0° - 90°$ and $0° - 180°$, although only the former was actually used as it enabled any differences between advancing and lagging phase to be studied.

The modulation was performed by a digital switch, but the modulated RF then passed through two low Q bandpass filters so the phase transition at the PA gate was delayed by 0.6μs, and had a rise time of about 1.1μs.

Details of the circuit are given in Appendix C.

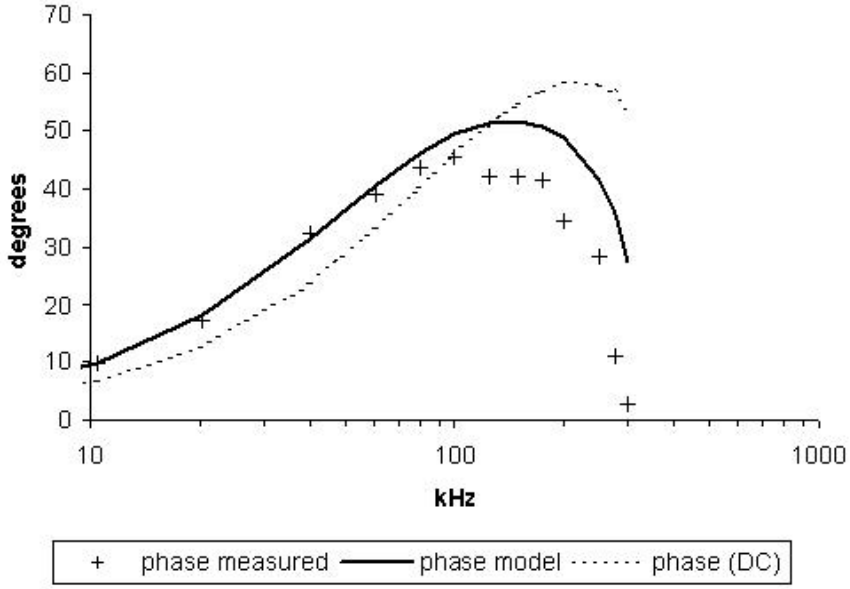

Figure 5.8: Modulator load impedance: phase

5.4.2 Phase modulation response

The RF phase was determined by measuring the relative times (with respect to the original logic transition) of the peaks and zero crossings of the RF signal at the phase modulator, PA gate, and PA output. Separate measurements were taken for the two polarities of transition, as the off-tune output circuit of Class E was expected to distinguish between them.

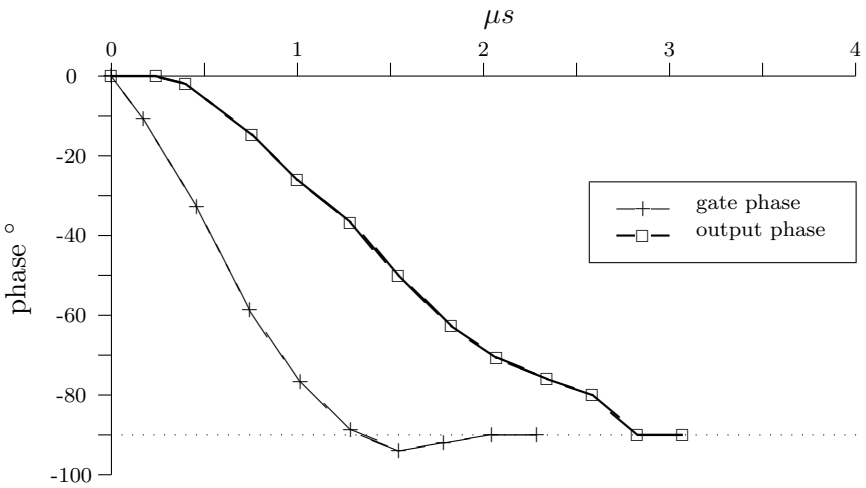

Figure 5.9: 2MHz PA: 90° phase lag response

The phase data is plotted in Figures 5.9 and 5.10. It can be seen that for the phase advance case the gate input phase seems to make limited progress beyond 80°; more data would be

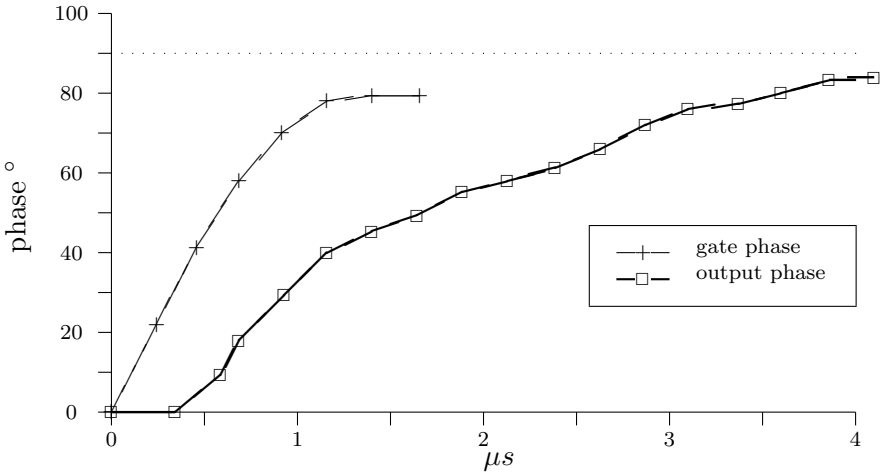

Figure 5.10: 2MHz PA: 90° phase advance response

useful here, but unfortunately this effect was not noticed until the raw timing measurements were analysed. Conversely, for the phase lag case there is a small overshoot. This could be caused by the gate circuit being slightly off-tune. Clearly the gate drive will eventually settle on 90°, if left long enough.

The output phase change also depends on direction. For phase advance it seems to shift quite rapidly at first, then more slowly. The phase lag measurements show a more linear variation. However, both cases show some weak evidence for beats.

The time delay for a step change derived from the measured data is compared in Table 5.5 with the predicted value (see (4.40) in Chapter 4) for a circuit Q of 13.3 at 2MHz. The result shows that there is significant extra damping, although not as much as for AM, but only a small difference due to the direction of the phase change.

phase advance delay	$0.84\mu s$
phase lag delay	$0.91\mu s$
predicted step delay	$1.47\mu s$

Table 5.5: 2MHz PA: phase step time delay

5.4.3 PM to AM

The amplitude data from the phase modulation measurements are plotted in Figure 5.11. Each phase change causes a large temporary change in amplitude, even though the circuit is operating

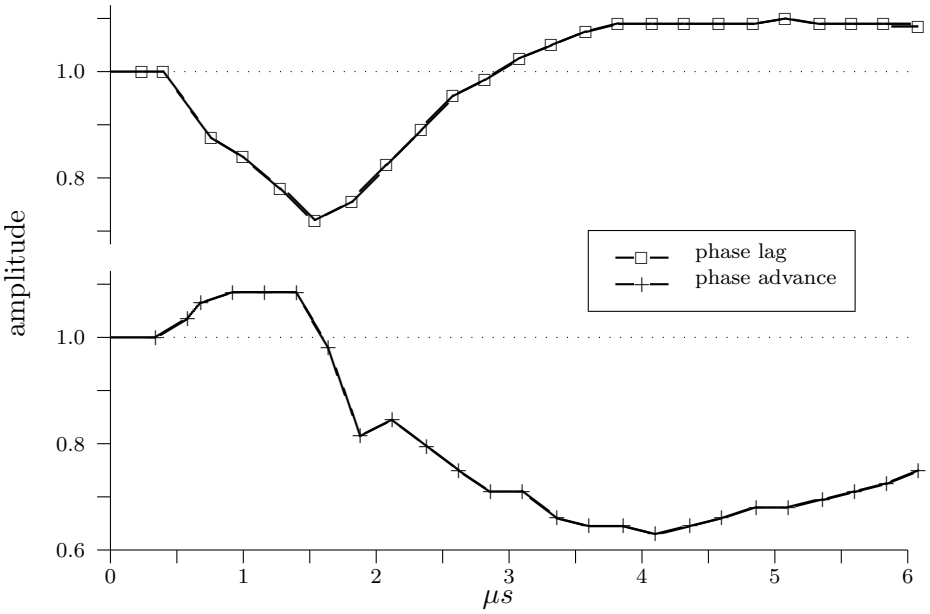

Figure 5.11: 2MHz PA: 90° phase change PM to AM

under near-ideal conditions. This seems to confirm that PM to AM distortion is inherent in the Class E architecture; see also Figure 4.4 which compares measured data with a model. The pattern of amplitude change depends on the direction of the phase change. These amplitude changes will cause extra switch losses and thus extra circuit damping; this is consistent with the phase step results above.

Amplitude changes due to a phase change will of course eventually die away, but seem to exhibit surprisingly long tails. The original raw data shows that by 8μs after a phase advance transition the amplitude had only recovered to about 80% of the pre-transition level. It is unclear why this is so because the drain feed time constant τ_{dc} is, like the AC time constant, in the region of 1-2μs. However, the reduced amplitude seems consistent with the relatively slow long term phase response seen in Figure 5.10; the incoming signal at the new phase is temporarily weaker than the reference level of the decaying transient. Conversely, the phase lag response has higher signal amplitude so achieves a quicker transition to the new phase.

5.4.4 Phase modulation spectrum

The central part of the spectrum resulting from 90° phase modulation is shown in Table 5.6, normalised to the carrier level. The baseband frequency was 15625Hz. It can be seen that the input spectrum from the modulator has only odd-order sidebands as expected, but the PA output includes even-order components. These arise from the asymmetric response shown in

the previous section.

component	expected	PA input	PA output
-5	-17.9 dBc	-18.2 dBc	-21.5 dBc
-4			-27.3 dBc
-3	-13.5 dBc	-13.7 dBc	-14.8 dBc
-2			-25.5 dBc
-1	-3.9 dBc	-4.0 dBc	-3.8 dBc
carrier	0 dBc	0 dBc	0 dBc
+1	-3.9 dBc	-4.0 dBc	-4.7 dBc
+2			-30.5 dBc
+3	-13.5 dBc	-13.5 dBc	-14.8 dBc
+4			-36.8 dBc
+5	-17.9 dBc	-17.8 dBc	-19.2 dBc

Table 5.6: 2MHz PA: 90° phase modulation spectrum

5.5 Polar Modulation

5.5.1 Polar modulator

A polar modulator was designed and constructed, to produce double-sideband suppressed-carrier modulation. The phase channel consisted of a comparator and a double-balanced mixer; the amplitude channel used a full-wave precision rectifier. The RF output from the phase channel provided gate drive for the 2MHz PA. The amplitude channel was used to replace the on-board modulator in the PA.

Full details of the circuit are given in Appendix C.

5.5.2 Intermodulation measurements

The aim was to measure the third order intermodulation distortion (IMD) as the baseband frequency was changed, and compare this with the level predicted by the outline theory described in Chapter 4. The initial results are shown in Figure 5.12.

It can be seen that there is little change of IMD level with baseband frequency. At low frequencies, where low IMD would be expected, the IMD remains high. At first it was thought that this might be caused by non-linear distortion in the PA amplitude modulation response (see Table 5.3). A little pre-distortion was tried, by adding an LED and series resistor connected across the feedback resistor R_{10} in the polar modulator (Figure C.4). No improvement was seen.

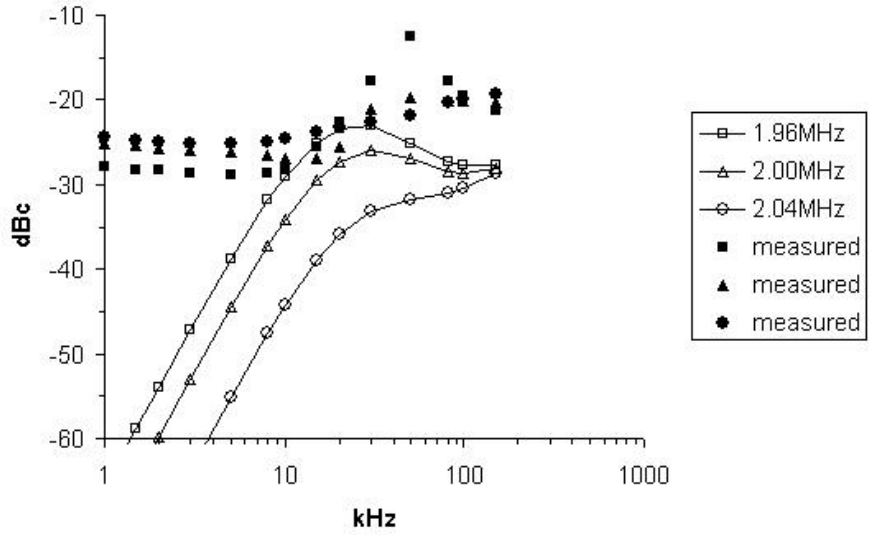

Figure 5.12: Polar IMD: initial results

It was then realised that a significant fraction of the IMD in the drain circuit could be caused by capacitive coupling from the gate. The gate drive is rich in odd order components, as it derives from square wave modulation (see Table 5.6, which is for a different but related situation). The gate-drain capacitance for the FET is non-linear, but according to the device data sheet could be expected to be in the region of 25pF to 100pF. It was decided to try to cancel this feedthrough signal by injecting it in antiphase into the drain. Accordingly, the PA circuit was modified by adding two extra gates and a capacitor – see skeleton circuit in Figure 5.13. Two parallel gates were used in order to match the gate drive circuit. The capacitor CX was adjusted and the IMD measured at a baseband frequency of 1kHz. It was found that significant improvement in IMD could be achieved as CX was increased.

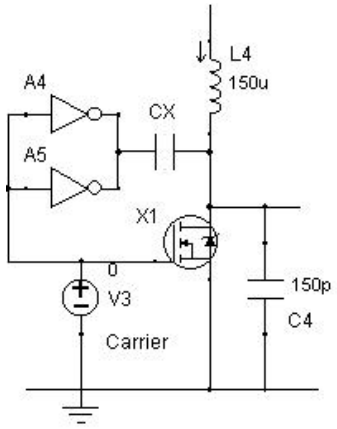

Figure 5.13: IMD cancellation circuit

However, the final value of 326pF for minimum IMD is significantly higher than can be justified from the likely range of values for the gate-drain capacitance of the FET. It seems that there are other distortion mechanisms in operation too. The IMD spectrum for this value of compensation capacitance is shown in Figure 5.14.

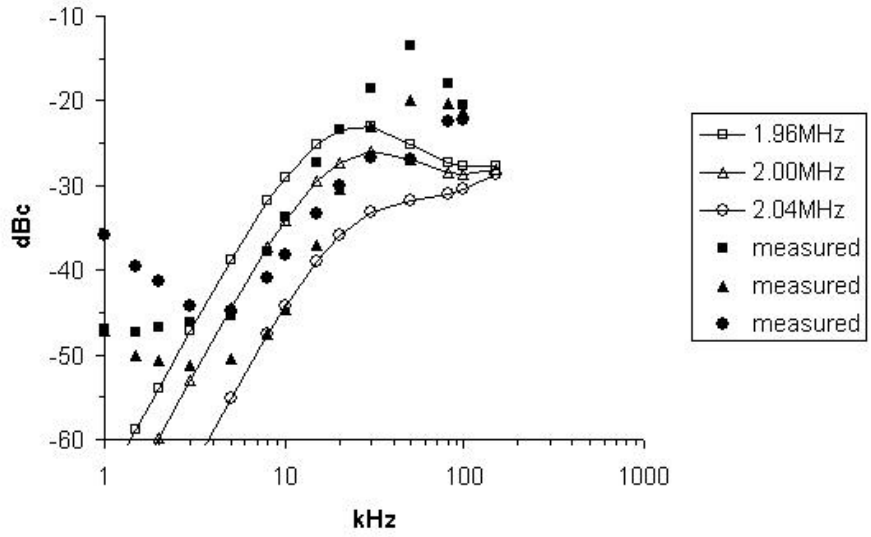

Figure 5.14: Polar IMD: optimum compensation

At low frequencies it is likely that the IMD is dominated by harmonics already present in the baseband sine wave signal, and non-linear distortion in the modulator and the drain modulation process in the PA. Although these effects should be small, the polar modulation process should have near-perfect cancellation of unwanted components in this region. Thus, the measured IMD should be much higher than the predicted level. This is seen.

In the middle region it is expected that IMD is dominated by the baseband phase and amplitude errors introduced by the finite bandwidth of the PA as it behaves as a second order low pass filter. The measured IMD should not be too different from that predicted. Although the general trend of the measured data is similar to the prediction, the levels differ by up to about 6dB and the measured level is generally lower than the prediction. Perhaps more significant is that the relative levels of IMD for different carrier frequencies are not as expected. This seems to confirm that there are other mechanisms at work.

In the upper region there is very little cancellation of unwanted components, and the IMD level is set by the overall RF bandwidth of the PA. This will depend on the level of damping imposed by excess switch loss, and so is unpredictable at present. Nevertheless, the measured data does show both a reduction in IMD at the highest baseband frequencies and a convergence of

level for the different carrier frequencies, as predicted. The data suggests that the RF bandwidth is higher than expected; this is consistent with the earlier phase modulation results.

Thus the measurements are approximately consistent (at least in the middle frequency region) with the theory developed thus far, but further work is needed. A set of measurements were taken with a compensation capacitance value of 82pF; this is about the highest value which can be justified from the device data sheet. The results are shown in Figure 5.15, and are quite similar to those with no compensation (Figure 5.12). It is conceivable that the device used has abnormally high internal capacitance. Although labelled IRF510, perhaps it is really an IRF520 or 530 (i.e. it contains extra device chips). Unfortunately a capacitance measurement would require a partial dismantling of the PA, so for this reason and time pressure it has not been attempted.

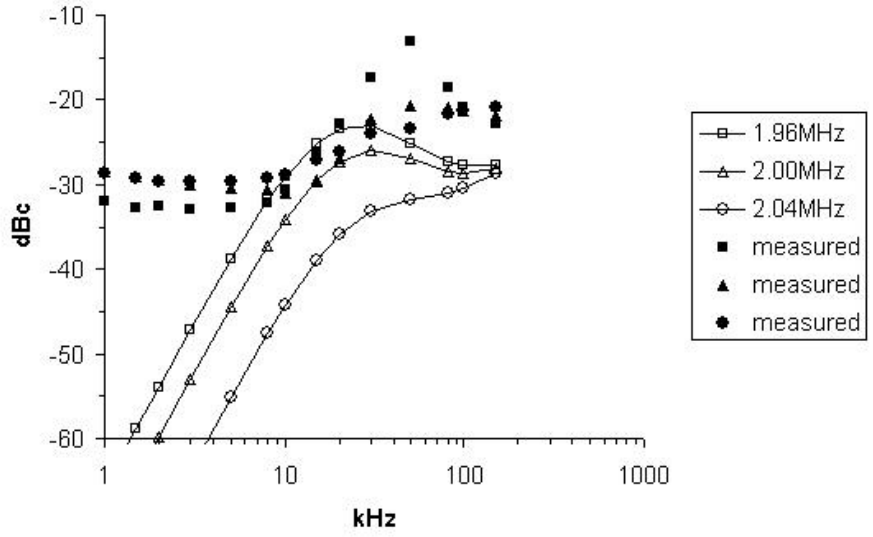

Figure 5.15: Polar IMD: 82pF compensation

5.6 Summary of Results

The earlier measurements of carrier and baseband frequency responses show good agreement with the quantitative steady-state and AM theory described in Chapters 3 and 4 respectively. Thus it is now possible to use this theory with confidence to design power amplifiers employing Class E.

The later measurements of phase and polar modulation were compared with more tentative qualitative theory, but even so show general characteristics which give some encouragement. It is clear that further work is needed in this area.

CHAPTER 6

CONCLUSIONS

6.1 Current Class E Project

6.1.1 Steady-state solutions

Two new analyses of steady-state operation of the Class E power amplifier have been presented in Chapter 3. They use different techniques and apply to different, but overlapping, domains characterised by circuit Q and normalised carrier frequency. Both analyses extend existing theoretical knowledge of the circuit and provide useful information for practising electronic engineers who wish to design a Class E amplifier.

The key findings from the first (power series) analysis are expressions for component values for finite Q circuits, and an estimate of the unwanted harmonic output. These were previously only known from numerical solutions at spot values of Q and frequency. The existence of the power series solution confirms that exact Class E conditions are possible for finite Q, but no longer coincide with peak efficiency. This analysis also gives expressions for the carrier frequency response, but for most purposes these are superseded by those obtained by considering energy conservation. Finally, the power series analysis gave rise to the insight that the role of the drain feed choke is simply to feed a current into the rest of the circuit; this then led to the amplitude modulation theory given in Chapter 4.

The significant results from the second (energy conservation) analysis are simple rational functions giving the frequency response of the Class E PA over the entire central region. This fills a long-standing knowledge gap, which may have seriously limited the practical usefulness of this circuit. Employing a circuit which is not peak-tuned is counter-intuitive for most engineers; especially if no frequency response formula is known. The carrier frequency response is an important input into understanding the behaviour of the circuit during phase modulation. This

work also provides a way to consider the effects of varying the drain shunt capacitance, which leads to high efficiency 'Class C' designs despite operating at 50% duty cycle.

The expressions from the first analysis provide results which agree with published numerical solutions. The findings of the second analysis agree with published solutions and measured data.

6.1.2 Modulation behaviour

It has been shown in Chapter 4 that the drain amplitude modulation behaviour of a Class E power amplifier can be modelled by an equivalent circuit. This includes real components (e.g. drain feed choke, RF decoupling), and virtual components (e.g. effective DC resistance) that model the baseband response of the switch and output circuit. The overall frequency response is that of a low Q second order low pass filter, with parameters which vary with carrier frequency. One important finding is that the output tuned circuit experiences considerable extra damping due to excess switch losses during modulation, thus widening the bandwidth at the expense of efficiency.

The equivalent circuit model for AM eases the design of transmitters. For example, a simulation can explore the operation of the modulator at baseband frequencies without having to simultaneously run a full PA model at carrier frequency. Theoretical studies of transmitter systems employing Cartesian or polar modulation may now use a more realistic model of PA amplitude modulation.

Measurements of AM frequency response and modulator load impedance confirm the model. Some work was done on phase and polar modulation, but further investigations are needed.

6.1.3 Publications

Four publications have arisen from this work. A summary of the steady-state power series analysis, together with early results from the AM modelling, were presented at a conference [1]. Full details of the power series analysis were subsequently published [5].

Papers describing the energy conservation analysis [6], and the AM equivalent circuit [7], have also been published. Copies of each paper are bound with this thesis.

6.2 Future Work

Possible future work falls into two categories: further exploration of Class E circuits, or using the techniques developed here to study other circuits.

6.2.1 Class E

There is clearly a need to understand the behaviour of the Class E amplifier during phase modulation, and then polar modulation. One possible approach is to develop the idea mentioned in Chapter 4: model the baseband behaviour as two orthogonal AM channels for I and Q, but with only changes in the I channel reacting back on the mean drain voltage. Under static conditions the output phase differs from the input phase, so there will be some mixing of the two channels which may perhaps be treated as a carrier frequency-dependent rotation in baseband phase space.

Although this work has studied the classic series-tuned Class E circuit, there are variants which can be considered using similar techniques. These include the dual circuit, parallel-tuned Class E [4], and related circuits such as the Class E frequency multiplier [36] or Class E rectifier [38].

6.2.2 Further applications

The power series technique could be used for other circuits which have a simple solution for high Q, but are more often employed at low Q. Possible application areas could include the various types of FM discriminator, and some oscillators.

The energy conservation technique could be used for circuits which in ideal form under ideal conditions are lossless, and have power input, output and losses which are easily calculable. A possible, but perhaps trivial, example is the choke-input DC power supply.

6.3 Finale

This project started as an investigation of efficient integrated transmitters/antennas employing the Class E architecture. It has taken several unplanned turns, and concludes with an investigation of Class E modulation. Along the way some interesting byways have been explored, and some unexpectedly elegant and useful results have emerged. It is hoped that this work will enable more widespread use of a clever invention, now that its properties are better understood.

To paraphrase the closing sentence of the Chancellor of the Exchequer, in his annual Budget Speech: 'I commend this thesis to the examiners!'

APPENDIX A

MATHEMATICS

A.1 Heaviside Operational Calculus

A.1.1 Brief history

Heaviside's operational calculus provides a method for solving linear differential equations, such as those that arise in circuit theory. Like the Laplace transform, which has largely replaced it, the operational calculus transforms the differential equation into an algebraic equation. The algebraic solution is then turned back into a function of time.

Heaviside developed his method in the 1880's [39], and used it successfully to solve engineering problems. Unfortunately his disdain for mathematicians and their rigour led him to take short cuts, and he was criticised for this. Although he almost always obtained the correct solution, this sometimes required the use of physical intuition to avoid mathematical difficulties. His contemporaries did not trust his method and believed that it had weak mathematical foundations. The subsequent development of the Laplace transform and inverse transform (Bromwich integral), based on contour integration in the complex plane, provided a welcome alternative technique for tackling these problems.

Recently there has been a resurgence of interest in Heaviside's method [40, 41, 42], which has now been placed on a firmer mathematical footing. Like the Laplace transform, the underlying theory is based on complex analysis. It is said [39, see note 38 on page 239] that Bromwich tried, but failed, to teach Heaviside this mathematics.

A.1.2 Solving differential equations

A brief outline of the Heaviside operational calculus is given here, as it will be unfamiliar to most engineers. Mathematicians are likely to find it unsettling!

Consider a simple differential equation

$$\frac{dy}{dt} + ay = b \tag{A.1}$$

where a and b are constants. Replace the time differential by the operator p, so the equation becomes

$$(p + a)y = b \tag{A.2}$$

Then the solution is

$$y = \frac{1}{p+a}b \tag{A.3}$$

where it must be remembered that any function of p is a unary operator so must have an operand – in this case the constant b. How should (A.3) be interpreted? Taking a factor of p out of the denominator and expanding gives:

$$\frac{1}{p+a}b = \frac{1}{p(1+a/p)}b = (p^{-1} - ap^{-2} + a^2p^{-3} + \ldots)b \tag{A.4}$$

where use has been made of the expansion

$$\frac{1}{1+x} = 1 - x + x^2 + \ldots \tag{A.5}$$

without being too bothered about convergence.

If p represents differentiation, then p^{-1} is the inverse i.e. integration. If the constant of integration is temporarily overlooked, then $p^{-1}b = bt$, $p^{-2}b = bt^2/2$ etc. Then

$$\begin{aligned} \frac{1}{p+a}b &= \left(t - \frac{at^2}{2} + \frac{a^2t^3}{6} + \ldots\right)b & \text{(A.6)} \\ &= \left[\frac{1}{a} - \frac{1}{a}\left(1 - at + \frac{a^2t^2}{2} - \frac{a^3t^3}{6} + \ldots\right)\right]b & \text{(A.7)} \\ &= \frac{1}{a}(1 - e^{-at})b & \text{(A.8)} \end{aligned}$$

By using a similar argument it can be shown that

$$\frac{p}{p+a}b = e^{-at}b \tag{A.9}$$

This can alternatively be obtained by using

$$\frac{p}{p+a}b = \left(\frac{p+a}{p+a} - \frac{a}{p+a}\right)b = [1 - (1 - e^{-at})]b = e^{-at}b \tag{A.10}$$

Second-order functions of p can arise when solving second-order differential equations. For example

$$\frac{p^2}{(p+a)^2 + n^2}b = \left(1 - \frac{2ap + a^2 + n^2}{(p+a)^2 + n^2}\right)b \tag{A.11}$$

p expression	interpretation
p^{-n}	$\frac{t^n}{n!}$
$\frac{1}{p+a}$	$\frac{1}{a}(1-e^{-at})$
$\frac{p}{p+a}$	e^{-at}
$\frac{a^2+n^2}{(p+a)^2+n^2}$	$1-e^{-at}\left(\cos nt+\frac{a}{n}\sin nt\right)$
$\frac{p}{(p+a)^2+n^2}$	$\frac{1}{n}e^{-at}\sin nt$
$\frac{p^2}{(p+a)^2+n^2}$	$e^{-at}(\cos nt-\frac{a}{n}\sin nt)$

Table A.1: Interpretation of Heaviside p functions

The second term is expanded into partial fractions based on the complex roots of the denominator. These first-order terms are then handled using the results given above. The final result is

$$\frac{p^2}{(p+a)^2+n^2}b = e^{-at}(\cos nt - \frac{a}{n}\sin nt)b \tag{A.12}$$

These and similar results are summarised in Table A.1.

A.1.3 Initial conditions

The procedure outlined above will give the solution $y(t)$ for all values of time t. However, in many cases what is required is the solution for $t \geq 0$, given initial conditions at $t = 0$. The Heaviside operational method incorporates initial conditions in a straightforward way.

Consider the equation

$$f(p)y(t) = v(t) \tag{A.13}$$

where $f(p)$ is a polynomial in p that represents the original differential operator i.e.

$$f(p) = \sum_{k=0}^{n} a_k p^k \tag{A.14}$$

Then using the product rule for differentiation

$$f(p)(U(t)y(t)) = \sum_{k=0}^{n} a_k \left[U(t)p^k y(t) + \sum_{j=0}^{k-1} p^{k-j-1}\delta(t)y(0;j) \right] \tag{A.15}$$

where $y(0;j)$ is the value at $t = 0$ of the jth derivative

$$y(0;j) = p^j y(t)|_{t=0} \tag{A.16}$$

$U(t)$ is the unit step function

$$U(t) = \begin{cases} 0 & t \leq 0 \\ 1 & t > 0 \end{cases} \tag{A.17}$$

and $\delta(t)$ is the Dirac delta so

$$pU(t) = \delta(t) \tag{A.18}$$

Use has been made of the peculiar properties of δ [41, 43] so that

$$\delta(t)g(t) = \delta(t)g(0) \tag{A.19}$$

Continuing from (A.15)

$$f(p)(U(t)y(t)) = U(t)\left[\sum_{k=0}^{n} a_k p^k\right] y(t) + \sum_{k=1}^{n} a_k \sum_{j=0}^{k-1} p^{k-j} U(t) y(0;j) \tag{A.20}$$

Using (A.13) and (A.14) on the first term, and reordering the summations for the second term gives

$$f(p)(U(t)y(t)) = U(t)v(t) + \sum_{j=0}^{n-1}\left[y(0;j)\sum_{k=j+1}^{n} a_k p^{k-j}\right] U(t) \tag{A.21}$$

For $t > 0$, this can be written as

$$f(p)y(t) = v(t) + \sum_{j=0}^{n-1} f_j(p) y(0;j) \tag{A.22}$$

where

$$f_j(p) = \sum_{k=j+1}^{n} a_k p^{k-j} \tag{A.23}$$

The rule for incorporating initial values is then:

1. Take the operator $f(p)$ on the LHS of the equation then remove any constant term to get $f_0(p)$.
2. Add $f_0(p)y(0;0)$ (i.e. $f_0(p)y(0)$) to the RHS of the equation.
3. Obtain f_i by dividing f_{i-1} by p and removing any constant term.
4. Add $f_i(p)y(0;i)$ to the RHS of the equation.
5. Repeat the previous two steps up to $i = n-1$ where n is the highest power of p in $f(p)$.

A.2 Integrals

The integrals used for the Fourier analysis of the output power in Section 3.1.5 on page 3-14 are

$$\int e^{ax}\sin bx \sin cx \mathrm{d}x = \frac{e^{ax}}{(a^2+b^2+c^2)^2 - 4b^2c^2}\begin{bmatrix} a(a^2+b^2+c^2)\sin bx \sin cx \\ -b(a^2+b^2-c^2)\cos bx \sin cx \\ -c(a^2-b^2+c^2)\sin bx \cos cx \\ +2abc\cos bx \cos cx \end{bmatrix}$$

$$\int e^{ax}\cos bx\cos cx\mathrm{d}x = \frac{e^{ax}}{(a^2+b^2+c^2)^2-4b^2c^2}\left[\begin{array}{l} a(a^2+b^2+c^2)\cos bx\cos cx \\ +b(a^2+b^2-c^2)\sin bx\cos cx \\ +c(a^2-b^2+c^2)\cos bx\sin cx \\ +2abc\sin bx\sin cx \end{array}\right]$$

$$\int e^{ax}\sin bx\cos cx\mathrm{d}x = \frac{e^{ax}}{(a^2+b^2+c^2)^2-4b^2c^2}\left[\begin{array}{l} a(a^2+b^2+c^2)\sin bx\cos cx \\ -b(a^2+b^2-c^2)\cos bx\cos cx \\ +c(a^2-b^2+c^2)\sin bx\sin cx \\ -2abc\cos bx\sin cx \end{array}\right]$$

These may be obtained by using integration by parts twice.

APPENDIX B

MATLAB POWER SERIES CALCULATIONS

B.1 Series Solution

The first-order calculation of the steady-state series solution is described in Chapter 3. This was originally carried out 'by hand', and a second-order solution attempted in the same way. Although some progress was made, it quickly became clear that help was needed with the algebra if simple mistakes were to be avoided. The 'Symbolic Toolkit' of Matlab was used, and the calculations extended at first to third-order, then to include frequency dependence.

The work was carried out in three phases:

1. Find third-order expressions for resonant frequencies (i.e. a and b), and hence component values.

2. Calculate input and output power, and hence efficiency, at the centre frequency.

3. Repeat Phase 2, but including frequency dependence so exact Class E conditions no longer apply.

The Matlab programs (m files) used are briefly described below. As Phase 3 employed updated versions of the Phase 2 programs these two phases are described together.

Some degree of human intervention was needed at times e.g. to simplify an intermediate result. Much use was made of the expansion (valid for $|x| < 1$)

$$\frac{1}{1+x} = 1 - x + x^2 - x^3 + \ldots \tag{B.1}$$

It was found that Matlab was not consistently able to identify and extract or eliminate common factors from complicated rational expressions, and some interactive work and 'pencil-and-paper' assistance was needed. Thus the calculation took on something of the nature of experimental work.

Phase 1 and the early part of Phase 2 was carried out on a PC using a student version of Matlab. This had a hard array size limit, which in turn limited the size of intermediate expressions. The work was transferred to a full Matlab version, running on a Sun workstation. This had a much larger, but softer, array size limit; very large expressions seemed to cause the software to overwrite parts of itself, resulting in a crash or 'garbage' output. This meant that some equations had to be calculated and simplified in sections, before finally assembling the result.

B.2 Phase 1

Third-order expansions of functions were used:

$$\begin{aligned} e^{-\frac{t}{\tau}} &= 1 - \frac{\pi}{2Q} + \frac{\pi^2}{8Q^2} - \frac{\pi^3}{48Q^3} \\ \sin\omega_0 t &= -\pi a + \frac{\pi^3 a^3}{6} \\ \cos\omega_0 t &= -1 + \frac{\pi^2 a^2}{2} \end{aligned} \tag{B.2}$$

Analogous expressions were used for $\sin\omega_1 t$ and $\cos\omega_1 t$. Class E parameters were calculated to third-order too:

$$\begin{aligned} \frac{1}{\omega_0} &= \frac{1}{2\pi f}(1 - a + a^2 - a^3) \\ \frac{C_2}{C_1 + C_2} &= 2(a-b) - 3a^2 - b^2 + 4ab + 4a^3 - 6a^2 b + 2ab^2 - \frac{a-b}{2Q^2} \end{aligned} \tag{B.3}$$

Matlab files used are:

setE0 This produces expressions for the charge and current at the end of the 'switch closed' period, based on their values at the start of the period, using (3.22) and (3.25).

setE1 This produces expressions for the charge and current at the end of the 'switch open' period, based on their values at the start of the period, using (3.21) and (3.24).

setE11 The expressions are combined to give equations for charge and current, based on steady-state Class E conditions.

setEab Matlab was used interactively to solve the equations, and the solutions for charge and current (analogous to (3.36)) included in this program file. These solutions are substituted back into the equations to give constraints on the values of a and b. First-order expressions for a and b are substituted, and this leads to second and third-order expressions being obtained. These are given in (3.44).

Finally, the expressions for a and b were used to obtain component values C_1 and C_2.

B.3 Phases 2 and 3

Having obtained component values, the power and then efficiency were calculated. In Phase 2 this was done by taking the known solutions for charge and current and substituting these into expressions for input and output power. For Phase 3 new solutions were needed, as the earlier phases assumed Class E conditions which are not valid away from the design centre frequency. The equations were more complex, as they now had to differentiate between the design frequency and the operating frequency. However, the values for a and b obtained in Phase 1 could be used.

The new expansions, including semi-normalised frequency offset $x = \Delta f / f_\mathrm{d}$ to $\mathrm{O}(x^2)$, were:

$$\begin{aligned} e^{-\frac{t}{\tau}} &= 1 - \frac{\pi}{2Q}(1 - x + x^2) + \frac{\pi^2}{8Q^2}(1 - 2x + 3x^2) - \frac{\pi^3}{48Q^3}(1 - 3x + 6x^2) \\ \sin\omega_0 t &= -\pi(a - x)(1 - x + x^2) + \frac{\pi^3(a - x)^3}{6}(1 - 3x + 6x^2) \\ \cos\omega_0 t &= -1 + \frac{\pi^2(a - x)^2}{2}(1 - 2x + 3x^2) \end{aligned} \tag{B.4}$$

Initially these expansions included factors like $1/(1 + x)^n$, but these were recast using (B.1) to create simple polynomials from the rational functions. Later, it was found that the frequency was better expressed as a full normalised offset $X = Q\Delta f / f_\mathrm{d}$.

Matlab files used were:

Vdavga This is an extended version of `setE0`, and produces expressions for charge and current during the 'switch closed' period.

Vdavgb This is an extended version of `setE1`, and produces expresions for charge and current during the 'switch open' period.

Vdavgc This is an extended version of `setE11`, and produces equations for charge and current assuming steady-state conditions.

Vdavgd This inserts the known Class E values for a and b.

Vdavge The equations for charge and current are solved, and an expression for the value of C_1 produced. From these two expressions for the mean drain voltage, and hence input power, are obtained. For the centre frequency (i.e. Class E conditions) this is to second order in Q. The alternative expression is valid for other frequencies, but only first order in Q.

Vdavgex This is similar to `Vdavge`, and uses the charge/current solution already obtained therein, but with some manual simplification.

Vdavgey This is also similar to `Vdavge`, but calculates the input power away from the centre frequency to second order in Q.

Pout This simply calls `Pouta`, `Poutb` and `Poutc` in order. The result is the output power to second order in Q. The task had to be split up between, and within, the programs in order to avoid space limitations in Matlab.

Pouta This uses Fourier analysis to calculate the sine component (3.63) of the AC current in the output circuit.

Poutb Similar to `Pouta`, but for the cosine component (3.64).

Poutc This forms the sum of squares of the two current components in order to obtain the output power.

Poutd This takes the result from `Poutc` and tidies it, returning the zeroth, first and second order terms separately. This is for the centre frequency only.

Poutdx This is a development of `Poutd` which handles other frequencies too.

It will be apparent from the above descriptions that the software was being developed 'on-the-fly'. If it were to be re-used, some rationalisation would be helpful. Copies of the m files are included with the thesis.

APPENDIX C

CIRCUITS

C.1 2MHz Power Amplifier and Amplitude Modulator

C.1.1 Purpose

The low frequency (LF) power amplifier was built in order to compare the steady-state and modulation behaviour of a near-ideal circuit with theoretical predictions. The carrier frequency was chosen to be low enough that the device would behave as a good switch, but high enough that inductors would have reasonable Q and not be too large.

It turned out that, as described below, the centre frequency and circuit design had to be slightly modified due to problems encountered with the original output inductor.

C.1.2 Circuit description

The circuit has three main parts: power amplifier, gate drive, and amplitude modulator. In addition there is a voltage regulator.

The Class E power amplifier follows the usual circuit topology. A small power MOSFET (IRF510) is used as a switch. There is a series tuned output circuit C_5-C_6-L_5, drain shunt capacitor C_4, and drain feed choke L_4. Nearly half of the required reactance across the switch is provided by the internal drain-source capacitance. The TO-220 MOSFET package is mounted on a small heatsink. The mounting flange and the heatsink form a small parallel plate capacitor, with the heat-conducting pad as dielectric. The RF properties of this dielectric are not known, but as it contributes less than 10% of the total drain capacitance some losses may be tolerated.

The FET switch ideally requires a square wave gate drive, but many Class E implementations use an overdriven sine wave. This wastes power and leaves the switch duty cycle somewhat poorly defined, but may be unavoidable at high frequencies. Fortunately 2MHz is low enough that good

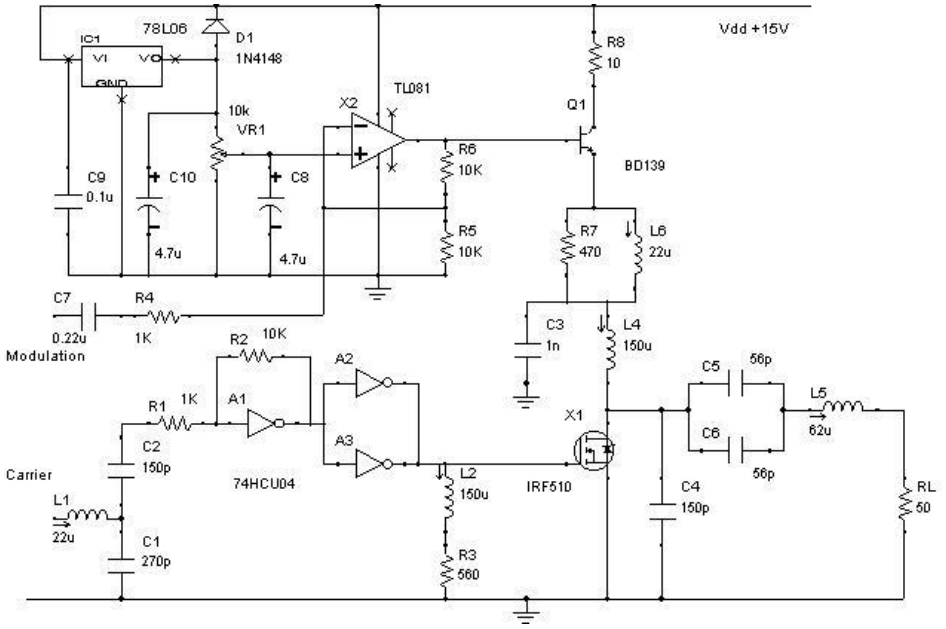

Figure C.1: LF power amplifier circuit

square waves may be obtained from standard logic circuitry.

The IRF510 operates in enhancement mode, with a gate threshold between 2V and 4V. This is a good match to CMOS logic, operating from the maximum 74HC series supply of 6V. Unbuffered logic (74HCU04) can operate as a fast analogue amplifier so this is used as an overdriven first stage to generate a reasonable square wave from the incoming sine wave. The second pair of gates then improves this, and provides enough drive current to cope with the gate capacitance of the FET. In a Class E circuit it is particularly important that the device switches off rapidly, so a simple speed-up circuit L_2-R_3 has been added to the gate. This increases the gate current during turn-off. The slight degradation in turn-on time that this causes can be tolerated.

The input network L_1-C_1-C_2 provides impedance matching, at a Q around 5. About 0dBm of input signal is sufficient to generate gate drive.

The modulator is simply an augmented op-amp. The DC level is set by the preset potentiometer VR1, with the amplifier operating in non-inverting mode with a voltage gain of 2. For external modulation the amplifier operates in inverting mode with a voltage gain of 10. The op-amp is followed by an emitter follower, which drives the PA via a decoupling network R_7-L_6-C_3. The network prevents RF from entering the modulator, but allows amplitude modulation up to quite a high fraction of the carrier frequency. The resistor R_7 damps a resonance.

A resistor R_8 is included in the collector circuit of the emitter follower. This allows for measurement of the PA supply current during modulation. Together with the voltage (at the

emitter) the effective modulation impedance of the PA can be measured. The effect of the decoupling network needs to be taken into account when measurements are made.

The linear regulator provides the +6V supply for the CMOS logic, and sets the potentiometer voltage. The regulator is protected from reverse current by the diode across it. Reverse current could arise if the incoming supply is interrupted, and then C_{10} discharges back through the regulator.

The LF PA was originally designed for Q of 16 at a centre frequency of 1.9MHz. A standard small 68μH inductor was intended for L_5. When measured, it was found to have an unexpectedly low unloaded Q of 40. A new inductor was constructed on a dust-iron toroidal core. This had higher Q (80), but the inductance was a little low at 62.3μH. It was decided to use the new inductor, but to carry out a partial redesign for a loaded Q of 13 at a centre frequency of 2MHz.

C.2 2MHz Phase Modulator

C.2.1 Purpose

In order to investigate the effect of phase modulation without complications being introduced by demodulation, it was decided that the RF waveform would be directly viewed on an oscilloscope. A stable trace will only be achieved if the modulation is phase-locked to the carrier frequency. A modulator was designed which derived the baseband and RF frequencies from a single input.

It is possible that some details of the phase modulation behaviour depend on the phase relationship between the baseband and RF signals, but it is thought that any such effect will be small provided that the Q of the PA output circuit is sufficiently large to smooth out the consequence of a change of excitation over several cycles of RF. It was decided that the convenience of phase-locking outweighed any risk of missing significant phenomena.

C.2.2 Circuit description

The phase modulator provides square wave modulation with the phase shift switchable between $0° - 90°$ and $0° - 180°$. The modulation frequency is selectable in powers of 2 from 2^{-2} to 2^{-8} times the carrier frequency. It is implemented using HCMOS logic. The circuit is shown in Figure C.2.

The sinusoidal input is at 8MHz from a signal generator. The input circuit provides an approximate match to 50Ω, and converts the signal to a square wave using gates A1A and A1B. Flip-flops U1A and U1B divide the frequency by four, and provide quadrature outputs.

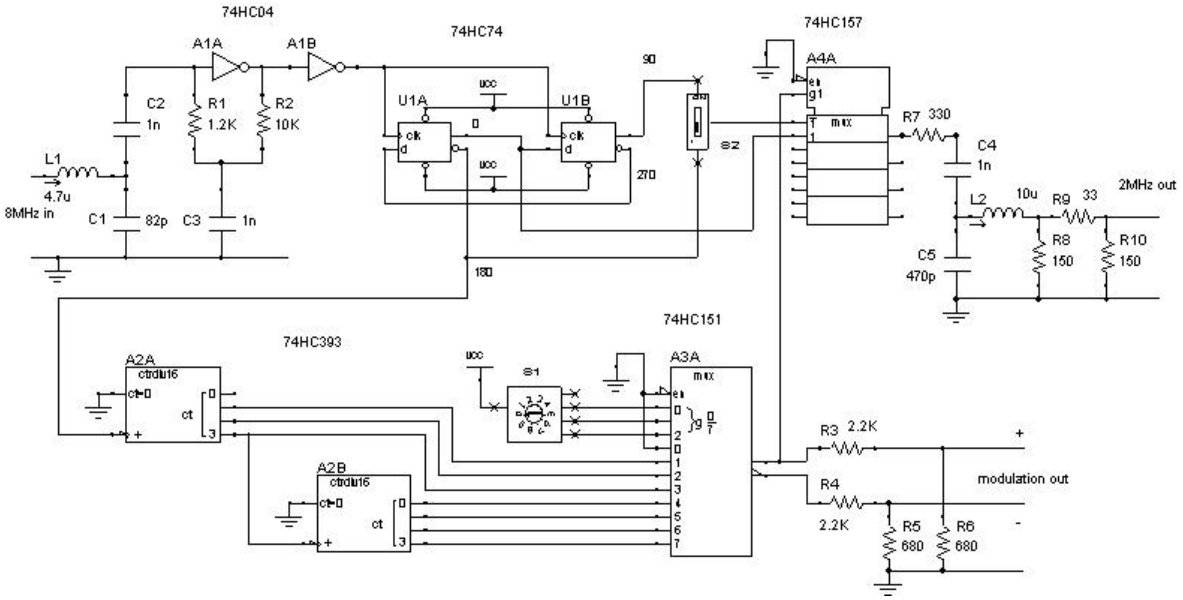

Figure C.2: LF phase modulator circuit

A section of 2–1 multiplexer A4A performs the phase modulation. One input receives the 0° signal, while the other input receives either 90° or 180° (chosen by switch S2). The baseband signal selects which of the two input signals is propagated to the output. The output circuit provides impedance matching, low pass filtering and some attenuation to provide the output at 2MHz.

The 2MHz signal from the divider also goes to an 8-stage binary counter (A2A and A2B). This provides a range of baseband frequencies. One of these is selected by the 8–1 multiplexer A3A under the control of a BCD switch S1. The baseband signal is made available for viewing in normal and inverted form via resistive dividers.

C.2.3 Frequency response

The input and output circuits were designed to be fairly broadband. This is particularly important for the output circuit, which directly affects the bandwidth of the modulation. Measurements were made to check the response.

The input frequency response was measured by finding the minimum input signal level at which proper switching action took place in the input gates – see Figure C.3. This shows that the input centre frequency of 6.8MHz is a little lower than expected, but the sensitivity at 8MHz was deemed to be adequate. An input signal level of 0dBm was used for subsequent work.

The output frequency response was obtained by measuring the output signal voltage, with a 0dBm input level. The response was very broad (Figure C.3). The signal level was lower than

expected, but sufficient for the intended purpose.

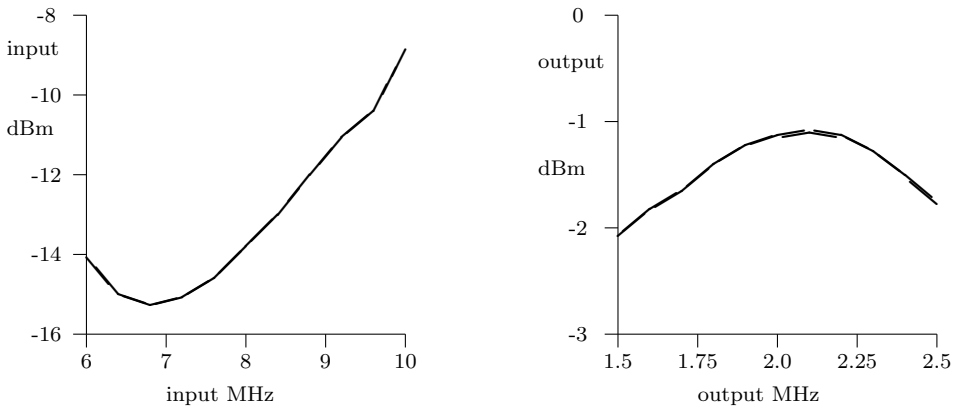

Figure C.3: Phase modulator: input sensitivity, output frequency response

C.3 Polar Modulator

C.3.1 Purpose

The polar modulator was developed in order to test how the LF PA behaved under simultaneous amplitude and phase modulation. The modulator produces amplitude and phase signals, synthesising double-sideband suppressed-carrier AM from a baseband input signal. The amplitude channel consists of a precision rectifier followed by a buffer amplifier; the phase channel has a comparator and a double-balanced mixer.

It was originally intended that the polar modulator should operate at a VHF carrier frequency, with baseband signals up to a few MHz. Problems were found with both the mixer and the rectifier, so after a review it was decided to modify the modulator for use at lower frequencies. The resultant circuit is shown in Figure C.4. For the sake of clarity, some power supply, decoupling and buffer components have been omitted.

C.3.2 Circuit description

The baseband signal enters via DC blocking capacitor C_1 and splits into the two channels. The phase channel starts with X1A, a comparator performing data slicing around the 0V level, to obtain the sign of the input signal. It has an open collector output so requires a pull-up resistor R_{15}. The circuit originally had provision for an active delay line at this point, in order to allow matching of the channel delays, but this was abandoned because the two delay lines tried seemed to be suffering from a batch fault which shorted the power supply.

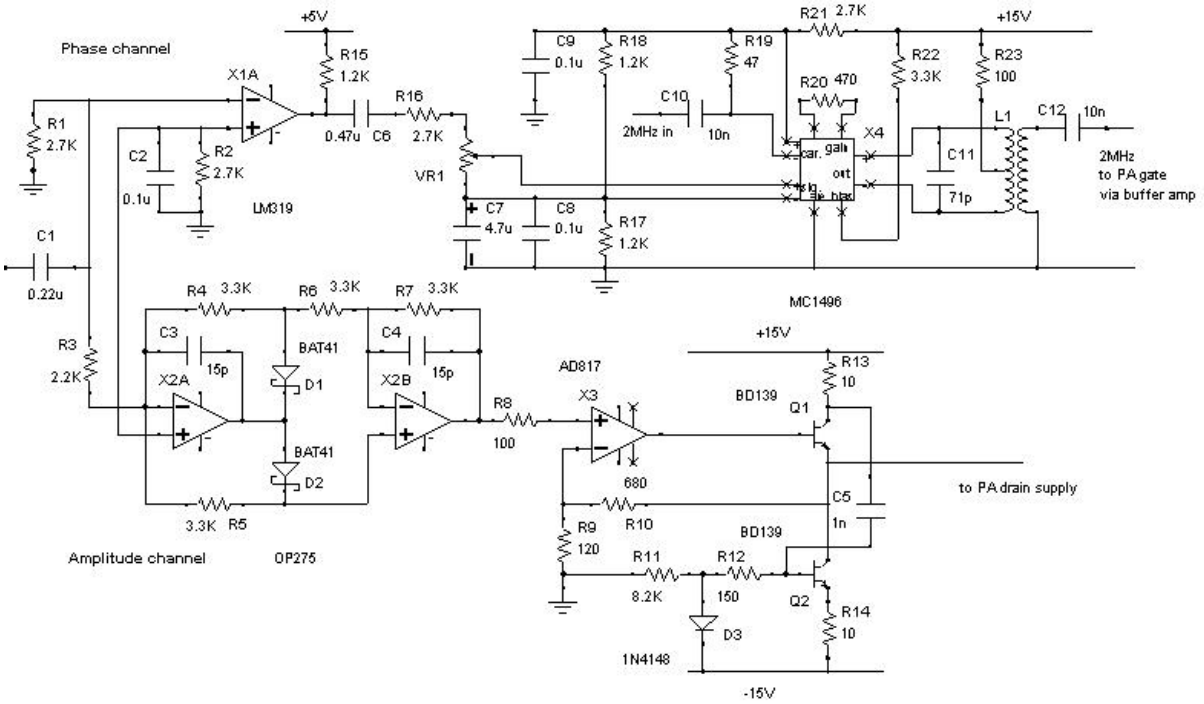

Figure C.4: LF polar modulator circuit

After attenuation, the sign signal enters the signal port of the double-balanced mixer X4. A 2MHz signal enters via the carrier port. The resultant 180° phase-switched signal is developed at the balanced output in transformer L1. From there it is amplified by a Mini-Circuits MAV-11 MMIC (not shown) before entering the PA board.

The circuit around X2 is a precision rectifier which delivers the amplitude of the input. X1 and X2A both operate from the same reference voltage, developed across R_2 by the small input current of the devices. The output is amplified by X3 and then buffered by the emitter follower Q1. The amplitude signal is taken from here to the PA, and replaces the drain feed from Q1 there (i.e. at the top end of L_6/R_7 in the PA).

The circuit around Q2 is an active load for Q1, which only takes effect for fast negative-going signals. It was added to the original design because a simple emitter follower is not capable of sustaining a high slew rate in the negative direction. The voltage developed across D3 is not quite enough to bias Q2 on. However, a sudden fall in current in Q1 will cause a voltage increase at the collector, which is transferred to the base of Q2 via C_5. Q2 turns on, thus pulling the output down. At the new lower frequencies being used, it is unclear whether Q2 is necessary but it was left in place.

C.3.3 Frequency response

The main constraint on the bandwidth of the polar modulator is the tuned circuit L_1-C_{11} at the output of the balanced mixer, in the phase channel. A little delay here is helpful, as it offsets the delay introduced into the amplitude channel by the PA itself. The output frequency response of the polar modulator was measured - see Figure C.5.

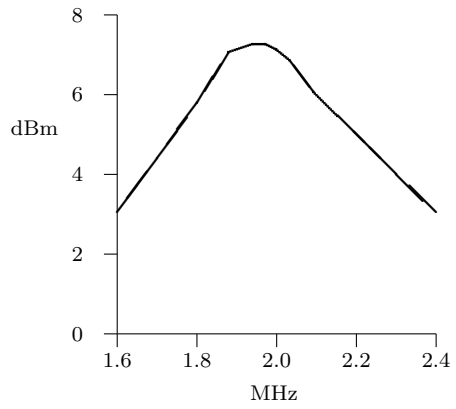

Figure C.5: Polar modulator: output frequency response

The -3dB bandwidth is 0.6MHz, with a centre frequency of 1.95MHz. This implies a Q of about 3.2, and a delay of 0.53μs due to the tuned circuit.

Measurements were made of the channel delay times, using the comparator output transition edge as the reference point. The total delay from this point to the phase change at the output was 0.6μs – consistent with the bandwidth. The delay from the edge transition to the negative cusp at the output of the amplitude channel was 0.24μs. Thus the differential delay was a lag of 0.36μs on the phase channel.

APPENDIX D

JUSTIFICATION OF AN APPROXIMATION AND AN ASSERTION

D.1 Large Feed Inductance in Series Solution

When calculating the behaviour of the output circuit for the 'switch open' state in Section 3.1 of Chapter 3, it was assumed that L_1 was sufficiently high in value that its inverse could be ignored. Then (3.8) simplifies to (3.13). Under what conditions is this approximation justified?

It is possible to solve the quartic equation which appears in the denominator of (3.8), but the solution would be cumbersome and so not very enlightening. However, if L_1 is high enough then the quadratic solution obtained in (3.14) and (3.15) will be an approximate solution for the quartic. A first order correction will then exhibit the effect of L_1.

The equation to be solved is

$$p^4 + \frac{R}{L_2}p^3 + \left[\frac{1}{L_2}\left(\frac{1}{C_1}+\frac{1}{C_2}\right)+\frac{1}{L_1C_1}\right]p^2 + \frac{R}{L_1L_2C_1}p + \frac{1}{L_1L_2C_1C_2} = 0 \qquad \text{(D.1)}$$

This can be written in a form which shows the quadratic terms (see (3.13)) for which a solution has already been obtained:

$$p^2\left[p^2 + \frac{R}{L_2}p + \frac{1}{L_2}\left(\frac{1}{C_1}+\frac{1}{C_2}\right)\right] + \frac{1}{L_1C_1}\left[p^2 + \frac{R}{L_2}p + \frac{1}{L_2}\left(\frac{1}{C_1}+\frac{1}{C_2}\right) - \frac{1}{L_2C_1}\right] = 0 \qquad \text{(D.2)}$$

The solutions of interest are a conjugate pair, so it is only necessary to consider one of them. Let a solution be

$$p = -\frac{1}{\tau} + j\omega_0 \qquad \text{(D.3)}$$

where (see (3.14) and (3.15))

$$\tau = \frac{2L_2}{R} + \Delta\tau \qquad \text{(D.4)}$$

and

$$\omega_0^2 = \frac{1}{L_2}\left(\frac{1}{C_1}+\frac{1}{C_2}\right) - \frac{1}{\tau^2} + \Delta\omega^2 \tag{D.5}$$

Substituting (D.3) for p in (D.2) gives

$$\begin{aligned}&\left(-\frac{1}{\tau}+j\omega_0\right)^2\left[\frac{2}{\tau^2}-\Delta\omega^2+2j\omega_0\left(\frac{1}{\tau-\Delta\tau}-\frac{1}{\tau}\right)-\frac{2}{\tau(\tau-\Delta\tau)}\right]\\&+\frac{1}{L_1C_1}\left[\frac{2}{\tau^2}-\Delta\omega^2+2j\omega_0\left(\frac{1}{\tau-\Delta\tau}-\frac{1}{\tau}\right)-\frac{2}{\tau(\tau-\Delta\tau)}-\frac{1}{L_2C_1}\right]=0\end{aligned} \tag{D.6}$$

If $\Delta\tau$ is sufficiently small then this can be written as

$$\begin{aligned}&\left(-\frac{1}{\tau}+j\omega_0\right)^2\left[-\Delta\omega^2+\frac{2j\omega_0\Delta\tau}{\tau^2}-\frac{2\Delta\tau}{\tau^3}\right]\\&+\frac{1}{L_1C_1}\left[-\Delta\omega^2+\frac{2j\omega_0\Delta\tau}{\tau^2}-\frac{2\Delta\tau}{\tau^3}-\frac{1}{L_2C_1}\right]=0\end{aligned} \tag{D.7}$$

or

$$\left[\left(-\frac{1}{\tau}+j\omega_0\right)^2+\frac{1}{L_1C_1}\right]\left[-\Delta\omega^2+\frac{2j\omega_0\Delta\tau}{\tau^2}-\frac{2\Delta\tau}{\tau^3}\right]=\frac{1}{L_1L_2C_1^2} \tag{D.8}$$

The real and imaginary parts of this equation can now be considered.

The imaginary part of (D.8) simplifies to

$$\left(\Delta\omega^2+\frac{2\Delta\tau}{\tau^3}\right)+\frac{\Delta\tau}{\tau}\left(-\omega_0^2+\frac{1}{\tau^2}+\frac{1}{L_1C_1}\right)=0 \tag{D.9}$$

The real part of (D.8) gives

$$\frac{4\omega_0^2\Delta\tau}{\tau^3}-\left(\Delta\omega^2+\frac{2\Delta\tau}{\tau^3}\right)\left(-\omega_0^2+\frac{1}{\tau^2}+\frac{1}{L_1C_1}\right)=\frac{1}{L_1L_2C_1^2} \tag{D.10}$$

Substituting using (D.9) gives

$$\frac{4\omega_0^2\Delta\tau}{\tau^3}+\frac{\Delta\tau}{\tau}\left(-\omega_0^2+\frac{1}{\tau^2}+\frac{1}{L_1C_1}\right)^2=\frac{1}{L_1L_2C_1^2} \tag{D.11}$$

Working to first order in $1/L_1$ this becomes

$$\frac{\Delta\tau}{\tau}\left(\omega_0^2+\frac{1}{\tau^2}\right)^2=\frac{1}{L_1L_2C_1^2} \tag{D.12}$$

Substituting from (D.5) but to first order only, the result is

$$\frac{\Delta\tau}{\tau}=\frac{L_2C_2^2}{L_1(C_1+C_2)^2} \tag{D.13}$$

Taking first order terms only, (D.9) can be written as

$$\Delta\omega^2=\frac{\Delta\tau}{\tau}\left(\omega_0^2-\frac{3}{\tau^2}\right) \tag{D.14}$$

If the output circuit Q is sufficiently high, then the term in τ^{-2} can be ignored and the result is

$$\frac{\Delta\omega^2}{\omega_0^2} = \frac{\Delta\tau}{\tau} \tag{D.15}$$

It is now possible to determine the effect of finite L_1. If the calculations of Chapter 3 are to be valid, then it is required that $\Delta\tau/\tau \ll 1$ i.e.

$$\frac{L_2 C_2^2}{L_1(C_1+C_2)^2} \ll 1 \tag{D.16}$$

The output circuit is resonant near the operating frequency:

$$L_2 C_2 \simeq \frac{1}{\omega_\mathrm{d}^2} \tag{D.17}$$

Provided the circuit Q is sufficiently high then $C_1 \gg C_2$, so (D.16) can be approximated as

$$\frac{C_2}{\omega_\mathrm{d}^2 L_1 C_1^2} = \frac{X_{\mathrm{C1}} C_2}{X_{\mathrm{L1}} C_1} = \frac{X_{\mathrm{C1}}^2}{X_{\mathrm{L1}} X_{\mathrm{C2}}} \ll 1 \tag{D.18}$$

From the canonical analysis (Chapter 2) it is known that the values of C_1 and C_2 are both related to the load resistance: $X_{\mathrm{C1}} = 5.4466R$ and $X_{\mathrm{C2}} \simeq QR$. So from (D.18) it is required that the reactance of L_1 at the design frequency satisfies

$$X_{\mathrm{L1}} \gg \frac{30R}{Q} \tag{D.19}$$

This can be refined by requiring that the shift in ω_0 caused by L_1 be significantly smaller than the shift due to circuit Q. Using (3.27) and (3.45) gives

$$X_{\mathrm{L1}} \gg 7R \tag{D.20}$$

D.2 Ignoring Offsets

In obtaining (4.11) on page 4-4 it was stated that when calculating circuit time constants one may ignore voltage or current offsets. This can be demonstrated by considering a CR circuit (Figure D.1). As a first-order circuit this is characterised by a time constant.

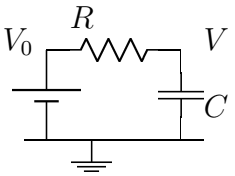

Figure D.1: CR circuit

The time constant can be obtained either by solving the differential equation for charge, or by considering stored and dissipated energy. The equation for charge is

$$\frac{q}{C} + R\dot{q} = V_0 \tag{D.21}$$

The solution, expressed as capacitor voltage V, is

$$V = (V_\mathrm{i} - V_0)e^{\frac{-t}{\tau}} + V_0 \tag{D.22}$$

where V_i is the initial voltage on the capacitor at $t = 0$ and τ is the circuit time constant given by

$$\tau = \frac{1}{CR} \tag{D.23}$$

The time constant does not depend on the offset voltage V_0, so when calculating τ via energy it is permissible to choose any value for V_0. It is usually convenient to choose $V_0 = 0$, as then there is no energy flow to or from the power supply. Then

$$\text{fractional rate of change of energy} = \frac{\text{power dissipation}}{\text{stored energy}} = \frac{\frac{V^2}{R}}{\frac{1}{2}CV^2} = \frac{2}{CR} \tag{D.24}$$

i.e.

$$\text{energy time constant} = \frac{CR}{2} \tag{D.25}$$

so

$$\text{voltage time constant} = \tau = CR \tag{D.26}$$

because when $V_0 = 0$, squaring the voltage to calculate energy simply corresponds to doubling the argument of the exponential (see (D.22)). As (D.21) and its solution (D.22) have the same form for any first-order system, the same argument can be used (as in Section 4.2.2).

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