UNIVERSITY OF BIRMINGHAM

COMMUTATION FAILURE PREDICTION AND INTERACTION MECHANISM OF MULTI-INFEED LCC-HVDC SYSTEMS UNDER ASYMMETRICAL FAULTS

by

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ABSTRACT

Line-Commutated Converter based HVDC (LCC-HVDC) systems have been widely used for long-distance bulk power transmission and will play a vital role in the future decarbonised power systems since renewable energy resources are normally far away from load centres. As a frequent dynamic event in LCC-HVDC inverters, the Commutation Failure (CF) is mostly caused by AC side faults, 70% of which are asymmetrical Single-Line-Ground (SLG) faults, and may cause power transmission cessation, cascading trips, and even blackout. Researchers have studied CF mechanism for decades, but most of them only considered the magnitude change of the faulty phase commutation voltage when predicting CFs under asymmetrical faults. However, this research proves that both the magnitude and phase angles of not only the faulty phase but also the non-faulty phase commutation voltages will also change and become unbalanced under asymmetrical faults, which reveals that previous CF prediction approaches are unrealistic and inaccurate.

By considering these factors, this research proposes mathematical methods for predicting CFs and Continuous CFs (CCFs) in Multi-Infeed LCC-HVDC systems under asymmetrical faults. Then an Immunity Index of the inverter to CCFs (IICCF) based on the proposed CF prediction method is proposed to quantify the safety margin of the inverter in normal operation condition to CCF risks. The Interaction Factor between inverters under asymmetrical faults with CCF risks (IFCCF) based on IICCF is also proposed to quantify the interaction between two inverters that whether CCFs occur in inverter would result in CCFs in its adjacent inverter or not. are analysed in Multi-Infeed LCC-HVDC systems. These mathematical methods can help the power system operators fast and efficiently predict CFs and identify CF risk areas.

Furthermore, an extended Phase-Locked Loop (PLL) topology is proposed to suppress CFs in LCC-HVDC systems under asymmetrical faults, considering the impact of the phase angle shifts of the commutation voltages.

The accuracy and effectiveness of the proposed methods and topology are verified by simulations on Real-Time Digital Simulator (RTDS). It needs to be emphasised that RTDS (or any other electromagnetic transient simulation software) is not suitable for practical scenarios due to the large scale and complexity of the actual power system and various types of faults as well as innumerable potential fault points, and consequently it is not capable of fully simulating the actual power grid, and all fault scenarios. In other words, it is essentially impossible to use RTDS to make predictions of CFs in large grids in real world scenarios.

Therefore, the fast, accurate and efficient mathematical CF prevention and mitigation methods reported in the thesis contribute to the predictability and suppression of CFs in LCC-HVDC projects, hence helping the system operators design new LCC-HVDC projects and upgrade existing ones.

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List of Publications & Patents

Journal Papers:

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2. N. Chen, Y. Yang, L. Li, C. Cui, Y. Xue, X. -P. Zhang, "Commutation Failure Prediction for Multi-Infeed LCC-HVDC Systems Under Asymmetrical Faults," *IEEE Transactions on Power Delivery* (under review, Jul. 2022)
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Report

1. N. Chen, Y. Xue, X. -P. Zhang, et al., "Key Technologies of Flexible LCC Converter with Controllable Capacitors", NARI report for SGCC project SGTYHT/20-JS-223, Jul. 2022

Patent

1. N. Chen, Y. Xue, X. -P. Zhang, et al., "Commutation failure prediction for LCC-HVDC systems," Applied to European Patent Office, Application No.: PCT/CN2022/095770, May 2022

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LIST OF ABBREVIATIONS

6M2A	Six-Machine-Two-Area
AAA	Asymmetrical Advancing Angle
AAAD	Asymmetrical Advancing Angle Difference
CC	Constant Current
CCF	Continuous Commutation Failure
CEA	Constant Extinction Angle
CF	Commutation Failure
CV	Constant Voltage
FCF	First Commutation Failure
FIM	Fault Inverse Module
HVDC	High Voltage Direct Current
LCC	Line-Commutated Converter
LCC-HVDC	LCC based HVDC
NCCF	Non-Continuous Commutation Failure
PLL	Phase-Locked Loop
SC	Symmetrical Components

CHAPTER 1 Introduction

1.1 Background

1.1.1 Needs for LCC-HVDC Transmission

Since the Industrial Revolution in the 1800s, the increase rate of the global temperature has become higher [1]. Climate change is one of the major threats to the global biodiversity in the next century [2][3], and it is predicted that as high as 54% of species will extinct due to climate change [4]. Climate change is mainly caused by the human activity of burning fossil fuels and changing the way of using the land. Carbon Dioxide (CO_2) is one of the major compositions of Greenhouse Gas (GHG) that causes the increase in the global temperature, and sources of anthropogenic CO_2 emissions which reach 40 Gt/year in 2019 mainly include oil (29%), gas (18%), and coal (33%) [5].

However, limiting human activities is not a sustainable solution to reducing GHG emissions and protecting the environment. The only efficient method of meeting up human's increasing energy demand is to develop renewable energy to replace the abovementioned fossil fuels. Many countries have set the "net-zero" goal by 2060. For instance, the UK aims to reach the 'Net-Zero' goal by 2050 [6]; China plans to peak carbon dioxide emissions by 2030 and reach carbon neutrality before 2060 [7]. All these countries are actively exploring renewable energy sources like wind power and solar power.

Nevertheless, most of renewable energy resources are far away from the load centre. This needs high-capacity long-distance power transmission, which can be realised by High-Voltage Direct Current (HVDC) and High-Voltage Alternative Current (HVAC) transmission systems. HVDC

technology is more suitable for long-distance transmission over 600 km than HVAC since it could save 30% - 50% of transmission losses and carry 30% - 40% more power given the same size of transmission lines [8]. Besides, HVDC also has the advantages of interconnection between asynchronous AC grids, elimination of reactive power for power transmission purposes, and improvement of grid stability [9][10]. Figure 1-1 shows the overview of HVDC projects all over the world based on data released by the European Joint Research Centre in 2017 [11], where China is estimated to install around 60% capacity of HVDC projects worldwide with only 20% of the number of the projects by 2018 [12], and the largest HVDC project is also located in China transferring 12 GW power on a single Line-Commutated Converter based HVDC (LCC-HVDC) link with the transmission distance of 3300 km [13].

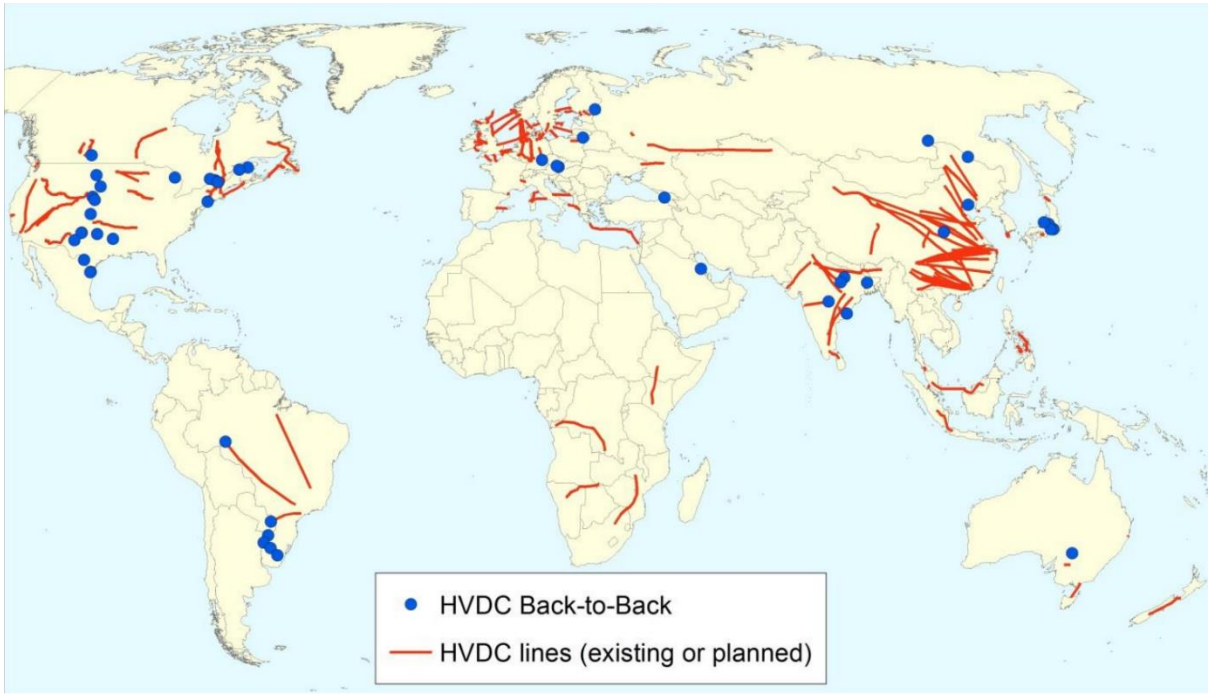


Figure 1-1 The world map of HVDC projects by 2017 [11]

Among the HVDC technologies, the LCC-HVDC technology is a mature technology with the highest power and efficiency rating that has been applied in commercial use for more than 50 years [14][15]. Compared with the other type of HVDC, i.e., Voltage-Sourced Converter based

HVDC (VSC HVDC), the LCC-HVDC has better performance in the transmission loss reductions and ultra-high voltage DC (UHVDC) power transmissions, and it has a higher number of projects than VSC HVDC. It has been reported in [16] that the LCC converter stations take up more than 70% of global HVDC projects based on a sample of 170 HVDC projects which are mainly dominated by the three HVDC technology suppliers - ABB (Hitachi), Siemens, and GE, as shown in Figure 1-2, respectively, where 'N/G' indicates the information is missing.

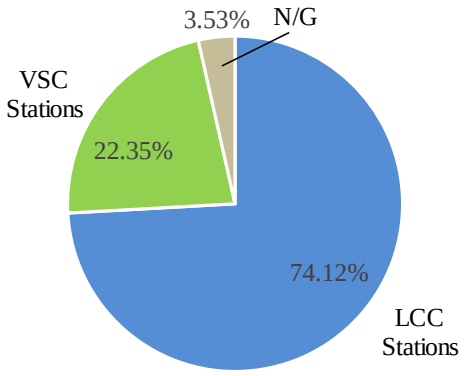


Figure 1-2 The global LCC and VSC converter station numbers based on a sample of 170 projects [16]

Therefore, as a highly efficient solution for economical bulk-power long-distance transmission and interconnecting asynchronous AC grids, LCC-HVDC technology still plays a vital role in power transmission systems nowadays and in the future. Developing research work on LCC-HVDC topology is meaningful and necessary for not only planning and designing new LCC-HVDC projects but also upgrading existing ones for stable association with adjacent power transmission networks.

1.1.2 The Weaknesses of LCC-HVDC

As a major weakness, Commutation Failure (CF) is a frequent dynamic event occurring in the

inverter valve groups when AC faults (e.g., lightning, strong wind, heavy snow, falling trees, mountain fire, etc.) happen at the LCC-HVDC inverter side AC system. Different with VSC HVDC technology that generates AC side voltages by switching in and out the voltage sources (capacitors at the DC side) through the fully controllable IGBTs which have no CF risks, the LCC-HVDC inverters require the AC side bus voltage as the commutation voltage to realise the DC current commutation among the three phase thyristor valve groups in their upper and lower arms. The valve currents I1, I2, …, I6 of the six thyristor groups in the inverter are shown in Figure 1-3, where the commutation indicates the whole process of the DC current commutated from one thyristor valve to the next, and TV1, TV2, …, TV6 are the thyristor valves. Under fault conditions as shown in Figure 1-3, once the commutations is unsuccessful (e.g., DC current fails to get commutated from TV1 to TV3), the upper and lower valve groups in the same phase will conduct the DC current at the same time under fault conditions which means the inverter is short-circuited, i.e., the valve currents under faults I1f and I4f lead to the short circuit issue between the two terminals of the DC side through TV1 and TV4. This phenomenon of failing the commutations and resulting in short circuit issues is defined as CF.

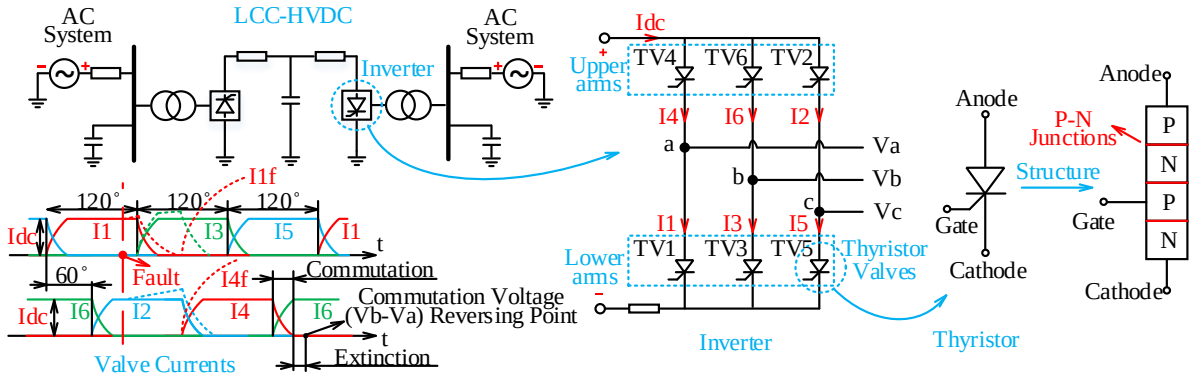


Figure 1-3 LCC-HVDC topology, inverter topology and the thyristor structure [17]

The phenomenon of CF was observed and studied by the researchers in the first application of the LCC-HVDC technology [17]–[19]. With decades of development, CF risk still exists

although the mercury arc valves were upgraded by the thyristor valves [20]. CFs are caused by the characteristic of the thyristors that these silicon-based semiconductors can only get into the forward-blocking state if they suffer from inverse terminal voltage (i.e., commutation voltage) for a certain period of time [21]. This time period is called the 'extinction' process as shown in Figure 1-3 during which the thyristors have to form the inner P-N junctions under the inverse terminal voltage to block the forward currents [22][23]. However, under AC faults, the P-N junctions may not be formed successfully due to the insufficient commutation voltage and reduced extinction angle. In this case, thyristors will fail the commutation process and cause short circuit problems to the two thyristor valves in the same phase within the inverter. The short circuit between the upper and lower thyristor valves in the same phase will decrease the DC voltage to near zero and increase the DC current sharply. Once the faults cannot be cleared in time, the continuous faulty status will cause the blocking of the inverters and then cut off the active power transfer [24], which will result in the supply-demand imbalance in both sending (rectifier) and receiving (inverter) ends of the LCC-HVDC system. This will further affect frequency stability and voltage stability, especially in low-inertia power systems due to increased integration of renewable energy. The details are listed below:

(1) At the sending end, power is over-supplied and then the system frequency will increase. The system operator may need to trip generators at this end to maintain the frequency around the rated value. The increase of the system voltage may also lead to the renewable energy sources going off-grid due to their insufficient high-voltage ride-through capability [25][26].

(2) At the receiving end, power is under-supplied which will cause the reduction of system frequency. It may be solved by activating backup generators or in extreme circumstances, tripping a part of the load [27].

Besides, the blocking of the faulty LCC-HVDC link will cause overload problems in parallel AC or DC transmission lines, which brings a high risk of cascaded tripping [28].

Furthermore, the continuous CFs (CCFs) occurring under severe fault cases will prolong the short circuit duration compared with the non-continuous CFs (NCCFs), and thus have higher risks on the system frequency stability and voltage stability. Here, CCF refers to the CFs which occur continuously after FCF in extreme fault conditions, and any cycles of the commutation process keep failing until the fault is removed, even under the adjustment of the control systems. NCCF indicates the CFs which occur intermittently after FCF, especially during the recovery process, and at least one cycle of successful commutation among the six thyristor valve groups in the inverter exists before NCCFs occur.

Therefore, it is vital to research the mechanism of CFs, especially the continuous CFs (CCFs), study the interactions of inverters in Multi-Infeed LCC-HVDC systems under AC faults, and propose new measures to reduce CF risks to maintain the stable operation of the power grids to help to design new LCC-HVDC projects and upgrade existing ones.

1.2 Literature Reviews

1.2.1 Commutation Failure Prediction and Prevention for LCC-HVDC Systems

As mentioned above, LCC-HVDC systems have been widely used for long-distance bulk power transmission [29]–[31], and CF is a frequent dynamic event at the inverter side mostly caused by AC system faults [32]–[35]. CF can lead to a cessation of active power transfer and severely affect the frequency stability of the connected AC systems (due to their up to 6-12GW rating). Therefore, a number of studies have been carried out on CF. They can be classified into the following categories:

1. Eliminating CF: By inserting controllable capacitors to provide extra commutation voltages to maintain successful commutations [29];

2. Mitigating CF through:

    a. Reducing the DC current order or improving CEA control systems to advance the firing instant, e.g., CFPREV[36], improved CEA control [37]–[43] and the whole control system [44][45] to increase the extinction angle margin to ensure successful commutations;

    b. Installing additional devices into the system, e.g. reactive power compensators [46] to improve the commutation voltage;

    c. Modifying the converter topology to mitigate CFs by utilising the full-bridge thyristor modules [47] or using new inverter transformers[48];

3. Analysing the interaction between DC and AC systems related to CFs, predicting CFs, and identifying CF risk areas. E.g., [49] proposed Multi-Infeed Interaction Factor (MIIF) and CF Immunity Index (CFII). [50] and [51] proposed Local CFII (LCFII), Concurrent CFII (CCFII), Weak Coupling MIIF (WCMIIF), ac-dc interaction factor (ADIF), and Distortion ADIF (DADIF). [50]–[55] predicted CFs and analysed CF risk areas in multi-infeed HVDC systems.

Methods in 1 and 2 can effectively improve the immunity of LCC-HVDC systems to CFs or even eliminate CFs. Methods in 3 are of practical importance in predicting CFs and identifying the risk areas of CF.

In the above three categories of CF-related research, CF is normally divided into the First CF (FCF) and Subsequent CF (SCF). SCF refers to the CFs that occur after the FCF during the

fault and the recovery process. SCFs are caused by severe faults as well as the delay of the control system, and will further prolong the short-circuit status of the thyristor valves and will ultimately bring more serious risks to the power grids, such as cascading trips, or even grid collapses [56] - [58]. Thus, due to the importance of predicting CFs and mitigating SCFs, a number of studies have been carried out. Reference [59] - [61] pointed out that the main reasons for SCFs are lack of reactive power, second voltage dip, harmonic distortion, and interaction of control systems. Reference [43], [62] proposed an early warning system for SCFs and a prediction criterion by combining model and data-driven methods. For CF prediction, the majority of researchers utilize the VTA method proposed by [63] to calculate the extinction angle during the fault to estimate CFs by comparing with the minimum required extinction angle and then develop their methods to mitigate CFs.

Faults in power systems can be categorised as symmetrical faults and asymmetrical faults. Symmetrical faults mainly include single-line-to-ground, line-to-line, and double-line-to-ground faults. While asymmetrical faults mainly indicate the balanced three phase faults.

It has been found from the above research that there is a significant lack of research publications on CF analysis under unbalanced faults that considers the changes of both the magnitude and phase angle of all three-phase commutation voltage during unbalanced faults. This is particularly important given that over 70% of transmission faults are single-phase faults [64], and most of the CFs are caused by single-phase faults [65]. Besides, [66] even pointed out that the asymmetrical fault could be more severe than symmetrical faults based on a large amount of EMT simulations. In addition, few studies have considered the impact of transformer connections on CFs. YY converter transformers were used in most of the existing research without considering the impact of the YD converter transformer.

Figure 1-4 shows the simulation results of a phase A fault in the CIGRE LCC-HVDC Benchmark system. It can be seen from Figure 1-4 that the magnitudes and phase angles of not only the faulty phase but also non-faulty phases are changed. Specifically, the magnitude and phase angle of phase B voltage is reduced by 15% and lags by 20 degrees, respectively. These changes have a direct impact on the commutation performance.

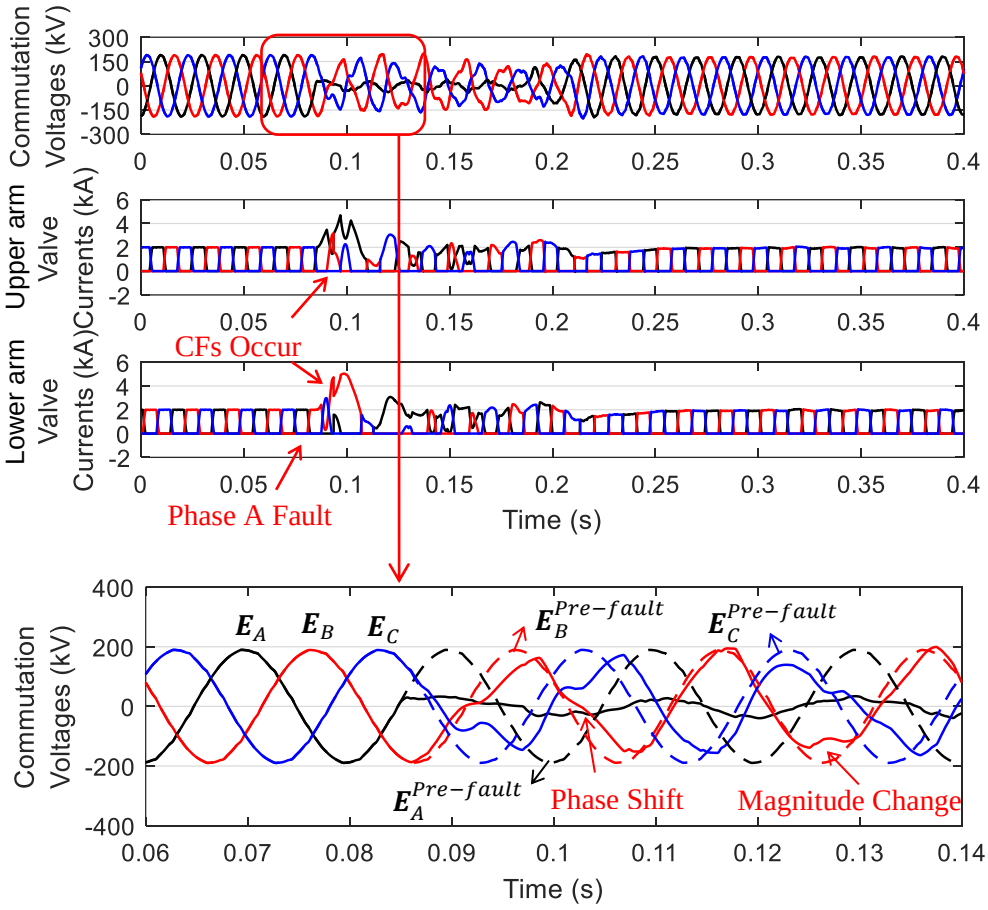


Figure 1-4 Commutation process of the CIGRE LCC-HVDC Benchmark system

Thus, the magnitude changes and the phase angle shifts of both faulty phase and non-faulty phase commutation voltages for LCC-HVDC systems under asymmetrical faults need to be studied. Detailed analysis is shown in Chapter 2.

In addition to the abovementioned research about CFs, the Symmetrical Components (SC) method is also used by a group of researchers to analyse the commutation voltages under

asymmetrical faults.

[67] utilised the SC method to analyse the relationship between the phase angle shift and the probability of CFs and put forward a model that describes the commutation process during the asymmetrical faults. However, the effect of the zero sequence components is neglected when utilizing the sequence network diagram to derive the mathematical model to describe the line voltages and phase shifts and didn't consider the effect of the inner-loop currents within the secondary side of the YD transformer in the 12-pulse LCC-HVDC system.

[68] utilised the SC method to propose an improved CF predictive control which is based on the CFPREV system to suppress the CFs, however, only the zero sequence components are utilised to accomplish the improvement and the sequence network diagram of the whole system is not considered. [69] also used the SC method to predict the commutation failures by considering the commutation voltage distortion and DC current variation. However, the detailed sequence network diagram of the inverter side of 12-pulse LCC-HVDC is simplified and not well developed.

[70] derived the commutation voltages for the 12-pulse LCC-HVDC system through the SC method to analyse the characteristic of the commutation voltage under faults with different fault impedance. But the phase angles and the magnitudes of the commutation voltages are calculated separately and only the faulty phase voltage magnitude is considered to change under the SLG faults. [71] presented the sequence network diagram of the simplified inverter side of the LCC-HVDC system to improve the control system to mitigate the CFs, and the final expressions also consider the impact of the wiring method of the YY and YD transformers. However, only the positive sequence components of the commutation voltages are utilised to improve the output of the control system to achieve the CF suppression which is not accurate

as the positive sequence components can not reflect the actual voltage change.

Therefore, the unbalanced variables for LCC-HVDC systems under asymmetrical faults can be solved by using the SC method. Detailed analysis is shown in Chapter 3.

1.2.2 Continuous Commutation Failure Study for LCC-HVDC Systems

As mentioned in Section 1.2.1, CF occurs in the inverter of the LCC-HVDC system frequently and is mainly caused by the AC system faults most of which are single-line-to-ground (SLG) faults [24], [34], [72], [73]. Under severe fault conditions, the commutation process will always fail due to the CCFs. Compared with NCCF, CCF is of particular concern as it can lead to the blocking of the inverters and then the cessation of the active power transfer [24]. Thus, it has higher risks on the voltage and frequency stability of the systems, e.g., load shedding, generator tripping, and even cascaded tripping [27] [28].

Facing the above challenges, it is of significant importance to predict CCFs under asymmetrical faults and study the interactions between the inverters in Multi-Infeed LCC-HVDC systems.

Although the prediction of CCFs has been discussed in existing research as shown below, few of them consider both the magnitude changes and phase shifts for all three phase commutation voltages under asymmetrical faults. This will result in inaccurate predictions and thus lead to detrimental consequences.

[41], [55], [74] considered the DC current change when evaluating the extinction angle to determine CFs. [69] predicted the risk of CFs by evaluating the extinction starting time and its duration. [62] [75] evaluated risks of Subsequent Commutation Failure (SCF) by comparing the derived extinction angle and the minimum extinction angle. However, the phase shifts of the commutation voltages are not considered in the above literature. The SCF prediction

method in [43] considered the phase shifts of the Line-to-Line (L-L) commutation voltages, but the phase shifts of the non-faulty phase commutation voltages are not considered.

[76] utilised voltage-time area (VTA) theory which is firstly put forward by [63] to predict CFs, but the impact of the phase shifts of the commutation voltages on the commutation process is not considered. [77] considered the CF prevention control system and the initial fault voltage angle (IFVA) when evaluating the CF risks. However, the phase shifts of the commutation voltages and the magnitude changes of non-faulty phase commutation voltages are neglected. [78] predicted the SCF also by using the VTA theory, but only the symmetrical three-phase fault conditions are considered.

[79][80] evaluated risks of CCFs by comparing the derived extinction angle and the minimum extinction angle. [81] analysed the criteria of CCF and then proposed an early warning method for CCF based on the Adaboost algorithm. [82] proposed a predictive method of CCF by comparing the actual commutation voltage and the threshold voltage which is derived from the constant extinction angle (CEA) control system. However, the above literature only consider the magnitude changes of the commutation voltages. [59] predicted CCFs by comparing the commutation voltage and its critical value which is obtained from the minimum extinction angle, but the phase shifts are not considered and only the symmetrical fault case is illustrated.

It can be concluded that little existing literature analyses the relationship between CF, especially CCF, and the phase and magnitude changes of all three commutation voltages under asymmetrical faults. It is well known that both the phase shifts and magnitude changes of commutation voltages can affect the commutation process. The study in Chapter 2 will also illustrate that both magnitudes and phases of the commutation voltages will change under asymmetrical faults in LCC-HVDC systems, for both faulty and non-faulty phases.

Table 1-1 shows the simulation results of changes of the commutation voltages of the inverter 1 during a phase-A SLG fault at the inverter bus with a fault impedance of 10 ohms. The system is modified from the four-machine-two-area system where the tie lines are replaced by two LCC-HVDC links as same as that in Chapter 2 (Figure 2-9). It can be seen that 1) under asymmetrical faults, magnitudes and phase angles of all commutation voltages have changed, and they are unbalanced; 2) the phase angle changes of the non-faulty phases are as large as 15 degrees; 3) The phase shift difference between the L-L commutation voltages is as large as 11 degrees. All these unbalanced magnitude changes and phase shifts have a significant impact on the commutation process.

Table 1-1 Simulation results of magnitude changes and phase shifts of commutation voltages under SLG faults

Under Phase	Phase Commutation Voltage			L-L Commutation Voltage		
A Fault	$\boldsymbol{E}_A$	$\boldsymbol{E}_B$	$\boldsymbol{E}_C$	$\boldsymbol{E}_{AB}$	$\boldsymbol{E}_{BC}$	$\boldsymbol{E}_{CA}$
Magnitude Change (p.u.) *	0.45	0.34	0.34	0.43	0.31	0.39
Phase Shift* (degree)	-15	-5	-13	-6	-9	-17

*Base value of the voltage magnitude is 230 kV for phase voltage. *Phase Shift: Negative values mean lagging.

Therefore, considering the changes of the magnitudes and phase angles of all three commutation voltages under asymmetrical faults is crucial for accurately predicting CFs, especially CCFs. A detailed study is presented in Chapter 4.

1.2.3 Immunity Index and Interaction Factor of Inverters in Multi-Infeed LCC-HVDC Systems

As mentioned above, the CCF, which indicates that the inverter keeps failing the commutations without a single cycle of successful commutations, is the most severe type of CFs that can cause inverter blocking and active power transfer accession [24], compared with FCF and

NCCF. In Multi-Infeed LCC-HVDC systems, the impact is even larger considering the high power transfer capacity of multiple LCC-HVDC links and the potential negative interactions between inverters that may cause CCFs. For instance, the overload of parallel lines has the risk of causing cascaded tripping [28].

Facing the above challenges, it is of significant importance to put forward a sufficient immunity index to estimate the immunity of the inverters to CCFs, and an interaction factor to quantify the interactions among the inverters in Multi-Infeed LCC-HVDC systems for CCFs under asymmetrical faults.

A lot of research has been conducted aiming at estimating the immunity and interactions of the inverters for CFs in Multi-Infeed LCC-HVDC systems.

[49][83] firstly proposed the immunity index (II), Commutation Failure II (CFII) which is the ratio of fault MVA to the rated active power transmitted by the HVDC, and Multi-Infeed Interaction Factor (MIIF) which is the ratio of the magnitude change of one inverter bus voltage to the 1% magnitude change of its adjacent inverter bus voltage, to characterize the immunity and interaction of the inverters in Multi-Infeed LCC-HVDC systems. [50] developed the concepts of Local CFII (LCFII) and Concurrent CFII (CCFII) by deriving the analytical expressions based on the minimum extinction angle criteria and Effective Short-Circuit Ratio (ESCR), and proposes an improved factor, the Weak Coupling MIIF (WCMIIF), to reflect the influence of the interactions of the inverters on CFs. [84] further developed LCFII and CCFII by considering the impact of voltage stability. [51] proposed the AC-DC Interaction Factor (ADIF) and Distortion ADIF (DADIF) to analytically evaluate the voltage depression-induced and distortion-induced CFs in Multi-Infeed LCC-HVDC systems, while the ADIF is utilised in [85] to analyse the CF risks in Multi-Infeed systems together with the factor Multi-Infeed

Interactive ESCR (MIESCR). ADIF and the minimum extinction angle criteria are used in [86] to examine successive CF risks in Multi-Infeed LCC-HVDC systems while taking into account the reactive power provided by the adjacent LCC-HVDC links. [87] assessed the influence of the coupling impedance on CFs in multi-infeed systems and then develops a decoupling method to simplify the analysis, with a target of transforming the multi-infeed system problem into the weakest Single-Infeed issue. By deriving the actual extinction angle as a function of MIIF, [88] utilizes the MIIF and CCFII as well as the minimum extinction angle criteria to estimate the interaction of the inverters in Multi-Infeed LCC-HVDC systems. Nevertheless, the phase shifts of the commutation voltages are not considered in the above studies.

[53][54] proposed the critical MIIF by using node impedance matrix and setting critical voltage drops on the basis of the minimum extinction angle, and evaluate the CF risks in Multi-Infeed LCC-HVDC systems. [89] put forward the AC-DC system Voltage Interaction Factor (ADVIF) and Critical ADVIF which are also based on the minimum extinction angle to identify the risks of CFs among the inverters when faults occur, by using the impedance matrix as well. The interaction factor expressed by the impedance matrix and the minimum extinction angle criteria is also utilised in [90] to estimate the interaction mechanism of CFs in Multi-Infeed LCC-HVDC systems. The area of severity for the simultaneous CF (AOS-CF) concept is suggested by [55] to present the CF risks for the inverters in Multi-Infeed systems by comparing the critical voltage drop and the voltage sag calculated through the impedance matrix under faults. However, the above research assesses the interaction of the inverters solely through the ratio of the voltage magnitude changes calculated by the impedance matrix, without considering the phase angles of the commutation voltages. [91] proposed the CF risk (CFR) and CF severity (CFS) concepts to evaluate the CF risks in Multi-Infeed LCC-HVDC systems considering the randomness of fault-occurrence time, although this method is simulation-based.

Nevertheless, the aforementioned studies primarily focus on the voltage magnitude changes of the inverter buses under the three-phase symmetrical fault when studying the interaction of inverters in Multi-Infeed LCC-HVDC systems, which cannot be applied when analysing the interactions under asymmetrical faults. Moreover, the existing research mainly focuses on general CFs, and there exists a great deficiency in the estimation and evaluation of the CCFs in Multi-Infeed LCC-HVDC systems, especially under asymmetrical faults.

Therefore, it is crucial to study the immunity and interaction of inverters in Multi-Infeed LCC-HVDC systems under asymmetrical faults with CCF risks considering the unbalanced commutation voltage magnitudes and phase angles. The detailed study is shown in Chapter 5.

1.2.4 PLL-Related Improvement for CF Suppression

The Phase-lock-loop (PLL) plays a vital role in the control systems of the LCC-HVDC system. PLL is designed to generate a saw-tooth waveform to cooperate with Alpha Order of Inverter (AOI) to output firing pulses for thyristor valves, to synchronize the converter voltages to the AC bus when the system is injected with disturbances, e.g., inverter side AC system faults.

To suppress the CFs which are mainly caused by the inverter side AC system faults, plenty of studies focused on the improvement of the AOI. [92] proposed the CFPREV system to advance the AOI to accelerate the firing instant, while [39] and [40] applied the Thevenin equivalent impedance and extra power component, respectively, to speed up the detection of AC faults and thus advance the firing instants. [93] utilised the arcsine value of the q-axis component of the PLL to supplement the AOI output of the control systems for mitigating the successive CFs in multi-terminal LCC-HVDC systems, but the output of the PLL is not discussed and the fault types are not specific.

Another group of studies aim to improve the PLL output to achieve the mitigation of CFs. [68]

proposed a new PLL model which includes an improved CFPREV system to mitigate the CFs; however, the impact of POW of the faults and the phase angle shift on the output of the control system is not developed. [71] improved the PLL output by deriving the sequence network diagram of the simplified inverter side of the LCC-HVDC system to mitigate the CFs. However, only the positive sequence components of the commutation voltages are utilised to compensate for the output of the PLL, and the impact of the unbalanced phase angle shifts of the commutation voltages and the impact of fault POW on PLL are not considered.

[93] mentioned the PLL dynamics would be varying and not always detrimental to the commutation process in unbalanced fault situations, but this study didn't analyse this issue. [94] stated that the phase and frequency of PLL will change under faults and proposes a new PLL topology by setting the estimated frequency fixed when a fault is detected to decouple the phase detection and frequency detection to realise the reduction of PLL frequency fluctuation and CF suppression during AC faults. However, the impact of the POW of faults on the PLL output is not considered.

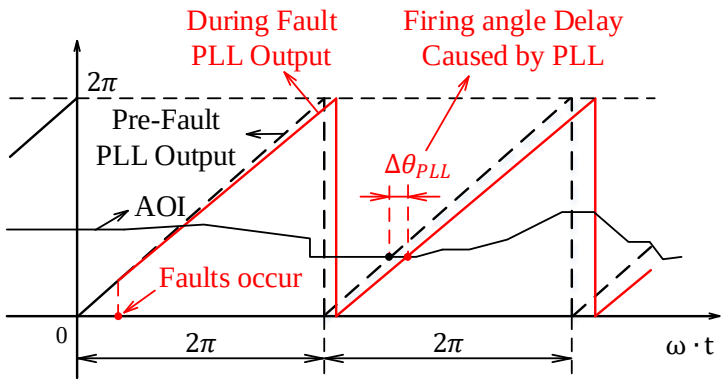


Figure 1-5 The PLL output and AOI under A-phase SLG fault at inverter side of CIGRE LCC-HVDC

However, in most of the studies about CF mitigation, the output of PLL is assumed to be unchanged. But in fact, it will change in fault cases. Figure 1-5 shows the PLL output under an A-phase SLG fault at the inverter side of the CIGRE LCC-HVDC Benchmark. It can be seen

that in this SLG fault case, the PLL output keeps lagging since the commutation voltages are lagging which has been illustrated in previous chapters. The lagging phase angles will finally postpone the firing instant for thyristor valves by $\Delta\theta_{PLL}$ which will further compress the margin of extinction angle. Once the real extinction angle is reduced below the minimum value, CFs will occur. Thus, the phase angle shift of the PLL has a significant impact on the commutation process. Besides, the POW of the faults would also affect PLL output, which will be explained in Chapter 6 in detail.

Therefore, it is vital to study the impact of AC faults on PLL output. Detailed analysis and a new PLL topology to prevent CFs are shown in Chapter 6.

1.2.5 Economic Analysis of LCC-HVDC Systems

As mentioned in Section 1.2.1, a lot of research has focused on the mitigation of CFs. Although these approaches can mitigate CFs to some extent, CF risks still exist. [66] shows a record of 1353 times of CFs occurring in 21 LCC-HVDC projects with a total capacity of 102GW during a 15-year period, from 2004 to 2018. One of the LCC-HVDC systems had as many as 24 times of CFs per year. As mentioned before, the active power cessation will cause a large demand-supply mismatch at both ends of the LCC-HVDC systems when CCFs occur and will cause overload problems to parallel AC systems [27][28]. Overall, there are still significant risks in CF and additional research is needed to find out an optimum strategy to eliminate CFs.

To solve this problem, [24] proposed a new LCC-HVDC topology by inserting controllable capacitor modules into the secondary side of the converter transformer to eliminate CFs. [29] presented a thyristor-based controllable capacitor (TBCC) module to realise CF elimination in ultra-high voltage direct current (UHVDC) systems. To further strengthen the applicability of the controllable capacitor-based LCC-HVDC (CC LCC-HVDC) systems, [95] suggested the

strategies of reactive power control and AC voltage control. Based on the CC LCC-HVDC topology, [96] developed an improved AC Filterless CC LCC-HVDC (ACFL-CC LCC-HDVC) topology by inserting parallel capacitors between phases at the secondary side of the converter transformer. Aside from the capacity to eliminate CFs, this topology also provides the following advantages: 1) no filter is required; 2) 50% HVDC station footprint is saved; 3) voltage rating of controllable capacitor modules is reduced; 4) lower reactive power transmitted through the converter transformer is achieved.

The technical performance has been discussed in detail in the above-mentioned studies. However, conducting an economic analysis of the above Flexible LCC-HVDC topologies is also crucial to facilitating their implementation in practice. As one of the common economic analysis methods, the life-cycle cost analysis (LCCA) was firstly introduced by the General Accounting Office of the United States in the 1930s [97]. It was gradually applied in the electric power industry over 20 years [98], mainly focusing on the off-shore wind farms [99] - [101], the transmission lines [102], and the converter transformer [103].

Although some other studies have examined the economics of HVDC systems [104] - [106], the majority of them have concentrated on voltage-sourced converter based HVDC (VSC-HVDC) and modular multi-level converter based HVDC (MMC-HVDC) systems. Few published papers have been found to attempt to analyse the cost of these Flexible LCC-HVDC topologies as mentioned above, particularly with detailed calculations and comparisons, which makes it difficult to evaluate the practicality and applicability of these topologies which can provide extra voltage by inserting additional devices for eliminating CFs.

Therefore, it is significant to figure out the economic analysis of the Flexible LCC-HVDC topology to verify the feasibility and applicability of “extra voltage” approaches of preventing

CFs in real LCC-HVDC projects. Detailed analysis is depicted in Chapter 7.

1.3 Simulation Validation Tool - RTDS

RTDS is used in this thesis to demonstrate the effectiveness of the proposed mathematical CF prediction and mitigation methods. RTDS can perform Electromagnetic Transient (EMT) simulations continuously in real time, and it is able to simulate complicated networks with a typical timestep of 25–50 μs, or subnetworks with a smaller timestep of 1-4 μs. The hardware consists of a multicore CPU placed in chassis, which makes it simple to expand the Simulator's computing capability when needed. It provides models of each part of power systems with customised parameters, e.g., synchronous generators, transmission lines, transformers, thyristor valves, etc., and a few of typical benchmarks, e.g., LCC-HVDC Benchmark. Simulations for analytical experiments can be performed more quickly using the RTDS Simulator than with offline EMT simulation software.

However, it needs to be noticed that RTDS (or any other offline EMT simulation software) is not suitable for simulating practical scenarios due to the large scale and complexity of the actual power system and various types of faults as well as innumerable potential fault points because processors in RTDS have limited computational capability and are costly (other offline EMT simulators take too much time for simulations), and consequently it is not capable of fully simulating the actual power grid, and all fault scenarios. In other words, it is essentially impossible to use RTDS to make predictions of CFs in large grids in real world scenarios.

Therefore, the RTDS is only used to validate the accuracy and effectiveness of the proposed mathematical methods and topology in this thesis.

Besides, another disadvantage of RTDS is the limited timestep from 25–50 μs, i.e., 0.45° - 0.9°

in the 50Hz systems. On the basis of one cycle, i.e., 360°, this time step will bring an error of up to 0.9°, which means an error of 0.25% when measuring the phase angles.

1.4 Research Aim and Objectives, Contributions, and Thesis Overview

1.4.1 Research Aim and Objectives

The aim of this research is to improve the predictability of CFs in LCC-HVDC systems by considering the changes of all three phase commutation voltages under asymmetrical faults and to mitigate CFs by proposing new control topologies. The objectives are:

Objective 1: Develop a more accurate method for predicting CFs and CCFs under asymmetrical faults considering non-faulty phase commutation voltage changes to improve the predictability of the LCC-HVDC systems.

Objective 2: Study the immunity of inverters to CCFs and the interactions between inverters under faults with CCF risks in Multi-Infeed LCC-HVDC systems. Propose a new Immunity Index and a new Interaction Factor to accurately estimate the inverter performance under asymmetrical faults by considering the non-faulty phase commutation voltage changes.

Objective 3: Research the methods to prevent CFs and propose new PLL topologies to eliminate the detrimental impact of PLL on the commutation process caused by the imbalance of commutation voltages under asymmetrical faults.

Objective 4: Develop an economic analysis framework based on the Life-Cycle Cost Analysis method for the LCC-HVDC topologies that can eliminate CF risks in LCC-HVDC systems.

1.4.2 Contributions

1. New methods of predicting CFs in Multi-Infeed LCC-HVDC systems are proposed

through accurately calculating the commutation voltages by considering the magnitude changes and phase angle shifts of both faulty and non-faulty phases under asymmetrical faults. Existing research as mentioned in Section 1.2.1 did not consider the phase angle shifts of non-faulty phases which in fact have a significant impact on the commutation process, and the error of the CF prediction in this thesis is reduced by as large as 62% compared with existing research. The proposed mathematical CF prediction methods can not only enable researchers to realise the importance of considering the phase shifts and magnitude changes of non-faulty phase commutation voltages under asymmetrical faults when predicting CFs, but also be applied to actual large-scale power systems for fast and accurate CF predictions which could help system operators design and upgrade LCC-HVDC projects.

2. A new approach to predicting continuous commutation failures (CCFs) in Multi-Infeed LCC-HVDC systems is proposed by utilizing the proposed Asymmetrical Advancing Angle (AAA). AAA can accurately quantify the adverse impact of the magnitude changes and phase angle shifts on the subsequent commutations after the First CF (FCF). Little existing literature focused on the prediction of CCFs which are more serious to the stability of the LCC-HVDC systems than the non-continuous CFs (NCCFs). The CCF prediction accuracy of the proposed method in this thesis is 67% more accurate than previous approaches as mentioned in Section 1.2.2. The proposed mathematical CCF prediction method helps researchers understand the quantitative effect of the imbalance of the phase shifts on the commutations under asymmetrical faults, and can be used to fast and accurately predict CCFs in actual power grids.
3. A new Immunity Index for CCF (IICCF) is proposed for evaluating the immunity of the inverters to CCF risks in LCC-HVDC systems based on the VTA method. A new

Interaction Factor for inverters under faults with CCF risks (IFCCF) is further proposed based on IICCF to describe the interaction between inverters in Multi-Infeed LCC-HVDC systems under asymmetrical faults. IICCF and IFCCF can accurately estimate the LCC-HVDC inverter performance under unbalanced faults that will cause CCFs, by taking into account the magnitude changes and phase angle shifts of both faulty and non-faulty phase commutation voltages under asymmetrical faults, which are not considered by existing literature. The two indices could enable researchers to comprehend the safety margin within which the inverters will operate without CCF risks, and help system operators to identify the CCF risk areas in large Multi-Infeed LCC-HVDC systems.

4. An improved PLL topology is proposed to mitigate CFs. This topology considers the impact of the phase angles of the commutation voltages and the impact of the POW of AC faults on PLL output under unbalanced faults. The proposed PLL topology can eliminate the detrimental impact of the PLL output on the commutation process caused by the asymmetrical faults, which is not considered by existing research. This research shows the importance of taking into account the phase shifts and AOI when studying the PLL for the purpose of suppressing CFs, and the proposed FIM-PLL can be applied in large-scale complex power networks with LCC-HVDC links to achieve the CF mitigation.
5. An economic analysis framework based on the Life-Cycle Cost Analysis method is developed for Flexible LCC-HVDC topologies that provide extra voltage by inserting addition devices for eliminating CFs. The life cycle cost comparisons show that the Flexible LCC-HVDC topologies can not only eliminate the cost caused by CFs, but also reduce the inverter station cost by up to 18% compared with the conventional LCC-

HVDC topology, which proves that the CF elimination approach is economic and practicable.

1.4.3 Thesis Overview

This thesis is accomplished by using theoretical analysis and Real-Time Digital Simulator (RTDS) simulations. It needs to be noted that the RTDS is designed to perform real-time EMT simulations continuously in real time and is capable of simulating complex networks using a typical timestep of 25-50 μs. Analytical studies using RTDS can be performed much faster than with offline EMT simulation programs.

The structure of this thesis is shown below:

Chapter 2 proposes a new CF prediction method for Multi-Infeed LCC-HVDC systems. The importance of the magnitude changes and phase angle shifts of both faulty and non-faulty phase commutation voltages are presented. Then a new calculation method for commutation voltages at the inverter side is presented and verified. The CF prediction criterion is then proposed based on the VTA method. Finally, the accuracy of this CF prediction method is demonstrated through simulation results based on RTDS, and potential approaches to prevent CFs are suggested. (**Objective 1**)

Chapter 3 develops the sequence network diagram of the 12-pulse LCC-HVDC inverter under asymmetrical faults which can accurately calculate the magnitudes and phase angles of three phase commutation voltages. Detailed derivation steps are illustrated and simulation demonstrates that the calculation results have smaller errors than the method in Chapter 2. (**Objective 1**)

Chapter 4 proposes a new CCF prediction method for Multi-Infeed LCC-HVDC systems. The

detailed commutation process of CCF after the FCF is illustrated by analysing the impact of the magnitude changes and phase angle shifts as well as the impact of the control systems on CCFs. New concepts of Asymmetrical Advancing Angle (AAA) and AAA Difference (AAAD) are proposed to help describe the impact of the commutation voltage imbalance on the commutation process. The criterion for predicting CCFs is then proposed and verified by the simulation of a Multi-Infeed LCC-HVDC system. Finally, potential CCF elimination approaches and applications of the proposed CCF prediction method are discussed. (**Objective 1**)

Chapter 5 proposes a new Immunity Index of the inverter for CCF (IICCF) for LCC-HVDC systems and a new Interaction Factor for inverters under faults with CCF risks (IFCCF) for Multi-Infeed LCC-HVDC systems. IICCF and IFCCF are quantitative indices that describe the performance of the inverters under asymmetrical faults with CCF risks. Different from existing approaches, these two concepts consider the magnitude changes and phase angle shifts of all commutation voltages under unbalanced faults, and thus, IICCF can sufficiently describe the immunity of the inverter to CCFs in asymmetrical fault cases and the IFCCF can be used to predict the CCFs risks for inverters in Multi-Infeed LCC-HVDC system by comparing the Critical IFCCF (CIFCCF) which can be obtained directly by IICCF of the inverters. In the end, the accuracy of the proposed factor is verified by simulations based on RTDS. (**Objective 2**)

Chapter 6 proposes an improved PLL topology to eliminate the adverse impact of AC faults on PLL and mitigate CFs. The impact of the unbalanced phase angles of commutation voltages as well as the impact of Point on Wave (POW) of the faults on the PLL output are theoretically analysed. The interesting fact that the PLL does not always have an adverse effect on the commutation process under faults is illustrated. Then an improved PLL topology is proposed

to eliminate the detrimental influence of delaying the PLL output phase angles due to the asymmetrical faults and consequently mitigate the CFs. Finally, through comparing the new PLL topology with conventional LCC-HVDC PLL and CF Prevention (CFPREV) control system, the feasibility of the proposed PLL to prevent CFs is demonstrated by simulations based on RTDS. (**Objective 3**)

Chapter 7 carries out the economic analysis of one of the CF elimination methods - providing extra voltage for the commutations under faults which is proposed in Chapter 2, and the need of inserting additional devices to provide extra voltage for successful commutations is discussed in Chapter 6. Although this extra voltage is realised by existing research through inserting controllable capacitors to eliminate CFs, it is still meaningful to develop an economic analysis to study the practicality and applicability of the 'extra voltage' approach. The Life-Cycle Cost Analysis (LCCA) method is applied for the economic analysis and the total cost of the conventional LCC-HVDC topology and three Flexible LCC-HVDC topologies are compared under multiple scenarios with different discount rates, fault impedance, and redundancies. In the end, a series of factors that affect the Life-Cycle Cost are discussed. (**Objective 4**)

Chapter 8 summarises the conclusions and potential future work is discussed.

Relationships between chapters:

The CCF prediction method proposed in **Chapter 4** is based on the commutation voltage analysis in **Chapter 2** & **Chapter 3**.

The Immunity Index for CCF (IICCF) and Interaction Factor for CCF (IFCCF) in **Chapter 5**

is based on the CCF analysis and prediction in **Chapter 4**.

The idea of the new PLL topology to prevent CFs by advancing the firing instants in **Chapter 6** is from the commutation process analysis in **Chapter 2** & **Chapter 4**.

Chapter 2 quantifies the extra voltage for avoiding CFs which can be provided by additional devices, and **Chapter 6** discusses the need of such extra voltage in preventing CFs. Although this extra voltage is realised by other researchers through inserting additional controllable capacitors to eliminate CFs, it is still meaningful to develop an economic analysis to study the practicality and applicability of the 'extra voltage' approach, since there is a significant lack of economic analysis about such CF elimination approaches by inserting additional devices. Therefore, **Chapter 7** develops an economic analysis framework of the LCC-HVDC with controllable capacitors that provide extra voltage to avoid CFs, to study the applicability of the idea of 'extra voltage' proposed in **Chapter 2**.

CHAPTER 2 Commutation Failure Prediction for Multi-Infeed LCC-HVDC Systems

2.1 Introduction

As mentioned in Section 1.2.1, the magnitudes and phase angle shifts of the commutation voltages have a direct impact on the commutation process. However, there is a significant lack of research on the non-faulty phase commutation voltage changes under unbalanced faults. Thus, the magnitude changes and the phase angle shifts of both faulty phase and non-faulty phase commutation voltages for LCC-HVDC systems under asymmetrical faults need to be studied.

Therefore, this chapter aims to develop a method for predicting CFs considering the magnitude changes and phase shifts of faulty and non-faulty phase voltages during SLG faults, and then derive the extra voltage expression for successful commutations to quantify ‘how close’ the commutations are to being successful.

The structure of this chapter is organised as below: Section 2.2 derives and verifies the calculation results of the phase angles and magnitudes of the commutation voltages under SLG faults. Then the prediction criterion for CF based on the VTA method and extra commutation voltage to avoid CFs are proposed in Section 2.3. Section 2.4 presents the simulation results to validate the effectiveness of the proposed method and Section 2.5 summarises this chapter.

2.2 Calculation of Commutation Voltages During SLG Faults

2.2.1 Test System

In this section, the CIGRE LCC-HVDC Benchmark system in [107] is utilised to explain the proposed method. As shown in Figure 2-1, a transmission line is added between the inverter AC bus and the AC source. A Single-Line-Ground (SLG) fault along the transmission line is considered when calculating the commutation voltages during the fault. The main parameters for the model are shown in [107] and Table 2-1.

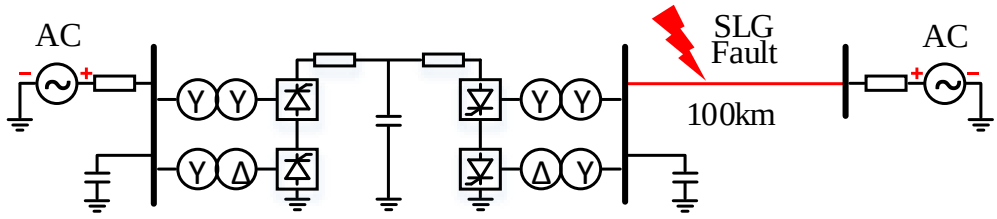


Figure 2-1 The modified 12-pulse CIGRE LCC-HVDC Benchmark model

Table 2-1 Parameters of Inverter Side of LCC-HVDC

Parameters	Value
Rated DC Voltage	500 kV
Rated Active Power Transmitted by HVDC	1000 MW
AC System Frequency	50 Hz
Voltage Ratings (Primary/Secondary) of Each Transformer at Inverter Side (Line-to-Line, RMS)	230 kV/211 kV
Voltage Ratings (Primary/Secondary) of Each Transformer at Rectifier Side (Line-to-Line, RMS)	345 kV/211 kV
Leakage Reactance of all Transformers (with the Power Base of 100 MVA)	0.18 p.u.
Rated Inverter Bus Voltage (Line-to-Line, RMS)	230 kV
Rated Rectifier Bus Voltage (Line-to-Line, RMS)	345 kV

DC Side Smoothing Reactance at Each End	0.5968 H
Total DC Transmission Line Impedance	5 ohm
Capacitors Connected to the Inverter Bus per Phase	7.522 uF
Resistance of Transmission Line per Phase per km	0.028 ohm
Inductive Reactance of Transmission Line per Phase per km	0.2708 ohm

2.2.2 Three Line Diagram of the Inverter Side

To calculate the commutation voltages during the SLG fault, the inverter side of the 12-pulse LCC-HVDC system is analysed in this chapter, as shown in Figure 2-2. A phase-A SLG fault is assumed to occur at a certain point along the transmission line. $\boldsymbol{Z}_{TL}$ is the total impedance of the transmission line for each phase. m is the ratio of the length of the transmission line between the fault point and the inverter bus to the total length. The capacitor banks and AC filters are represented by $\boldsymbol{Z}_C$.

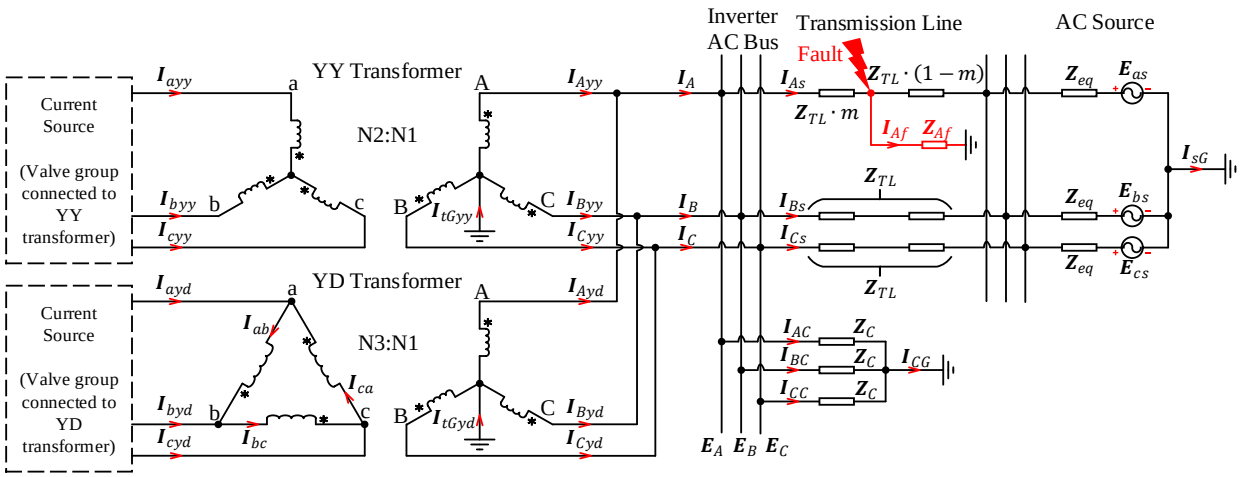


Figure 2-2 The three-line diagram of the inverter side of the LCC-HVDC system.

2.2.3 Derivation of Commutation Voltages

Applying Kirchhoff's Current Law (KCL), the relationships among currents in the AC system,

YY transformer, and YD transformer can be expressed by:

1). AC system:

$$\boldsymbol{I}_A = \boldsymbol{I}_{Ayy} + \boldsymbol{I}_{Ayd} = \boldsymbol{I}_{AC} + \boldsymbol{I}_{As} = \frac{N2}{N1} \cdot \boldsymbol{I}_{ayy} + \frac{N3}{N1} \cdot \boldsymbol{I}_{ab} \tag{2-1}$$

$$\boldsymbol{I}_B = \boldsymbol{I}_{Byy} + \boldsymbol{I}_{Byd} = \boldsymbol{I}_{BC} + \boldsymbol{I}_{Bs} = \frac{N2}{N1} \cdot \boldsymbol{I}_{byy} + \frac{N3}{N1} \cdot \boldsymbol{I}_{bc} \tag{2-2}$$

$$\boldsymbol{I}_C = \boldsymbol{I}_{Cyy} + \boldsymbol{I}_{Cyd} = \boldsymbol{I}_{CC} + \boldsymbol{I}_{Cs} = \frac{N2}{N1} \cdot \boldsymbol{I}_{cyy} + \frac{N3}{N1} \cdot \boldsymbol{I}_{ca} \tag{2-3}$$

$$\boldsymbol{I}_{tGyy} + \boldsymbol{I}_{tGyd} = \boldsymbol{I}_{CG} + \boldsymbol{I}_{Af} + \boldsymbol{I}_{sG} \tag{2-4}$$

where all the currents with directions can be found in Figure 2-2.

And the commutation voltages $\boldsymbol{E}_A$, $\boldsymbol{E}_B$, and $\boldsymbol{E}_C$ (voltages at inverter bus) can be expressed as:

$$\boldsymbol{E}_A = \left[\boldsymbol{Z}_C // (\boldsymbol{Z}_L + \boldsymbol{Z}_{Af} // \boldsymbol{Z}_R)\right] \cdot \boldsymbol{I}_A + \frac{(\boldsymbol{Z}_C + \boldsymbol{Z}_L) // \boldsymbol{Z}_{Af}}{\boldsymbol{Z}_R + (\boldsymbol{Z}_C + \boldsymbol{Z}_L) // \boldsymbol{Z}_{Af}} \cdot \frac{\boldsymbol{Z}_C}{\boldsymbol{Z}_C + \boldsymbol{Z}_L} \cdot \boldsymbol{E}_{as} \tag{2-5}$$

$$\boldsymbol{E}_B = [\boldsymbol{Z}_C // (\boldsymbol{Z}_L + \boldsymbol{Z}_R)] \cdot \boldsymbol{I}_B + \frac{\boldsymbol{Z}_C}{\boldsymbol{Z}_C + \boldsymbol{Z}_L + \boldsymbol{Z}_R} \cdot \boldsymbol{E}_{bs} \tag{2-6}$$

$$\boldsymbol{E}_C = [\boldsymbol{Z}_C // (\boldsymbol{Z}_L + \boldsymbol{Z}_R)] \cdot \boldsymbol{I}_C + \frac{\boldsymbol{Z}_C}{\boldsymbol{Z}_C + \boldsymbol{Z}_L + \boldsymbol{Z}_R} \cdot \boldsymbol{E}_{cs} \tag{2-7}$$

where '//' means paralleling of the two impedance, and

$$\boldsymbol{Z}_L = \boldsymbol{Z}_{TL} \cdot m \tag{2-8}$$

$$\boldsymbol{Z}_R = \boldsymbol{Z}_{TL} \cdot (1 - m) + \boldsymbol{Z}_{eq} \tag{2-9}$$

2). YY transformer:

$$\boldsymbol{I}_{Ayy} = \frac{N2}{N1} \cdot \boldsymbol{I}_{ayy}, \quad \boldsymbol{I}_{Byy} = \frac{N2}{N1} \cdot \boldsymbol{I}_{byy}, \quad \boldsymbol{I}_{Cyy} = \frac{N2}{N1} \cdot \boldsymbol{I}_{cyy} \tag{2-10}$$

$$\boldsymbol{I}_{Ayy} + \boldsymbol{I}_{Byy} + \boldsymbol{I}_{Cyy} = \boldsymbol{I}_{tGyy}, \quad \boldsymbol{I}_{ayy} + \boldsymbol{I}_{byy} + \boldsymbol{I}_{cyy} = 0 \tag{2-11}$$

3). YD transformer:

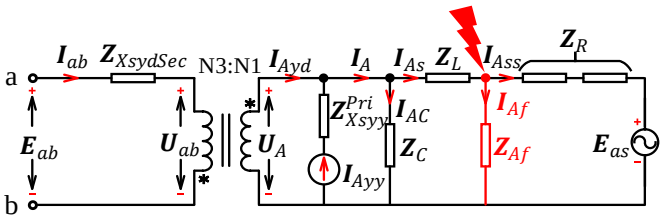
$$\boldsymbol{I}_{Ayd} = \frac{N3}{N1} \cdot \boldsymbol{I}_{ab}, \quad \boldsymbol{I}_{Byd} = \frac{N3}{N1} \cdot \boldsymbol{I}_{bc}, \quad \boldsymbol{I}_{Cyd} = \frac{N3}{N1} \cdot \boldsymbol{I}_{ca} \tag{2-12}$$

$$\boldsymbol{I}_{ab} = \boldsymbol{I}_{ayd} + \boldsymbol{I}_{ca}, \quad \boldsymbol{I}_{bc} = \boldsymbol{I}_{byd} + \boldsymbol{I}_{ab}, \quad \boldsymbol{I}_{ca} = \boldsymbol{I}_{cyd} + \boldsymbol{I}_{bc} \tag{2-13}$$

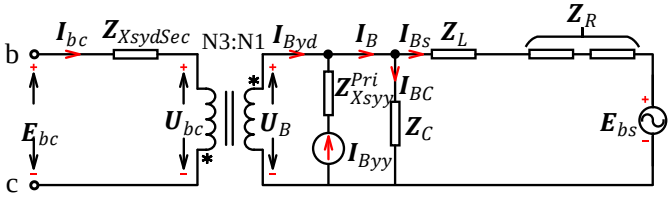
$$\boldsymbol{I}_{Ayd} + \boldsymbol{I}_{Byd} + \boldsymbol{I}_{Cyd} = \boldsymbol{I}_{tGyd}, \quad \boldsymbol{I}_{ayd} + \boldsymbol{I}_{byd} + \boldsymbol{I}_{cyd} = 0 \tag{2-14}$$

where $\frac{N2}{N1}$ and $\frac{N3}{N1}$ are the turns ratios of the secondary side to the primary side of the YY and YD transformer, respectively.

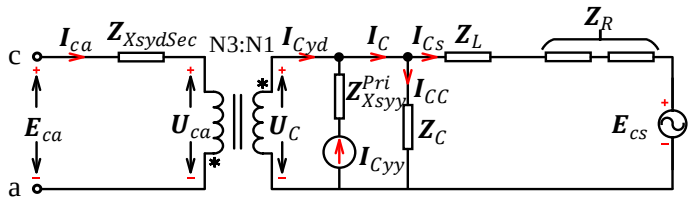
To derive the phase currents at the secondary side of the YD transformer ($\boldsymbol{I}_{ab}$, $\boldsymbol{I}_{bc}$, and $\boldsymbol{I}_{ca}$ in Figure 2-2), the equivalent diagrams for phase A, B, and C during phase-A faults are shown in Figure 2-3.



(a) The Phase A Circuit Diagram



(b) The Phase B Circuit Diagram



(c) The Phase C Circuit Diagram

Figure 2-3 The A, B, and C phase diagrams of the system looking into the secondary side of the YD transformer.

Then the voltages across each secondary winding can be calculated as:

$$\boldsymbol{E_{ab}} = \boldsymbol{I_{ab}} \cdot \boldsymbol{Z_{XsydSec}} + \frac{N3}{N1} \cdot \left(\frac{N2}{N1} \cdot \boldsymbol{I_{ayy}} + \frac{N3}{N1} \cdot \boldsymbol{I_{ab}} + \frac{\boldsymbol{Z_{Af}} // \boldsymbol{Z_R}}{\boldsymbol{Z_L} + \boldsymbol{Z_{Af}} // \boldsymbol{Z_R}} \cdot \frac{\boldsymbol{E_{as}}}{\boldsymbol{Z_R}}\right) \cdot \left[\boldsymbol{Z_C} // (\boldsymbol{Z_L} + \boldsymbol{Z_{Af}} // \boldsymbol{Z_R})\right] \quad (2\text{-}15)$$

$$\boldsymbol{E_{bc}} = \boldsymbol{I_{bc}} \cdot \boldsymbol{Z_{XsydSec}} + \frac{N3}{N1} \cdot \left(\frac{N2}{N1} \cdot \boldsymbol{I_{byy}} + \frac{N3}{N1} \cdot \boldsymbol{I_{bc}} + \frac{\boldsymbol{E_{bs}}}{\boldsymbol{Z_L} + \boldsymbol{Z_R}}\right) \cdot \left[\boldsymbol{Z_C} // (\boldsymbol{Z_L} + \boldsymbol{Z_R})\right] \quad (2\text{-}16)$$

$$\boldsymbol{E_{ca}} = \boldsymbol{I_{ca}} \cdot \boldsymbol{Z_{XsydSec}} + \frac{N3}{N1} \cdot \left(\frac{N2}{N1} \cdot \boldsymbol{I_{cyy}} + \frac{N3}{N1} \cdot \boldsymbol{I_{ca}} + \frac{\boldsymbol{E_{cs}}}{\boldsymbol{Z_L} + \boldsymbol{Z_R}}\right) \cdot \left[\boldsymbol{Z_C} // (\boldsymbol{Z_L} + \boldsymbol{Z_R})\right] \quad (2\text{-}17)$$

Figure 2-4 presents the equivalent circuit of the secondary side of the YD transformer:

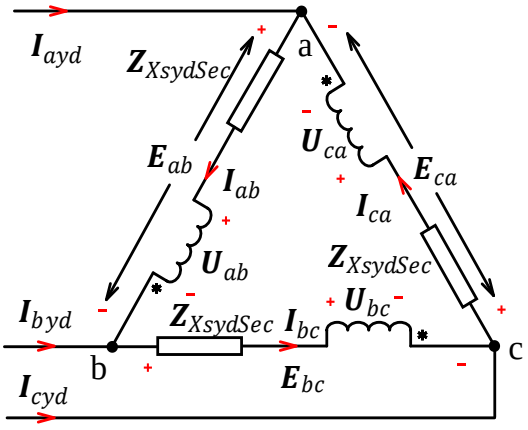


Figure 2-4 The inner loop circuit diagram of the secondary side of YD transformer.

After applying KVL, the phase currents within the inner loop can be calculated based on (2-1)-

(2-3) and (2-10)-(2-17):

$$\boldsymbol{I}_{ab} = \frac{\boldsymbol{Z}_{ca}}{\boldsymbol{Z}_{ab}+\boldsymbol{Z}_{bc}+\boldsymbol{Z}_{ca}} \cdot \boldsymbol{I}_{ayd} + \frac{-\boldsymbol{Z}_{bc}}{\boldsymbol{Z}_{ab}+\boldsymbol{Z}_{bc}+\boldsymbol{Z}_{ca}} \cdot \boldsymbol{I}_{byd} + \frac{-(\boldsymbol{V}_{sa}+\boldsymbol{V}_{sb}+\boldsymbol{V}_{sc})}{\boldsymbol{Z}_{ab}+\boldsymbol{Z}_{bc}+\boldsymbol{Z}_{ca}} \quad (2\text{-}18)$$

$$\boldsymbol{I}_{bc} = \frac{\boldsymbol{Z}_{ca}}{\boldsymbol{Z}_{ab}+\boldsymbol{Z}_{bc}+\boldsymbol{Z}_{ca}} \cdot \boldsymbol{I}_{ayd} + \frac{\boldsymbol{Z}_{ab}+\boldsymbol{Z}_{ca}}{\boldsymbol{Z}_{ab}+\boldsymbol{Z}_{bc}+\boldsymbol{Z}_{ca}} \cdot \boldsymbol{I}_{byd} + \frac{-(\boldsymbol{V}_{sa}+\boldsymbol{V}_{sb}+\boldsymbol{V}_{sc})}{\boldsymbol{Z}_{ab}+\boldsymbol{Z}_{bc}+\boldsymbol{Z}_{ca}} \quad (2\text{-}19)$$

$$\boldsymbol{I}_{ca} = \frac{-(\boldsymbol{Z}_{ab}+\boldsymbol{Z}_{bc})}{\boldsymbol{Z}_{ab}+\boldsymbol{Z}_{bc}+\boldsymbol{Z}_{ca}} \cdot \boldsymbol{I}_{ayd} + \frac{-\boldsymbol{Z}_{bc}}{\boldsymbol{Z}_{ab}+\boldsymbol{Z}_{bc}+\boldsymbol{Z}_{ca}} \cdot \boldsymbol{I}_{byd} + \frac{-(\boldsymbol{V}_{sa}+\boldsymbol{V}_{sb}+\boldsymbol{V}_{sc})}{\boldsymbol{Z}_{ab}+\boldsymbol{Z}_{bc}+\boldsymbol{Z}_{ca}} \quad (2\text{-}20)$$

where

$$\boldsymbol{Z}_{ab} = \boldsymbol{Z}_{XsydSec} + \left(\frac{N3}{N1}\right)^2 \cdot \left[\boldsymbol{Z}_C // (\boldsymbol{Z}_L + \boldsymbol{Z}_{Af} // \boldsymbol{Z}_R)\right] \quad (2\text{-}21)$$

$$\boldsymbol{Z}_{bc} = \boldsymbol{Z}_{XsydSec} + \left(\frac{N3}{N1}\right)^2 \cdot [\boldsymbol{Z}_C // (\boldsymbol{Z}_L + \boldsymbol{Z}_R)] \quad (2\text{-}22)$$

$$\boldsymbol{Z}_{ca} = \boldsymbol{Z}_{XsydSec} + \left(\frac{N3}{N1}\right)^2 \cdot [\boldsymbol{Z}_C // (\boldsymbol{Z}_L + \boldsymbol{Z}_R)] \quad (2\text{-}23)$$

$$\boldsymbol{V}_{sa} = \frac{N3}{N1} \cdot \left(\frac{N2}{N1} \cdot \boldsymbol{I}_{ayy} + \frac{\boldsymbol{Z}_{Af} // \boldsymbol{Z}_R}{\boldsymbol{Z}_L + \boldsymbol{Z}_{Af} // \boldsymbol{Z}_R} \cdot \frac{\boldsymbol{E}_{as}}{\boldsymbol{Z}_R}\right) \cdot \left[\boldsymbol{Z}_C // (\boldsymbol{Z}_L + \boldsymbol{Z}_{Af} // \boldsymbol{Z}_R)\right] \quad (2\text{-}24)$$

$$\boldsymbol{V}_{sb} = \frac{N3}{N1} \cdot \left(\frac{N2}{N1} \cdot \boldsymbol{I}_{byy} + \frac{\boldsymbol{E}_{bs}}{\boldsymbol{Z}_L + \boldsymbol{Z}_R}\right) \cdot [\boldsymbol{Z}_C // (\boldsymbol{Z}_L + \boldsymbol{Z}_R)] \quad (2\text{-}25)$$

$$\boldsymbol{V}_{sc} = \frac{N3}{N1} \cdot \left(\frac{N2}{N1} \cdot \boldsymbol{I}_{cyy} + \frac{\boldsymbol{E}_{cs}}{\boldsymbol{Z}_L + \boldsymbol{Z}_R}\right) \cdot [\boldsymbol{Z}_C // (\boldsymbol{Z}_L + \boldsymbol{Z}_R)] \quad (2\text{-}26)$$

Applying (2-1)-(2-3) and (2-18)-(2-20) to (2-5)-(2-7), the commutation voltages are calculated

$$\boldsymbol{E}_A = \frac{(\boldsymbol{Z}_C + \boldsymbol{Z}_L) // \boldsymbol{Z}_{Af}}{\boldsymbol{Z}_R + (\boldsymbol{Z}_C + \boldsymbol{Z}_L) // \boldsymbol{Z}_{Af}} \cdot \frac{\boldsymbol{Z}_C}{\boldsymbol{Z}_C + \boldsymbol{Z}_L} \cdot \boldsymbol{E}_{as} + \left[\boldsymbol{Z}_C // (\boldsymbol{Z}_L + \boldsymbol{Z}_{Af} // \boldsymbol{Z}_R)\right] \cdot \left\{\frac{N2}{N1} \cdot \boldsymbol{I}_{ayy} \quad (2\text{-}27)\right.$$

$$+\frac{N3}{N1}\cdot\left[\frac{\boldsymbol{Z}_{ca}}{\boldsymbol{Z}_{ab}+\boldsymbol{Z}_{bc}+\boldsymbol{Z}_{ca}}\cdot\boldsymbol{I}_{ayd}+\frac{-\boldsymbol{Z}_{bc}}{\boldsymbol{Z}_{ab}+\boldsymbol{Z}_{bc}+\boldsymbol{Z}_{ca}}\cdot\boldsymbol{I}_{byd}+\frac{-(\boldsymbol{V}_{sa}+\boldsymbol{V}_{sb}+\boldsymbol{V}_{sc})}{\boldsymbol{Z}_{ab}+\boldsymbol{Z}_{bc}+\boldsymbol{Z}_{ca}}\right]\right\}$$

$$\begin{aligned}\boldsymbol{E}_B=&\frac{\boldsymbol{Z}_C}{\boldsymbol{Z}_C+\boldsymbol{Z}_L+\boldsymbol{Z}_R}\cdot\boldsymbol{E}_{bs}+[\boldsymbol{Z}_C//(\boldsymbol{Z}_L+\boldsymbol{Z}_R)]\cdot\left\{\frac{N2}{N1}\cdot\boldsymbol{I}_{byy}\right.\\&\left.+\frac{N3}{N1}\cdot\left[\frac{\boldsymbol{Z}_{ca}}{\boldsymbol{Z}_{ab}+\boldsymbol{Z}_{bc}+\boldsymbol{Z}_{ca}}\cdot\boldsymbol{I}_{ayd}+\frac{\boldsymbol{Z}_{ab}+\boldsymbol{Z}_{ca}}{\boldsymbol{Z}_{ab}+\boldsymbol{Z}_{bc}+\boldsymbol{Z}_{ca}}\cdot\boldsymbol{I}_{byd}+\frac{-(\boldsymbol{V}_{sa}+\boldsymbol{V}_{sb}+\boldsymbol{V}_{sc})}{\boldsymbol{Z}_{ab}+\boldsymbol{Z}_{bc}+\boldsymbol{Z}_{ca}}\right]\right\}\end{aligned}\tag{2-28}$$

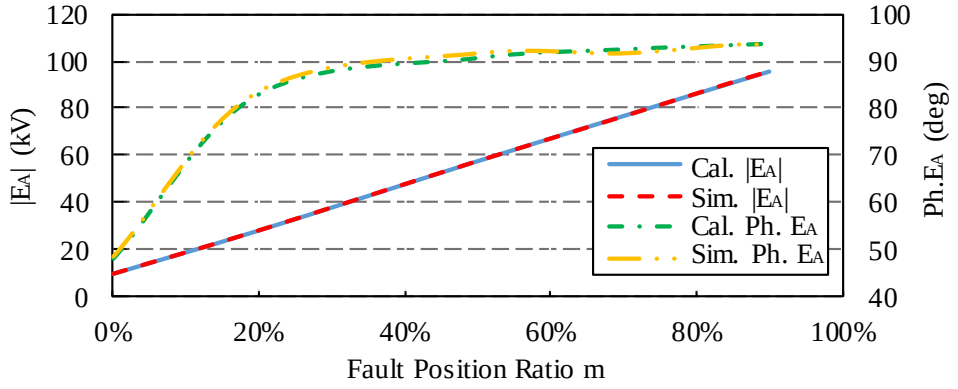
$$\begin{aligned}\boldsymbol{E}_C=&\frac{\boldsymbol{Z}_C}{\boldsymbol{Z}_C+\boldsymbol{Z}_L+\boldsymbol{Z}_R}\cdot\boldsymbol{E}_{cs}+[\boldsymbol{Z}_C//(\boldsymbol{Z}_L+\boldsymbol{Z}_R)]\cdot\left\{\frac{N2}{N1}\cdot\boldsymbol{I}_{cyy}\right.\\&\left.+\frac{N3}{N1}\cdot\left[\frac{-(\boldsymbol{Z}_{ab}+\boldsymbol{Z}_{bc})}{\boldsymbol{Z}_{ab}+\boldsymbol{Z}_{bc}+\boldsymbol{Z}_{ca}}\cdot\boldsymbol{I}_{ayd}+\frac{-\boldsymbol{Z}_{bc}}{\boldsymbol{Z}_{ab}+\boldsymbol{Z}_{bc}+\boldsymbol{Z}_{ca}}\cdot\boldsymbol{I}_{byd}+\frac{-(\boldsymbol{V}_{sa}+\boldsymbol{V}_{sb}+\boldsymbol{V}_{sc})}{\boldsymbol{Z}_{ab}+\boldsymbol{Z}_{bc}+\boldsymbol{Z}_{ca}}\right]\right\}\end{aligned}\tag{2-29}$$

Equations (2-27)-(2-29) are the final calculation results of inverter commutation voltages during a phase-A fault. It can be seen that there are two parts in each expression – the first part is the voltage $\boldsymbol{E}_{as}$, $\boldsymbol{E}_{bs}$, or $\boldsymbol{E}_{cs}$, and their coefficients, while the second part is the rest of each expression of (2-27)-(2-29). The physical meaning of the first part is the voltage at the inverter bus caused by the voltage source $\boldsymbol{E}_{as}$, $\boldsymbol{E}_{bs}$, and $\boldsymbol{E}_{cs}$, and the second part indicates the voltage caused by converter currents that are flowing into the AC network.

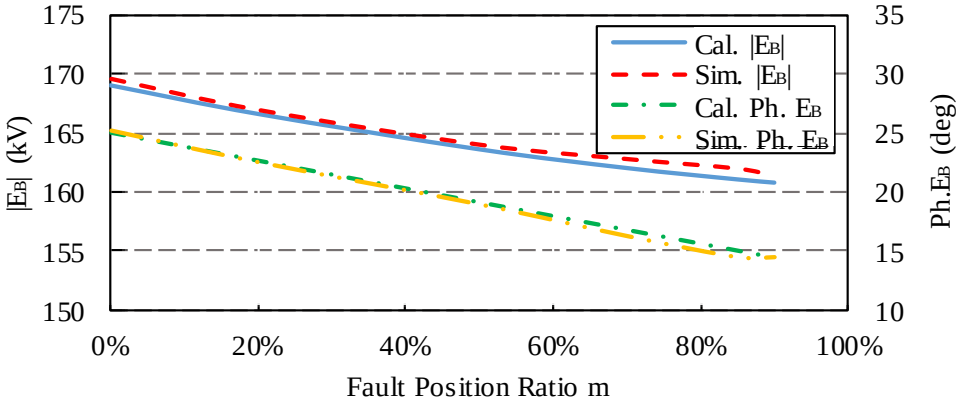
It can be seen from the expressions that the proposed method considers the fault location, fault impedance, and the impact of the YD transformer on the commutation voltages due to the loop currents $\boldsymbol{I}_{ab}$, $\boldsymbol{I}_{bc}$ and $\boldsymbol{I}_{ca}$, which are not considered in existing research.

2.2.4 Calculation Accuracy

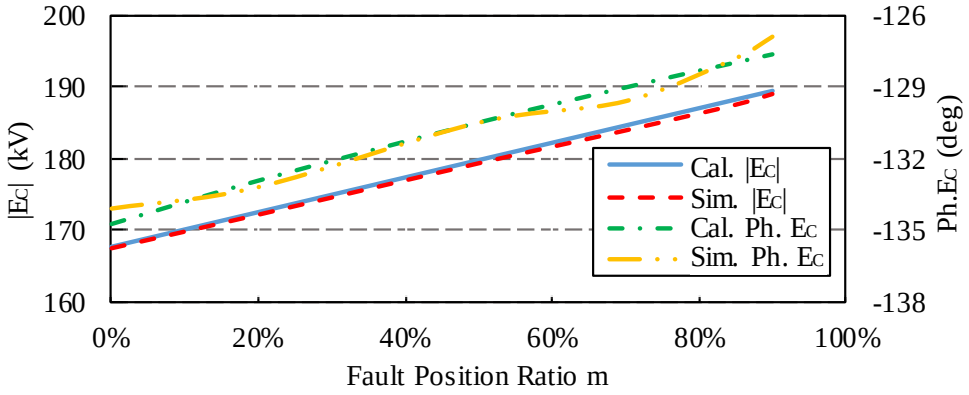
To verify the accuracy of the proposed method, the network shown in Figure 2-2 is modelled in RTDS and the simulation results are compared with the calculation results.



(a) Phase A commutation voltage comparison



(b) Phase B commutation voltage comparison



(c) Phase C commutation voltage comparison

Figure 2-5 The comparisons of the calculation and simulation results.

The comparisons of both voltage magnitudes and phase angles are presented in Figure 2-5. In

the comparisons, a phase-A SLG fault with the fault impedance of 2 ohms at different locations on the line are simulated. The fault location at 0%, 20%, 50%, 70%, 85%, and 90% of the transmission line is considered, by changing the value of m.

It can be seen from Figure 2-5 that the error between the proposed method and simulation results is less than 1%. It is important to point out that: 1) the magnitude and phase angle of the faulty and non-faulty phase voltages are changing under SLG faults; 2) the magnitude changes and phase shifts of the phase A and C increase when the fault is further away from the inverter bus, and they decrease for phase B. These are not revealed in existing research where only the magnitude change of the faulty phase is considered while the magnitude and phase angles of non-faulty phases remained unchanged. As will be shown in the next section, the more accurate calculation of commutation voltage will improve the accuracy of CF prediction.

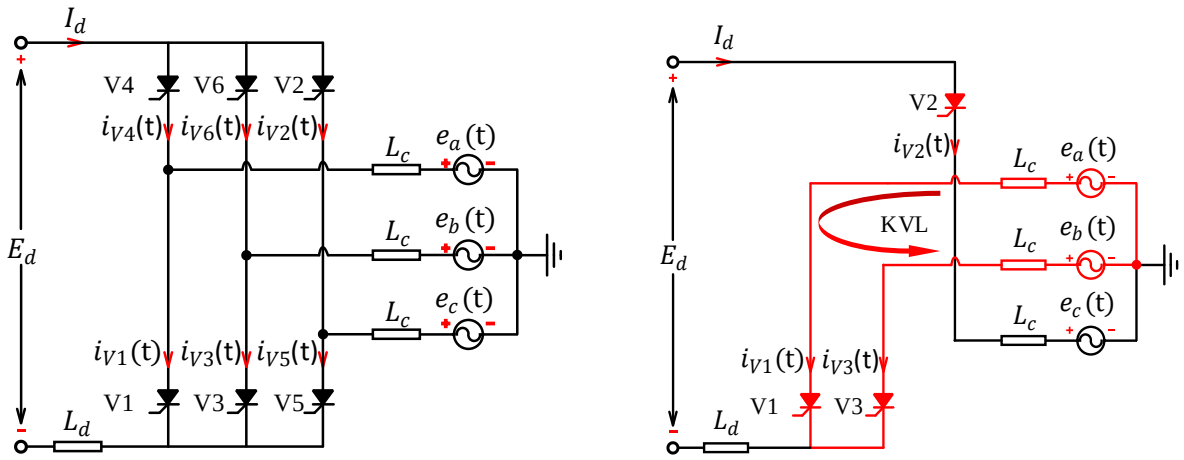
2.3 Commutation Failure Prediction

The voltage-time area (VTA) method can be utilised to estimate the possibility of CF. In this section, based on the VTA method, the calculation results from Section 2.2 are used to improve the accuracy of CF estimation.

2.3.1 Theoretical Basis of VTA Method

The theory of the VTA method [36][38][63] can be explained by analysing the commutation process from valve 1 (V1) to valve 3 (V3) of a 6-pulse inverter as shown in

Figure 2-6.



(a) The Graetz Bridge Model (b) The Circuit for Commutation Process from V1 to V3

Figure 2-6 The Commutation Process of a 6-pulse inverter

where E_d is the inverter side DC voltage; I_d is the inverter side DC current; L_d is the inverter side DC current smoothing reactance; V1, V2, V3, V4, V5, and V6 are the 6 valve groups of the 6-pulse inverter; $i_{V1}(t)$, $i_{V2}(t)$, $i_{V3}(t)$, $i_{V4}(t)$, $i_{V5}(t)$, and $i_{V6}(t)$ are the current flow through the valves of V1, V2, V3, V4, V5, and V6; L_c is the commutation reactance; $e_a(t)$, $e_b(t)$, and $e_c(t)$ are the A, B, and C phase commutation voltages in the Graetz Bridge Model.

Figure 2-6(a) presents the Graetz Bridge model of an ideal 6-pulse inverter. The commutation process from V1 to V3 is analysed. Applying KVL Law to the red loop in

Figure 2-6(b), the following equation can be obtained:

$$L_c \cdot \frac{di_{V1}(t)}{dt} - L_c \cdot \frac{di_{V3}(t)}{dt} - e_a(t) + e_b(t) = 0 \tag{2-30}$$

This can be written in the form of the line-to-line voltage:

$$L_c \cdot \frac{di_{V1}(t)}{dt} - L_c \cdot \frac{di_{V3}(t)}{dt} = e_a(t) - e_b(t) = e_{ab}(t) \tag{2-31}$$

where $e_{ab}(t)$ is the line-to-line commutation voltage.

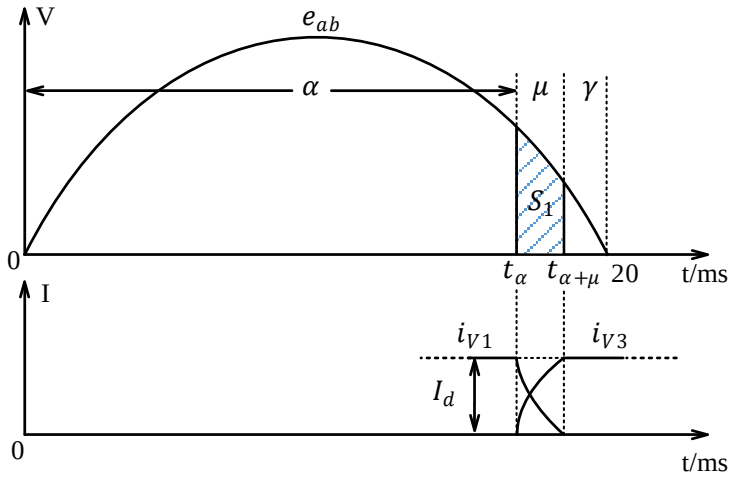


Figure 2-7 The commutation waveforms of $e_{ab}(t)$, $i_{V1}(t)$ and $i_{V3}(t)$.

By assuming the phase of the commutation voltage $e_{ab}(t)$ is zero, the commutation process from V1 to V3 is shown in Figure 2-7, where t_α is the time instant of the beginning of the commutation firing pulse; $t_{\alpha+\mu}$ is the time instant of the end of the commutation process; α is the firing angle; μ is the overlap angle; γ is the extinction angle.

It can be seen from Figure 2-7 that the commutation process starts from t_α to $t_{\alpha+\mu}$, with the duration of μ degrees. The extinction process starts from $t_{\alpha+\mu}$ to t=20 ms with the duration of γ degrees. During the commutation period, the valve current i_{V1} decreases from the DC current value to zero gradually and i_{V3} increases from zero to the DC current. Within the extinction process, the thyristor valve V1 becomes totally blocked before its commutation voltage becomes positive.

Then the values of $i_{V1}(t)$ and $i_{V3}(t)$ at t_α and $t_{\alpha+\mu}$ can be obtained:

$$i_{V1}(t) = \begin{cases} I_d, & t = t_\alpha \\ 0, & t = t_{\alpha+\mu} \end{cases} \tag{2-32}$$

$$i_{V3}(t) = \begin{cases} 0, & t = t_\alpha \\ I_d, & t = t_{\alpha+\mu} \end{cases} \tag{2-33}$$

$$i_{V1}(t) + i_{V3}(t) = I_d \tag{2-34}$$

Through integrating both sides of (2-31) from t_α to $t_{\alpha+\mu}$, it can be written as below:

$$\int_{t_\alpha}^{t_{\alpha+\mu}} \left(L_c \cdot \frac{di_{V1}(t)}{dt} - L_c \cdot \frac{di_{V3}(t)}{dt} \right) dt = \int_{t_\alpha}^{t_{\alpha+\mu}} e_{ab}(t) dt \tag{2-35}$$

By applying (2-34) to (2-35), the results can be obtained:

$$L_c \cdot \left(I_d|_{t=t_\alpha} + I_d|_{t=t_{\alpha+\mu}} \right) = \int_{t_\alpha}^{t_{\alpha+\mu}} e_{ab}(t) dt \tag{2-36}$$

Considering I_d will remain constant when the system is in the steady state, $I_d|_{t=t_\alpha}$ will be equal to $I_d|_{t=t_{\alpha+\mu}}$, and (2-36) can be expressed as below:

$$2 \cdot L_c \cdot I_d = \int_{t_\alpha}^{t_{\alpha+\mu}} e_{ab}(t) dt \tag{2-37}$$

The right-hand side of (2-37) is the shadowed area S_1 (in blue) as shown in Figure 2-7. This voltage-time area equals the integration of $e_{ab}(t)$ over time during the commutation duration, i.e., μ degrees. The value of the left side part indicates a certain amount of VTA S_{AC_req} that the inverter valves require to commutate.

Under faults with no CF risks, the VTA provided by the AC system S_{AC_prov} is equal to the VTA required by the inverter S_{AC_req}, which can be expressed as:

$$S_{AC\_prov} = S_{AC\_req} \tag{2-38}$$

However, with the constant overlap angle μ and commutation voltage $e_{ab}(t)$, the VTA provided by the AC system S_{AC_req} will decrease if γ is reduced. Thus, the minimum extinction angle γ_{min} can be used to calculate the minimum VTA $S_{\min\ \_req}$ which is required by the valve groups to maintain successful commutations. This means that the transient dynamic CFs will be forecasted once the minimum required VTA cannot be provided by the AC system.

Once the commutation voltages decrease sharply in fault cases and the VTA provided by the AC system S_{AC_prov} is smaller than the minimum VTA $S_{\min\ \_req}$ required for successful commutations, CFs will occur. This can be expressed in (2-39)

$$S_{AC\_prov} < S_{min\_req} \tag{2-39}$$

2.3.2 CF Prediction

In this section, the calculation results from Section 2.2 are utilised to improve the CF prediction.

The prediction criterion is shown below:

1). Firstly, the minimum VTA for a specific HVDC system S_{min_req} is calculated by (2-40) based on the minimum extinction angle γ_{min}:

$$S_{min\_req} = \int_{t_{\alpha_1}}^{t_{\alpha_1+\mu}} \boldsymbol{e}_{ab}\, dt \Big|_{\gamma=\gamma_{min}} \tag{2-40}$$

where α_1 is the firing angle when the distinction angle reaches the minimum value; μ is the overlap angle; γ is the extinction angle.

2). Then the VTA provided by the AC system S^f_{ACprov} for all commutation voltages is calculated during faults which means the transient dynamics are not considered, by utilizing the commutation voltages calculated in Section 2.2, as shown in Figure 2-8.

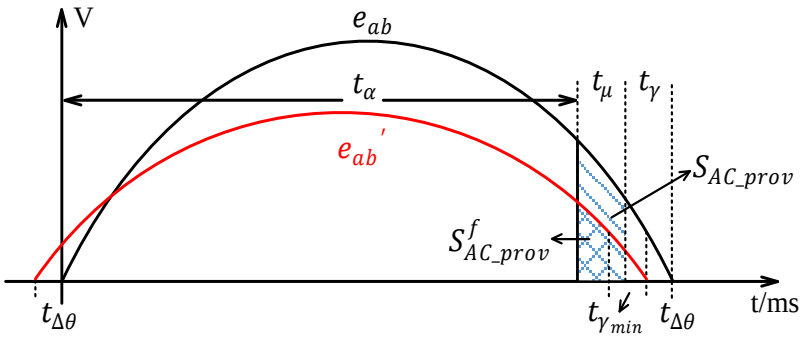


Figure 2-8 Commutation voltage $\boldsymbol{e}_{ab}(t)$ before and during SLG faults.

$$S^f_{ab\_ACprov} = \int_{t_\alpha}^{t_{\alpha+\mu-\Delta\theta^f_{ab}}} \boldsymbol{e}^f_{ab} dt \Big|_{\boldsymbol{e}^f_{ab}=\left|\boldsymbol{E}^f_{Abus}-\boldsymbol{E}^f_{Bbus}\right|} \tag{2-41}$$

$$S^f_{bc\_ACprov} = \int_{t_\alpha}^{t_{\alpha+\mu-\Delta\theta^f_{bc}}} \boldsymbol{e}^f_{bc} dt \Big|_{\boldsymbol{e}^f_{bc}=\left|\boldsymbol{E}^f_{Bbus}-\boldsymbol{E}^f_{Cbus}\right|} \tag{2-42}$$

$$S^f_{ca\_ACprov} = \int_{t_\alpha}^{t_{\alpha+\mu-\Delta\theta^f_{ca}}} \boldsymbol{e}^f_{ca} dt \Big|_{\boldsymbol{e}^f_{ca}=\left|\boldsymbol{E}^f_{Cbus}-\boldsymbol{E}^f_{Abus}\right|} \tag{2-43}$$

$$S^f_{AC\_prov} = min\left\{S^f_{ab\_ACprov}, S^f_{bc\_ACprov}, S^f_{ca\_ACprov}\right\} \tag{2-44}$$

where $\boldsymbol{e}_{ab}$, $\boldsymbol{e}_{bc}$, $\boldsymbol{e}_{ca}$, $\boldsymbol{e}^f_{ab}$, $\boldsymbol{e}^f_{bc}$,and $\boldsymbol{e}^f_{ca}$ are the line-to-line commutation voltages before and during faults. $\boldsymbol{E}^f_{Abus}$, $\boldsymbol{E}^f_{Bbus}$, $\boldsymbol{E}^f_{Cbus}$ are the equivalent commutation phase voltages during faults which can be calculated by (2-27)-(2-29); $\Delta\theta^f_{ab}$, $\Delta\theta^f_{bc}$, $\Delta\theta^f_{ca}$ are the phase shift angles of $\boldsymbol{e}^f_{ab}$ leading $\boldsymbol{e}_{ab}$, $\boldsymbol{e}^f_{bc}$ leading $\boldsymbol{e}_{bc}$, and $\boldsymbol{e}^f_{ca}$ leading $\boldsymbol{e}_{ca}$, respectively.

3). Compare S_{min_req} and $S^f_{AC\_prov}$ and then predict the occurrence of CFs:

If the $S_{AC\_prov}^{f}$ is less than S_{min_req}, CFs would occur; On the contrary, CFs would not.

It needs to be pointed out that in practical projects, FCF may still occur even if $S_{AC\_prov}^{f}$ is larger than S_{min_req} during faults as quasi steady-state equations are used for the calculations. However, the system will quickly recover to normal operation after FCF, causing limited impacts on the AC network. It is the SCF that may cause the blocking of converters and is therefore of concern in practical LCC-HVDC projects.

2.3.3 Extra Voltage for Commutation Voltages to Avoid CF

To further explore 'how close' the commutations are to being successful under SLG faults, the extra phase voltage ΔE_{extra} that is required to avoid CF can be calculated by following steps:

1) Calculate the critical commutation phase voltages $\boldsymbol{E}_{Abus}^{f.Cri}$, $\boldsymbol{E}_{Bbus}^{f.Cri}$, $\boldsymbol{E}_{Cbus}^{f.Cri}$

$$\boldsymbol{E}_{Abus}^{f.Cri} = (\left|\boldsymbol{E}_{Abus}^{f}\right| + \Delta E_{extra}\,)\angle \boldsymbol{E}_{Abus}^{f} \tag{2-45}$$

$$\boldsymbol{E}_{Bbus}^{f.Cri} = (\left|\boldsymbol{E}_{Bbus}^{f}\right| + \Delta E_{extra}\,)\angle \boldsymbol{E}_{Bbus}^{f} \tag{2-46}$$

$$\boldsymbol{E}_{Cbus}^{f.Cri} = (\left|\boldsymbol{E}_{Cbus}^{f}\right| + \Delta E_{extra}\,)\angle \boldsymbol{E}_{Cbus}^{f} \tag{2-47}$$

Then the critical equivalent VTAs during faults provided by the AC system are obtained:

$$S_{ab\_ACprov}^{f.Cri} = \int_{t_\alpha}^{t_{\alpha+\mu-\Delta\theta_{ab}^{f.Cri}}} \boldsymbol{e}_{ab}^{f.Cri} dt \Big|_{\boldsymbol{e}_{ab}^{f.Cri}=\left|\boldsymbol{E}_{Abus}^{f.Cri}-\boldsymbol{E}_{Bbus}^{f.Cri}\right|} \tag{2-48}$$

$$S_{bc\_ACprov}^{f.Cri} = \int_{t_\alpha}^{t_{\alpha+\mu-\Delta\theta_{bc}^{f.Cri}}} \boldsymbol{e}_{bc}^{f.Cri} dt \Big|_{\boldsymbol{e}_{bc}^{f.Cri}=\left|\boldsymbol{E}_{Bbus}^{f.Cri}-\boldsymbol{E}_{Cbus}^{f.Cri}\right|} \tag{2-49}$$

$$S_{ca\_ACprov}^{f.Cri} = \int_{t_\alpha}^{t_{\alpha+\mu-\Delta\theta_{ca}^{f.Cri}}} \boldsymbol{e}_{ca}^{f.Cri} dt \Big|_{\boldsymbol{e}_{ca}^{f.Cri} = \left|\boldsymbol{E}_{Cbus}^{f.Cri} - \boldsymbol{E}_{Abus}^{f.Cri}\right|} \tag{2-50}$$

2). The extra voltages $\Delta E_{extra,1}$, $\Delta E_{extra,2}$ and $\Delta E_{extra,3}$ can be calculated by comparing the critical equivalent VTA during faults provided by the AC system and the minimum VTA required for the inverters:

$$S_{ab\_ACprov}^{f.Cri}\Big|_{\Delta E_{extra} = \Delta E_{extra,1}} = S_{min\_req} \tag{2-51}$$

$$S_{bc\_ACprov}^{f.Cri}\Big|_{\Delta E_{extra} = \Delta E_{extra,2}} = S_{min\_req} \tag{2-52}$$

$$S_{ca\_ACprov}^{f.Cri}\Big|_{\Delta E_{extra} = \Delta E_{extra,3}} = S_{min\_req} \tag{2-53}$$

3). The final extra voltage ΔE_{extra} needed for the inverter bus to prevent CFs can be obtained:

$$\Delta E_{extra} = max\left\{\Delta E_{extra,1},\ \Delta E_{extra,2},\ \Delta E_{extra,3}\right\} \tag{2-54}$$

It can be seen from (2-54) that the extra commutation voltages needed to avoid CFs are different for each phase due to different magnitude changes and phase shifts of the three phases. The maximum value is used to qualify the risk of CFs.

2.4 Case study

To further validate the effectiveness of the proposed method in Section 2.2 and the CF prediction in Section 2.3, a 6M2A Multi-Infeed LCC-HVDC system modified from the 4M2A system [108] is modelled. The topology of the system is shown in Figure 2-9.

2.4.1 6M2A Model Description

It can be seen from Figure 2-9 that the 6M2A system consists of six generators and two areas connected by two LCC-HVDC transmission lines. Four generators (G1, G2, G5, G6) and one centralised load (L7) are located in Area 1 while two generators (G3, G4) and the two centralised loads (L9, L23) are located in Area 2. The capacity of two HVDC transmission lines is 1000MW and 800MW, respectively. A 30km transmission line (T3) connects the two receiving end buses (Bus 1 and Bus 2) of the HVDC systems. Parameters are from [108] and listed in Table 2-2.

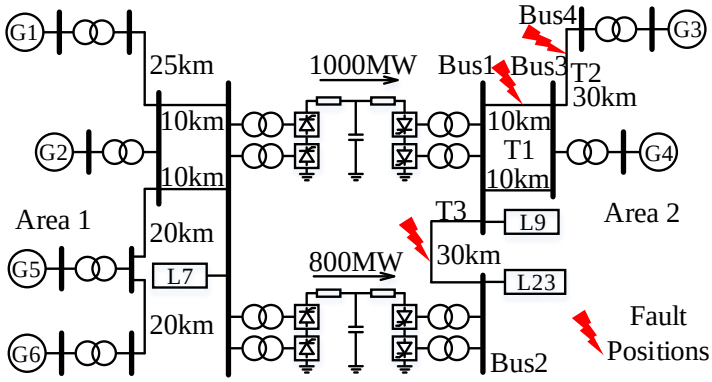


Figure 2-9 The topology of the 6M2A system.

Table 2-2 Parameters of 6M2A System

Parameters	Value
Rated AC Voltage at Area 1 & Area 2 (Line-to-Line, RMS)	230 kV
Voltage Ratings (Primary/Secondary) of the Transformers Connected with Synchronous Generators (Line-to-Line, RMS)	230 kV/20 kV
Leakage Reactance of the Transformers Connected with Synchronous Generators (with the Power Base of 100 MVA)	0.017 p.u.
Capacitors Connected to the Inverter Bus per Phase	33.06 uF
SLG Fault Impedance from Fault Point to Ground	1~160 ohm
Resistance of T1, T2 and T3 per Phase per km	0.028 ohm

Inductive Reactance of T1, T2, and T3 per Phase per km	0.2708 ohm
L7 - Load at Rectifier Side	860MW+100MVar
L9 - Load at Inverter 1 Side	2530MW+100MVar
L23 - Load at Inverter 2 Side	600MW+50MVar

2.4.2 Commutation Voltage Calculations

For this multi-infeed system, the calculation method explained in Section 2.2 is used to calculate the commutation voltages under phase A faults at different locations on the transmission lines. The three-line diagram of the 6M2A system is shown in Figure A-1 in Appendix, and the final expressions of the commutation voltages are shown below:

$$\boldsymbol{E}_{A1} = \boldsymbol{I}_{Aac1} \cdot \boldsymbol{Z}_{Aeq} + \boldsymbol{E}_{Aeq} \tag{2-55}$$

$$\boldsymbol{E}_{A2} = \left(\frac{N3}{N1} \cdot \boldsymbol{I}_{ab1} + \frac{N2}{N1} \cdot \boldsymbol{I}_{ayy1} + \frac{N5}{N1} \cdot \boldsymbol{I}_{ab2} + \frac{N4}{N1} \cdot \boldsymbol{I}_{ayy2} - \boldsymbol{I}_{Aac1} - \boldsymbol{I}_{Af3}\right) \cdot \boldsymbol{Z}_{C2} \tag{2-56}$$

$$\boldsymbol{E}_{B1} = \boldsymbol{I}_{Bac1} \cdot \boldsymbol{Z}_{Beq} + \boldsymbol{E}_{Beq} \tag{2-57}$$

$$\boldsymbol{E}_{B2} = \left(\frac{N3}{N1} \cdot \boldsymbol{I}_{bc1} + \frac{N2}{N1} \cdot \boldsymbol{I}_{byy1} + \frac{N5}{N1} \cdot \boldsymbol{I}_{bc2} + \frac{N4}{N1} \cdot \boldsymbol{I}_{byy2} - \boldsymbol{I}_{Bac1}\right) \cdot \boldsymbol{Z}_{C2} \tag{2-58}$$

$$\boldsymbol{E}_{C1} = \boldsymbol{I}_{Bac1} \cdot \boldsymbol{Z}_{Beq} + \boldsymbol{E}_{Beq} \tag{2-59}$$

$$\boldsymbol{E}_{C2} = \left(\frac{N3}{N1} \cdot \boldsymbol{I}_{ca1} + \frac{N2}{N1} \cdot \boldsymbol{I}_{cyy1} + \frac{N5}{N1} \cdot \boldsymbol{I}_{ca2} + \frac{N4}{N1} \cdot \boldsymbol{I}_{cyy2} - \boldsymbol{I}_{Cac1}\right) \cdot \boldsymbol{Z}_{C2} \tag{2-60}$$

where 1 and 2 stand for inverter 1 and inverter 2 of the 1000MW and 800MW HVDC systems, respectively; $\boldsymbol{E}_A$, $\boldsymbol{E}_B$, and $\boldsymbol{E}_C$, are the commutation voltages of each phase; $\boldsymbol{I}_{Aac1}$, $\boldsymbol{I}_{Bac1}$, $\boldsymbol{I}_{Cac1}$ are currents from inverter 1 to the AC system for phase A, B, and C, respectively; $\boldsymbol{Z}_{Aeq}$, $\boldsymbol{Z}_{Beq}$,

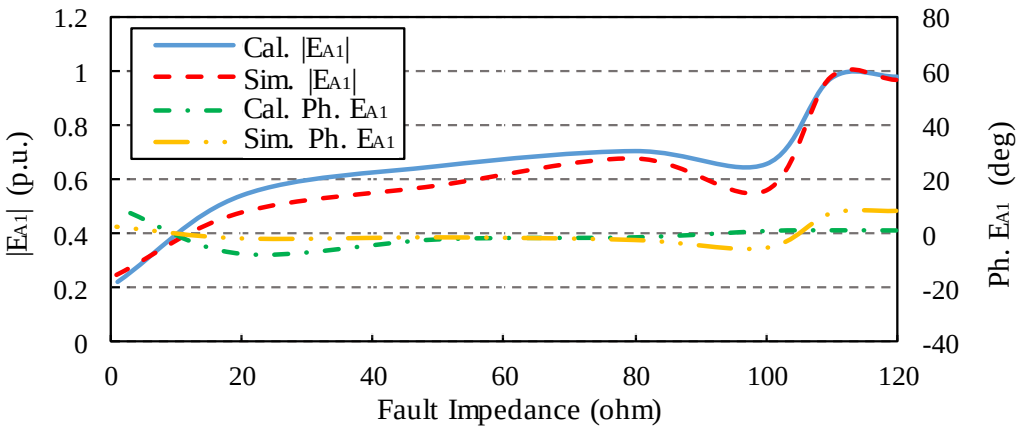
$\boldsymbol{Z}_{Ceq}$, $\boldsymbol{E}_{Aeq}$, $\boldsymbol{E}_{Beq}$, and $\boldsymbol{E}_{Ceq}$ are the impedance and voltages of phase A, B, and C of the AC system at the inverter 1 side, respectively; other variables have the same meaning as that in Figure 2-2 -Figure 2-4. Detailed equations are shown in (A1) - (A33) in Appendix.

It can be seen from the final expressions of the commutation voltages that they contain the variables of fault impedance, fault position, and all parameters of the inverter side of the system, which means that the impact of the YD transformers and the magnitude changes and phase shifts of all commutation voltages have been taken into account under SLG faults.

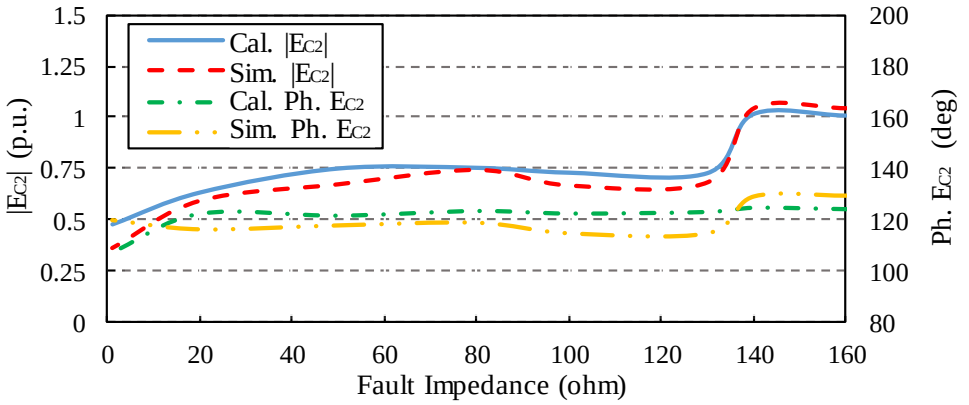
2.4.3 Simulation Validation of the Proposed Method

A phase-A SLG faults at different locations along transmission lines T1, T2, and T3 (as shown in Figure 2-9) is simulated in this chapter. The fault impedance varies from 1 ohm to 160 ohms for each fault point. Besides, to take the impact of Point on Wave (POW) into account, each fault case is simulated 12 times with different POWs spaced by 30 electrical degrees.

Figure 2-10 and Figure 2-11 show the comparison of results (voltage magnitude and phase angles) between the proposed method and simulation. For both figures, phase-A faults in the middle of transmission lines with varying fault impedance are considered.

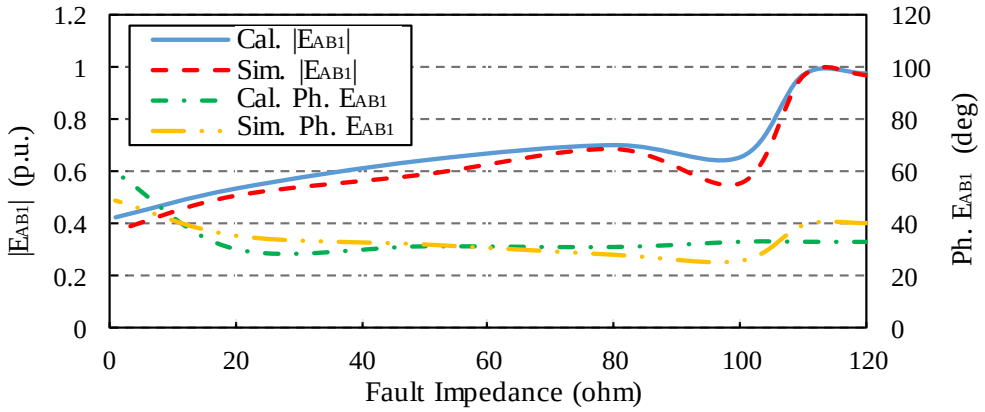


(a) Phase A Commutation Voltage for Inv 1 when phase A faults occur in the middle of T2

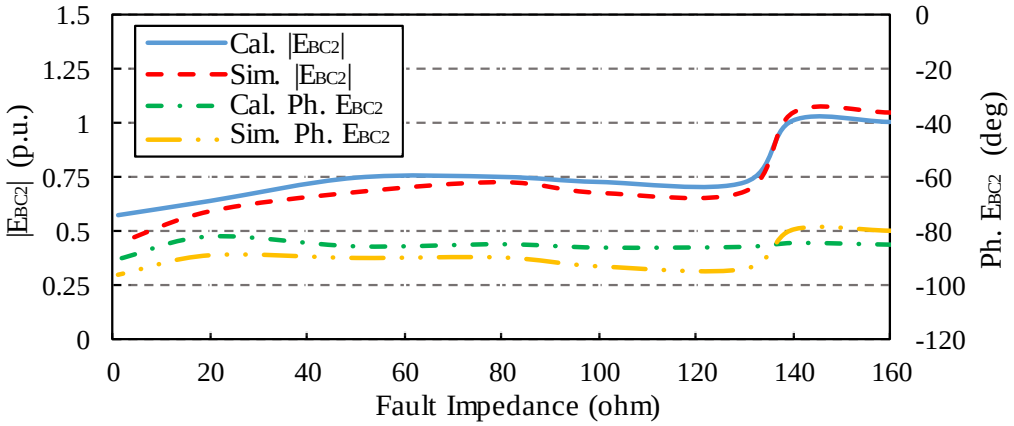


(b) Phase C Commutation Voltage for Inv 2 when phase A faults occur in the middle of T3

Figure 2-10 Comparison of proposed calculation and simulation results of the commutation voltages.



(a) L-L Commutation Voltage E_{AB1} for Inv 1 when phase A faults occur in the middle of T2



(b) L-L Commutation Voltage E_{BC2} of Inv 2 when Phase A faults occur in the middle of T3

Figure 2-11 Comparison of calculation and simulation results of the L-L commutation voltages.

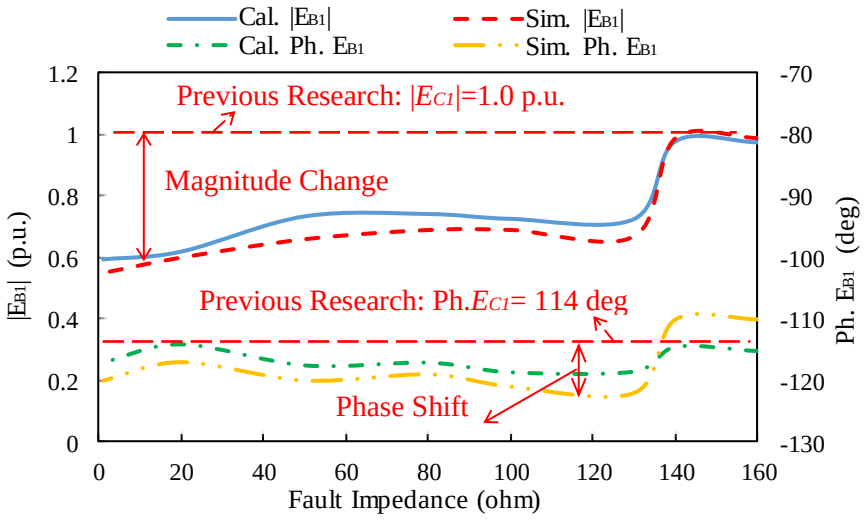
From Figure 2-10 and Figure 2-11, it can be seen that the average error between the proposed calculations and simulation results is smaller than 5%, which is mainly caused by the impact of the control system and the voltage harmonics under SLG faults. It is important to point out that when the fault position is fixed and fault impedance increases, the magnitudes of the faulty and non-faulty phase commutation voltages rise.

Since the phase angle of the commutation voltage E_{A1} and E_{C2} are 6° and 124° in the normal condition, it can be observed from Figure 2-10 and Figure 2-11 that both the phase angles of E_{A1} and E_{C2} drop (lag) once there is a SLG fault on phase A on T2 and T3. Similarly, the phase angles of E_{AB1} and E_{BC2} also drop (lag) under SLG faults. Their magnitude changes and phase shifts have a significant impact on the commutation process according to the VTA calculations in Section 2.3.

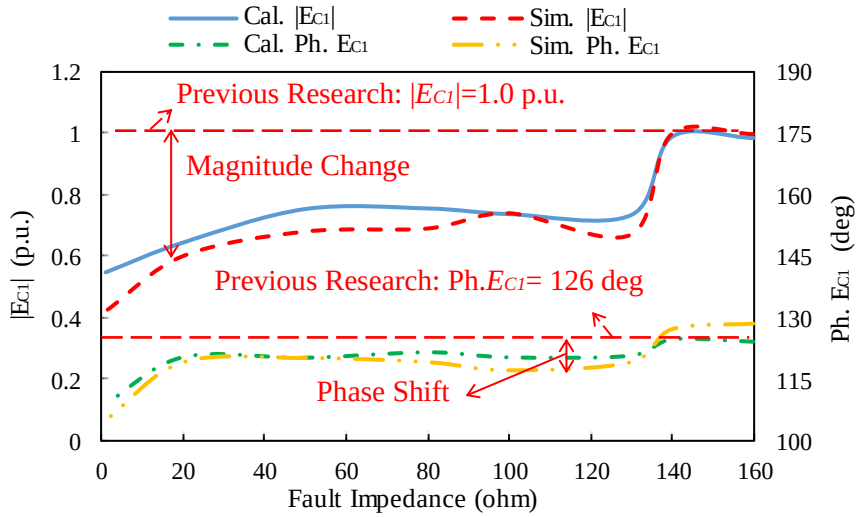
It needs to be pointed out that since all the parameters can be obtained in real projects, the proposed method can be utilised to carry out offline or online calculations to obtain commutation voltages under SLG faults. In online applications, the parameters that are used in (2-55) - (2-60) can be obtained from the measurement devices.

2.4.4 Magnitude Change and Phase Shift of Non-Faulty Phase Commutation Voltages

To quantify the impact of magnitude changes and phase shifts of the non-faulty phase voltages on commutation, comparisons between the proposed method and previous research (where changes in non-faulty phases are not considered as shown in Section 1.2.1) are presented in Figure 2-12 together with RTDS simulation results with varying fault impedance.



(a) Non-faulty Phase B Commutation Voltage



(b) Non-faulty Phase C Commutation Voltage

Figure 2-12 Magnitude and phase of commutation voltages when phase A faults occur in the middle of T3 with varying fault impedance.

The horizontal dotted lines in Figure 2-12 are the magnitude and phase of non-faulty phase commutation voltages which are assumed to be unchanged under SLG faults in previous research.

It can be seen from Figure 2-12 that when phase A faults occur in the middle of T3 with varying

fault impedance from 1 to 160 ohm, the magnitudes of Phase B&C commutation voltages of inverter 1 decrease by as large as 50% and 60%, respectively, and the phase angles lag by as large as 10 and 22 degrees, respectively. Such significant changes in magnitude and phase angle can on their own cause CFs (similar to moderate faults) and should be considered in predicting the CFs. For example, commutation voltages decreasing by 50% will directly cause CFs since CFs could happen under 10%-14% of voltage depression at inverter AC bus [24].

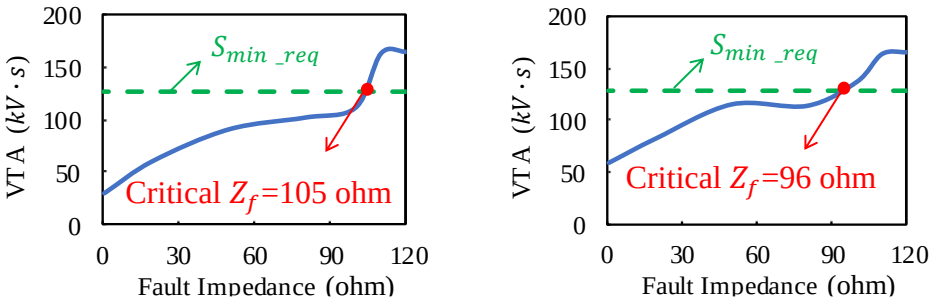
2.4.5 CF Prediction Based on the Proposed Method

The performance of the proposed method in predicting CF is demonstrated in this section.

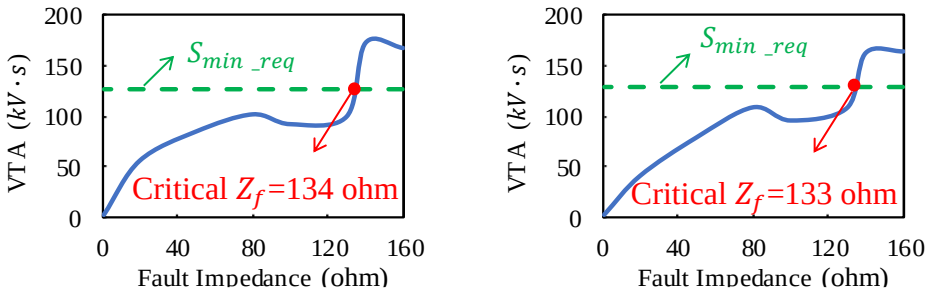
Firstly, with a minimum extinction angle of 7°, the minimum VTA S_{min_req} required for inverter 1 and inverter 2 are obtained as 127.41 kV·s and 128.44 kV·s, respectively, by applying (2-40).

The VTA $S^{f}_{AC\_prov}$ provided by the AC system under different fault cases can be then calculated through using (2-44). By comparing S_{min_req} and $S^{f}_{AC\_prov}$, CF can be predicted.

Figure 2-13 shows the calculation results for the VTA provided by the AC system under phase A faults occurring in the middle of T2 and T3 with different fault impedance. The dotted lines in Figure 2-13 are the minimum VTA S_{min_req} required for the inverters.



(a)VTA Provided to Inv.1 (Faults on T2). (b) VTA Provided to Inv.2 (Faults on T2)



(c)VTA Provided to Inv.1 (Faults on T3). (d) VTA Provided to Inv.2 (Faults on T3)

Figure 2-13 Proposed calculation results - S_{ACprov}^{f} provided by the AC system to Inv 1 and Inv 2 when phase A SLG faults occur in the middle of T2 and T3.

The crossing points indicate the critical fault impedance calculated by the proposed method. It means that when a SLG fault occurs with a fault impedance lower than the critical value, CFs will occur.

It can be seen from Figure 2-13 that the VTA provided by the AC system is far smaller than the minimum VTA required by the inverters when the fault impedance decreases to near zero, which means the commutation process cannot be completed. As the fault impedance approaches around 100-130 ohm, the VTA provided by the AC system is comparable to the minimum required VTA for successful commutation.

To verify the accuracy of the proposed calculation results shown in Figure 2-13, EMT simulations have been carried out to obtain the critical fault impedance as shown in Table 2-3. For each value of fault impedance, 50 times of simulations under the SLG fault with different POW are performed to obtain the critical fault impedance. Comparisons in Table 2-3 are made with existing research where magnitude changes and phase shifts of non-faulty phase voltages are ignored. The results are under the assumptions that the impact of the control system and the voltage harmonics are not considered in the proposed method, and parameters of three phases of each part of the system is assumed symmetrical for all comparisons. It can be clearly

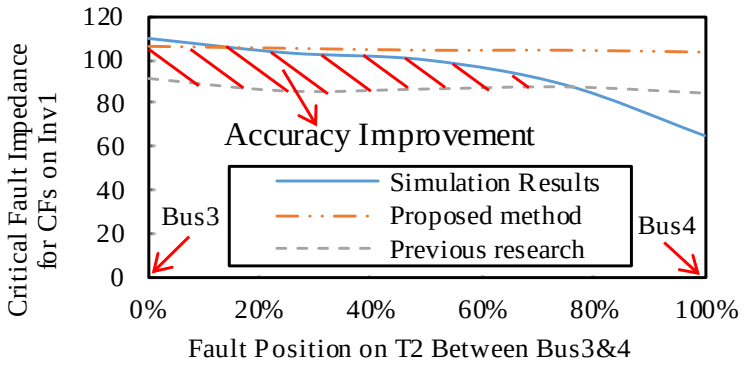
seen from Table 2-3 that the proposed method can accurately calculate the critical fault impedance for SLG fault compared with previous research, since the error of the prediction results by the proposed method is less than 3% while the error of previous research ranges from 14% to 65%. Thus, the proposed method can reduce the CF prediction error by 14% to 62% compared with previous approaches that only consider the magnitude change of the faulty-phase commutation voltage.

Table 2-3 Comparison of calculation and simulation results for critical SLG fault impedance

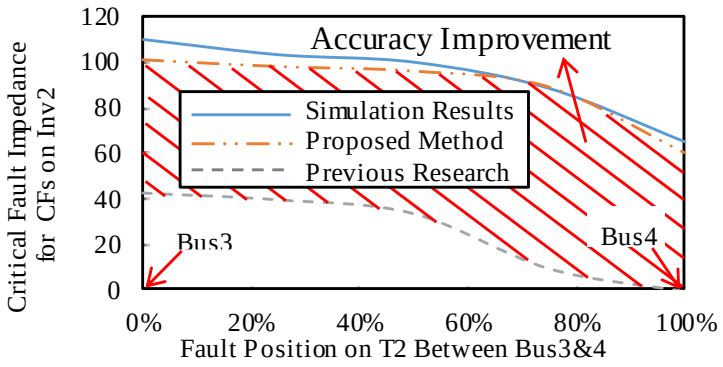
Critical Fault Impedance (Ω)	Calculation Results	Simulation Results	Previous Research
On T2 For Inv. 1	100	100	86
On T2 For Inv. 2	97	100	35
On T3 For Inv. 1	134	135	105
On T3 For Inv. 2	133	135	83

Using the proposed method, the critical SLG fault impedance for Inv1 and Inv2 along T2 and T3 can be calculated, as shown in the form of the dash-double-dot lines in Figure 2-14, where they are compared with the previous research and simulation results. The area between the horizontal axis and each curve is the corresponding CF risk area. The shadowed areas between the previous research curves and the proposed method curves in Figure 2-14 indicate the accuracy improvement of the proposed method. For example, once a SLG fault occurs within the accuracy improvement areas in Figure 2-14, previous research will predict that this fault does not cause CF, while in fact, it does. As mentioned before, such inaccurate prediction is caused by neglecting the magnitude changes and the phase shifts of the non-faulty phase voltages.

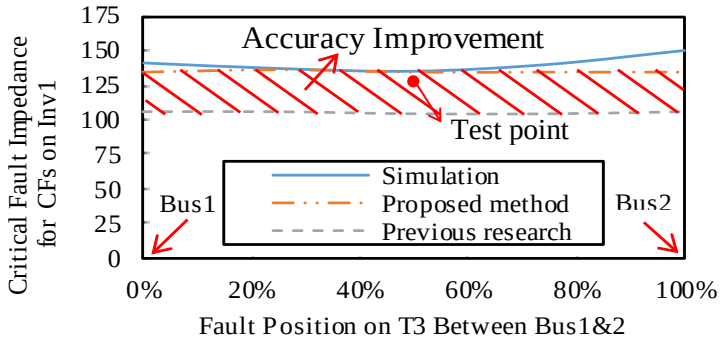
In addition, from the comparisons in Figure 2-14(b) - (d), the errors between the proposed calculation results and simulation results are less than 5%. In Figure 2-14 (a), the error becomes larger when faults are closer to Bus 4. This again shows that the CF prediction using the proposed method is more accurate than previous methods.



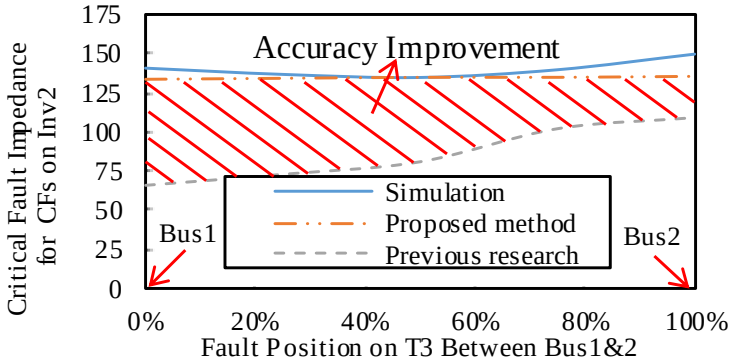
(a) Accuracy Improvement for Critical Fault Impedance for CFs for Inv. 1 when SLG Faults Occur on T2



(b) Accuracy Improvement for Critical Fault Impedance for CFs for Inv. 1 when SLG Faults Occur on T2



(c) Accuracy Improvement for Critical Fault Impedance for CFs for Inv. 1 when SLG Faults Occur on T3



(d) Accuracy Improvement for Critical Fault Impedance for CFs for Inv. 1 when SLG Faults Occur on T3

Figure 2-14 Accuracy improvement by comparing the critical fault impedance by the proposed method, previous research and simulation results.

It also can be seen that the critical fault impedance obtained from the proposed method and that from the simulation results are higher than that in previous research that did not consider the magnitude changes and phase shifts of the non-faulty phase voltages. This reveals that the proposed method is more conservative than previous research, which is certainly favourable for practical applications.

To verify the results from Figure 2-14, time-domain simulation results using RTDS are presented in Figure 2-15 where the fault condition corresponds to the 'Test point' in Figure 2-14 (c) is simulated. It clearly validates that faults within the accuracy improvement area will cause CFs. It needs to be pointed out that the magnitudes and phase angles of the commutation voltages keep changing during the fault and recovery process, and thus SCFs occur as shown in Figure 2-15. The reason is that the 6M2A system is dominated by synchronous generators without ideal voltage sources. Therefore, the recovery of the system voltage will be slower than that with ideal voltage sources, which consequently causes SCFs. In contrast, for those systems with voltage sources that have been used by existing research, i.e., the CIGRE LCC-HVDC Benchmark system, SCFs will not occur as it takes less time for the system voltage to recover

to the nominal value.

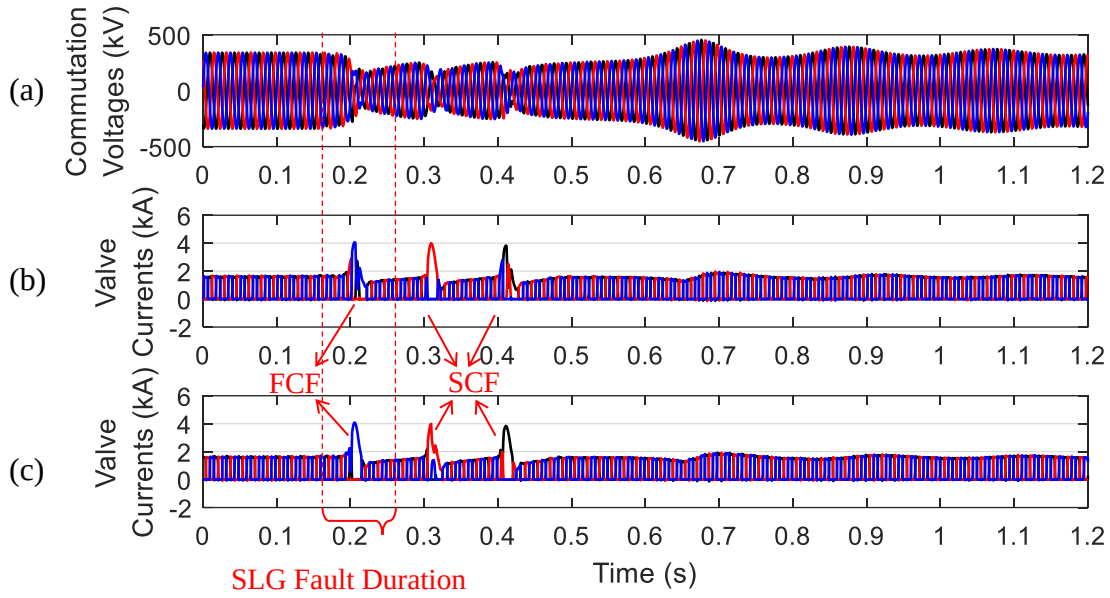


Figure 2-15 Commutation process of Inv 2 when SLG fault occurs on T3. (a) Three phase commutation voltages waveforms. (b) Three phase valve currents in the upper arms. (c) Three phase valve currents in the lower arms.

It is important to conclude from the results that for multi-infeed HVDC systems, the inverters located in different areas have varying requirements for successful commutations, based on the topologies of the systems, the fault location, and the fault impedance. The proposed calculation method can accurately calculate the critical fault impedance value under SLG faults for multi-infeed HVDC systems considering the magnitude changes and the phase shifts of the non-faulty phase voltages. This is practically beneficial for system operators to develop a clearer understanding of CF risks for multi-infeed systems.

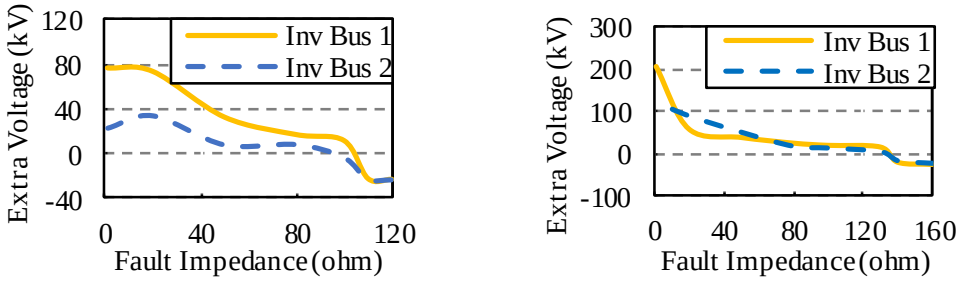
2.4.6 Error Analysis

The error between the proposed method and the simulation results in Figure 2-14 is mainly caused by the impact of the control system and the voltage harmonics under SLG faults (see Figure 1-4). These aspects can be considered but may lead to significant complexity in the calculation process. As the error between the proposed method and simulation results is small,

i.e., less than 5% as shown in Figure 2-14 for most cases, the above aspects are not considered in the proposed method. Furthermore, such error normally causes inaccurate prediction of FCF (rather than SCF) which is self-recoverable and has less impact on the AC network.

2.4.7 Extra Voltage to Prevent Subsequent CFs

Based on (2-45) - (2-54), the extra voltage to avoid CFs can be calculated, as shown in Figure 2-16. The values indicate the minimum extra commutation voltages that are needed for successful commutations. For example, as shown in Figure 2-16 (a), when a phase-A fault occurs in the middle of T2 with 40 ohms of fault impedance, CFs happen in both inverters, and Inv Bus 1 and Inv Bus 2 need 10kV and 43kV of extra commutation voltages, respectively, to avoid CFs. On the contrary, when a phase-A fault occurs in the middle of T3 with 140 ohms of fault impedance (Figure 2-16 (b)), there are no CFs, but CFs would occur if the two inverter bus voltages further decrease by 25kV. Such a method of quantifying the risk of CF provides a more accurate way for system operators to understand the severity of CF under unbalanced faults.



(a) Faults occur on T2

(b) Faults occur on T3

Figure 2-16 Extra voltage to avoid CFs for two inverters when SLG faults occur in the middle of T2 and T3.

It can be concluded from Figure 2-16 that 1) Lower fault impedance causes larger extra commutation voltages required for maintaining successful commutations for both inverters; 2) Faults cause larger extra commutation voltages required by the nearest inverter than the ones

far away from the fault locations for successful commutations; 3) Faults that occur on the transmission lines connecting the two inverters result in little difference in the extra commutation voltages required by the two inverters on both sides of the transmission line for successful commutations.

The extra voltage value can be used to: 1) Quantify how "close" the commutations are to being successful or failing; 2) Quantify the voltage ratings of the additional devices (e.g., controllable capacitors) which provide extra commutation voltages to achieve CF elimination goal. It can help the system operator design LCC-HVDC projects and upgrade ones.

2.5 Summary

This chapter proposes an extended method of calculating commutation voltages under SLG faults that can be used to significantly improve the accuracy of CF prediction (CF prediction is also available under other types of asymmetrical faults by changing the fault circuit part as shown in Figure A-1 in red to the corresponding circuit). This is achieved by calculating the changes of not only the magnitudes but also the phase angles of all three phase commutation voltages, which is vital for the success of commutations but not comprehensively considered by previous research. The accuracy of the proposed methods in this chapter is verified by simulations based on RTDS. The proposed mathematical CF prediction method makes can be applied to predict CFs for large-scale and complex power systems with LCC-HVDC systems which cannot be simulated on RTDS due to the limitations of computing capability of the processors. Thus, the proposed mathematical CF prediction method can help the system operators design new LCC-HVDC projects and upgrade existing ones.

With the abovementioned benefits, the proposed method is utilised to calculate the extra

commutation voltages needed to avoid CFs. This provides a new pathway in quantifying the how ‘close’ the commutations are to being successful or unsuccessful, which is not analysed by previous research. Also, it can provide the voltage ratings of the additional devices (e.g., controllable capacitors) to achieve CF elimination goal and thus help the system operator design LCC-HVDC projects and upgrading ones. It needs to be noticed that the extra voltage indicates voltage magnitude, and consequently the output voltage of the additional devices needs to be maintained synchronous with the commutation voltage at the inverter bus.

CHAPTER 3 An Improved Commutation Voltage Calculation Method Based on Symmetrical Components Theory

3.1 Introduction

As mentioned in Section 1.2.1, the SC method has not been applied in calculating unbalanced variables of the LCC-HVDC system under asymmetrical faults. Since the SC method is for analysing asymmetrical faults by considering symmetrical components of all power system devices in positive, negative, and zero sequences which could reflect the unbalanced parts of all variables, e.g., the loop current in the secondary side of the YD transformer, the calculation results of all power system variables under unbalanced faults by other methods will be less accurate if the SC method is not applied. To solve the above problems and illustrate the fact that the magnitudes and phase angles of all three phase commutation voltages will change and become unbalanced under asymmetrical faults, this chapter studies the sequence network diagram of the 12-pulse LCC-HVDC inverter side including a transmission line using SC method. To predict CFs, the magnitudes and phase angles of both faulty phase and non-faulty phase commutation voltages of the LCC-HVDC under the SLG fault are calculated based on the SC method. In the end, the accuracy of the calculation results is verified by comparing the calculation results with the simulation results through RTDS as well as the calculation results based on the method in Chapter 2.

This structure of this chapter is organised as below: Section 3.2 explains the theory of the SC method, and Section 3.3 derives the sequence network diagram of the inverter side of the LCC-

HVDC including a transmission line under asymmetrical faults, and then presents the expressions for the commutation voltages and fault current. Section 3.3 verifies the accuracy of the SC method through simulation demonstrations on RTDS and the comparison with the method proposed in Chapter 2.

3.2 Theory of the Symmetrical Components Method

The concept of the SC was first developed in [109] to resolve an unbalanced system into several systems with balanced phasors which are named "symmetrical components" of the original system phasors. The benefit of the SC method is its feasibility and convenience in solving unbalanced problems, such as asymmetrical faults in power grids. By decoupling the three phases of the power system by converting it to three independent sequence networks (positive, negative and zero sequences). Then the unbalanced parameters can be obtained by adding their own three sequence components together.

For instance, for the three-phase commutation voltages, their positive sequence components have the same magnitude and have the same phase angle shift between them (e.g., Phase A is leading phase B by 120 deg and leading phase C by 240 deg, as shown in the positive-sequence phasor diagram in Figure A-2 (a) in Appendix). Negative components have the same magnitude, but their phase angle shifts are inverse (e.g., phase A is lagging phase B by 120 deg and lagging phase C by 240 deg, as shown in the negative-sequence phasor diagram in Figure A-2 (b) in Appendix). Their zero sequence components have the same magnitude and the same phase angle, as shown in the zero-sequence phasor diagram in Figure A-2 (c) in Appendix. Under the normal operation condition, only the positive sequence components exist since the system is symmetrical. However, under unbalanced faults, the commutation voltages are asymmetrical,

and the positive sequence components plus the negative and zero sequence components can describe the unbalanced voltages. As a result, the asymmetrical problem is converted to a set of symmetrical problems which can be more easily solved.

In general, the steps of applying the SC method are as follows:

(1) Plot the three sequence diagrams according to the symmetrical components of each device based on the circuit diagram of the system;

(2) Derive the Thevenin Equivalent circuit for each sequence diagram from the point where the asymmetrical faults occur to the ground;

(3) Figure out the boundary conditions (fault currents and fault point voltages for all three phases) for the three-phase quantities at the fault point based on the fault type and then transform them into equations with sequence quantities;

(4) Based on the sequence equations derived from the boundary conditions in (3), connect the three sequence Thevenin Equivalent circuits properly with the fault impedance;

(5) Solve the integrated circuit to calculate sequence quantities and then transform them back to the phase quantities.

The above steps will be illustrated in detail in the following sections.

3.3 The Sequence Network Diagram of the LCC-HVDC Inverter Side

Based on the above explanation, the SC method can be utilised to analyse the asymmetrical issues in the power grids and derive all variables under asymmetrical faults. In this section, the modified 12-pulse CIGRE LCC-HVDC Benchmark system is analysed, and its sequence

network diagram of the inverter side is derived.

3.3.1 The Three-Line Diagram of the Inverter Side

To obtain the sequence network diagram of the inverter side of the 12-pulse LCC-HVDC system, the three-line diagram needs to be firstly derived.

The valve groups in inverters at the DC side of the transformers are represented by the current sources [34][51] to simplify the analysis which means the current sources will have negative and zero sequence components, and the impact control system and the voltage harmonics are not considered, the same as that in Chapter 2. Different with Figure 2-2, the transmission line with distributed parameters is replaced by a two-PI model for calculation simplifications. All the other parameters are corresponding to the detailed CIGRE LCC-HVDC Benchmark system [107] and Table 2-1. The three-line diagram of the inverter side of this 12-pulse LCC-HVDC system is presented in Figure 3-1, under a phase-A SLG fault occurring on the transmission line.

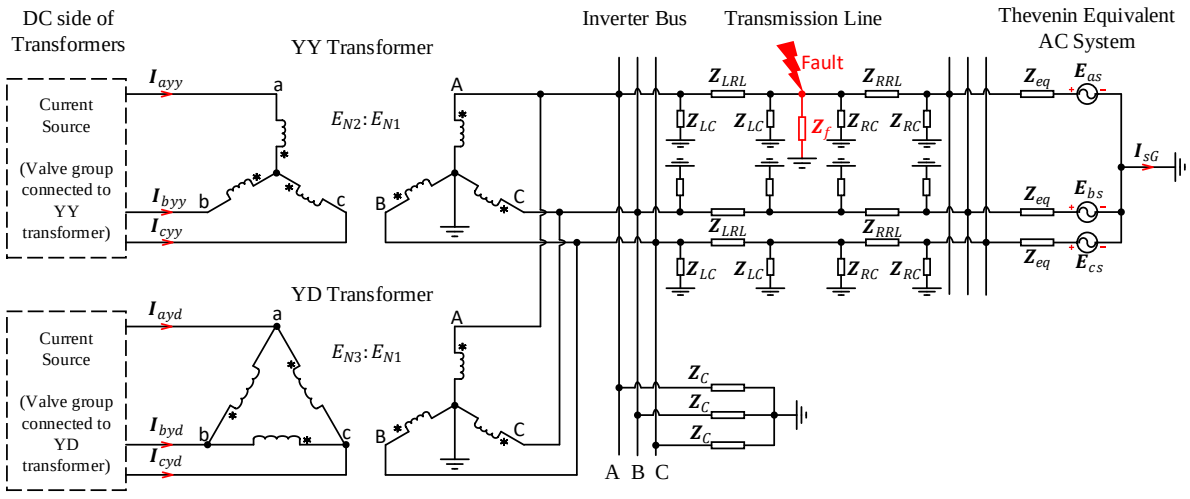


Figure 3-1 The three-line diagram of the 12-pulse LCC-HVDC inverter side

where $E_{N2}:E_{N1}$ and $E_{N3}:E_{N1}$ are the rated line-to-line voltage ratio of the secondary side to the primary side of the YY and YD transformer, respectively; $\boldsymbol{I}_{ayy}$, $\boldsymbol{I}_{byy}$, and $\boldsymbol{I}_{cyy}$, are the currents

from the phase A, B, and C ports of the current source connected with the YY transformer to the neutral point of the YY transformer secondary side, respectively; $\boldsymbol{I}_{ayd}$, $\boldsymbol{I}_{byd}$, and $\boldsymbol{I}_{cyd}$, are the currents from the phase A, B, and C ports of the current source connected with the YD transformer to the A, B, and C ports of the YD transformer secondary side, respectively; $\boldsymbol{Z}_{LRL}$ and $\boldsymbol{Z}_{LC}$ are the resistant and inductive reactance and the capacitive reactance of the PI model of the left part of the transmission line (between the fault point and the inverter bus), respectively; $\boldsymbol{Z}_{RRL}$ and $\boldsymbol{Z}_{RC}$ are the resistant and inductive reactance and the capacitive reactance of the PI model of the right part of the transmission line (between the fault point and the Thevenin Equivalent AC system), respectively; $\boldsymbol{Z}_{C}$ represents the equivalent capacitive reactance of the reactive power compensators and filters connected to the inverter bus per phase; $\boldsymbol{Z}_{Af}$ is the fault impedance from the fault point to the ground; $\boldsymbol{Z}_{eq}$ indicates the Thevenin Equivalent impedance per phase; $\boldsymbol{E}_{as}$, $\boldsymbol{E}_{bs}$, and $\boldsymbol{E}_{cs}$ are the Thevenin Equivalent voltages for phase A, B, and C, respectively; the Phase-B transmission line has the same parameters as phase C.

3.3.2 The Sequence Network Diagram of the Inverter Side

Based on the SC theory, the positive, negative, and zero sequence diagrams of the above system are studied as below:

1) Positive Sequence:

Since the positive components of the three-phase quantities are symmetrical, the primary side currents of the YY and YD transformers could be represented by $\frac{E_{N2}}{E_{N1}} \cdot \boldsymbol{I}_{ayy}^{+}$ and $\frac{E_{N3}}{E_{N1}} \cdot \boldsymbol{I}_{ayd}^{+} \cdot 1\angle 30°$, based on the transformation principles of the YY and YD transformers.

Thus, the positive sequence diagram of the inverter side of the 12-pulse LCC-HVDC system

can be drawn as shown in Figure 3-2.

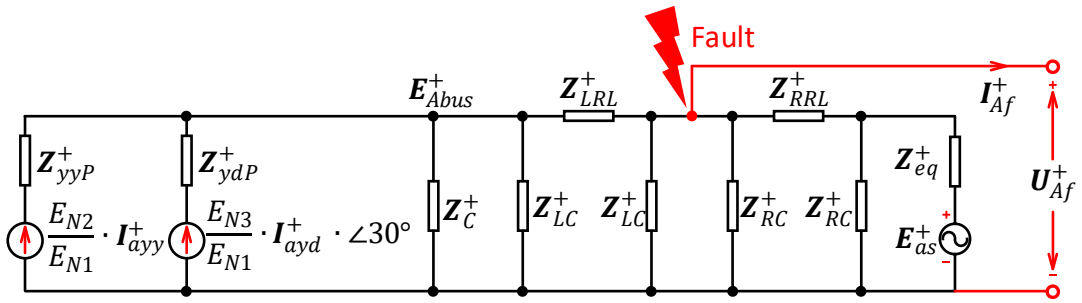


Figure 3-2 The Positive Sequence Diagram of the system

where $\boldsymbol{Z}^+_{yyP}$ is the positive sequence component of the primary side equivalent leakage impedance of the YY transformer; $\boldsymbol{Z}^+_{ydP}$ is the positive sequence component of the primary side equivalent leakage impedance of the YD transformer; $\boldsymbol{E}^+_{Abus}$ is the positive sequence component of the phase A potential of inverter bus; $\boldsymbol{U}^+_{Af}$ is the positive sequence component of the fault point potential $\boldsymbol{U}_{Af}$; $\boldsymbol{I}^+_{Af}$ is the positive sequence component of the fault point current to the ground $\boldsymbol{I}_{Af}$; $\boldsymbol{I}^+_{ayy}$, $\boldsymbol{I}^+_{ayd}$, $\boldsymbol{Z}^+_{LRL}$, $\boldsymbol{Z}^+_{LC}$, $\boldsymbol{Z}^+_C$, $\boldsymbol{Z}^+_{RRL}$, $\boldsymbol{Z}^+_{RC}$, $\boldsymbol{Z}^+_{eq}$, and $\boldsymbol{E}^+_{as}$ are the positive sequence components of $\boldsymbol{I}_{ayy}$, $\boldsymbol{I}_{ayd}$, $\boldsymbol{Z}_{LRL}$, $\boldsymbol{Z}_{LC}$, $\boldsymbol{Z}_C$, $\boldsymbol{Z}_{RRL}$, $\boldsymbol{Z}_{RC}$, $\boldsymbol{Z}_{eq}$, and $\boldsymbol{E}_{as}$, respectively.

It needs to be noticed from Figure 3-2 that the fault point is on the transmission line, and thus the positive sequence component of the fault voltage $\boldsymbol{U}^+_{Af}$ can be regarded as the voltage from the fault point to the ground point as shown in Figure 3-2 when looking into the whole system from these two points.

Then the Thevenin Equivalent circuit of the positive sequence diagram can be represented as shown in Figure 3-3.

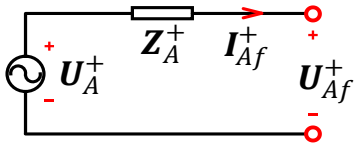


Figure 3-3 Thevenin Equivalent circuit of the Positive Sequence Diagram looking into the fault point

From Figure 3-2, the variables in Figure 3-3 can be derived as follows:

$$\boldsymbol{Z_A^+} = (\boldsymbol{Z_C^+}//\boldsymbol{Z_{LC}^+} + \boldsymbol{Z_{LRL}^+})//\boldsymbol{Z_{LC}^+}//\boldsymbol{Z_{RC}^+}//(\boldsymbol{Z_{RC}^+}//\boldsymbol{Z_{eq}^+} + \boldsymbol{Z_{RRL}^+}) \tag{3-1}$$

$$\begin{aligned}\boldsymbol{U_A^+} = \left[\left(\frac{E_{N2}}{E_{N1}} \cdot \boldsymbol{I_{ayy}^+} + \frac{E_{N3}}{E_{N1}} \cdot \boldsymbol{I_{ayd}^+} \cdot 1\angle 30°\right) \cdot \frac{\boldsymbol{Z_C^+}//\boldsymbol{Z_{LC}^+}}{\boldsymbol{Z_C^+}//\boldsymbol{Z_{LC}^+} + \boldsymbol{Z_{LRL}^+}} + \frac{\boldsymbol{E_{as}^+}}{\boldsymbol{Z_{eq}^+}}\right. \\ \left. \cdot \frac{\boldsymbol{Z_{RC}^+}//\boldsymbol{Z_{eq}^+}}{\boldsymbol{Z_{RC}^+}//\boldsymbol{Z_{eq}^+} + \boldsymbol{Z_{RRL}^+}}\right] \\ \cdot \left[(\boldsymbol{Z_C^+}//\boldsymbol{Z_{LC}^+} + \boldsymbol{Z_{LRL}^+})//\boldsymbol{Z_{LC}^+}//\boldsymbol{Z_{RC}^+}//(\boldsymbol{Z_{RC}^+}//\boldsymbol{Z_{eq}^+} + \boldsymbol{Z_{RRL}^+})\right]\end{aligned} \tag{3-2}$$

Besides, the expressions of the positive sequence component of the fault point phase-A voltage $\boldsymbol{U_{Af}^+}$ and that of the phase-A commutation bus voltage $\boldsymbol{E_{Abus}^+}$ can be derived as below:

$$\boldsymbol{U_{Af}^+} = \boldsymbol{U_A^+} - \boldsymbol{I_{Af}^+} \cdot \boldsymbol{Z_A^+} \tag{3-3}$$

$$\begin{aligned}\boldsymbol{E_{Abus}^+} = \boldsymbol{U_{Af}^+} + \left[\left(\frac{E_{N2}}{E_{N1}} \cdot \boldsymbol{I_{ayy}^+} + \frac{E_{N3}}{E_{N1}} \cdot \boldsymbol{I_{ayd}^+} \cdot 1\angle 30°\right) \cdot (\boldsymbol{Z_C^+}//\boldsymbol{Z_{LC}^+}) - \boldsymbol{U_{Af}^+}\right] \\ \cdot \frac{\boldsymbol{Z_{LRL}^+}}{\boldsymbol{Z_C^+}//\boldsymbol{Z_{LC}^+} + \boldsymbol{Z_{LRL}^+}} \\ = \left(\frac{E_{N2}}{E_{N1}} \cdot \boldsymbol{I_{ayy}^+} + \frac{E_{N3}}{E_{N1}} \cdot \boldsymbol{I_{ayd}^+} \cdot 1\angle 30° + \frac{\boldsymbol{U_{Af}^+}}{\boldsymbol{Z_{LRL}^+}}\right) \cdot (\boldsymbol{Z_C^+}//\boldsymbol{Z_{LC}^+}//\boldsymbol{Z_{LRL}^+})\end{aligned} \tag{3-4}$$

2) Negative Sequence:

Similarly, the negative sequence components of all devices are as same as their positive ones.

The only difference is that the voltage source in the Thevenin Equivalent AC system only contains the positive component. Then the negative sequence diagram can be plotted as shown in Figure 3-4:

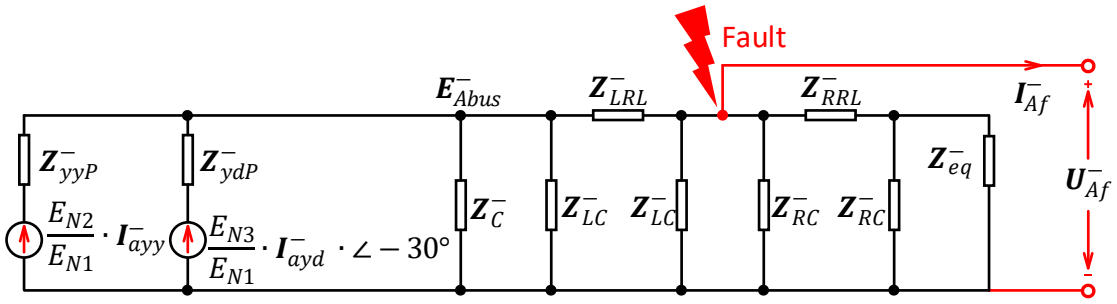


Figure 3-4 The negative sequence diagram of the system

where $\dot{Z}^-_{yyP}$ and $\dot{Z}^-_{ydP}$ are the negative sequence components of the primary side equivalent leakage impedance of the YY and YD transformers, respectively; $\dot{E}^-_{Abus}$ is the negative sequence component of the phase A potential of inverter bus; $\dot{U}^-_{Af}$ is the negative sequence component of the fault point potential $\dot{U}_{Af}$; $\dot{I}^-_{Af}$ is the negative sequence component of the fault point current to the ground $\dot{I}_{Af}$; $\dot{I}^-_{ayy}$, $\dot{I}^-_{ayd}$, $\dot{Z}^-_{LRL}$, $\dot{Z}^-_{LC}$, $\dot{Z}^-_{C}$, $\dot{Z}^-_{RRL}$, $\dot{Z}^-_{RC}$, and $\dot{Z}^-_{eq}$ are the negative sequence components of $\dot{I}_{ayy}$, $\dot{I}_{ayd}$, $\dot{Z}_{LRL}$, $\dot{Z}_{LC}$, $\dot{Z}_{C}$, $\dot{Z}_{RRL}$, $\dot{Z}_{RC}$, and $\dot{Z}_{eq}$, respectively.

Then the Thevenin Equivalent circuit of the negative sequence diagram can be drawn in Figure 3-5.

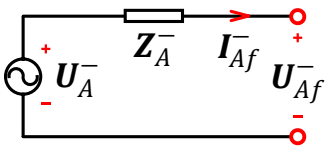


Figure 3-5 Thevenin Equivalent circuit of the negative sequence diagram looking into the fault point

According to Figure 3-4, the variables in Figure 3-5 can then be calculated as below:

$$\boldsymbol{Z}_A^- = (\boldsymbol{Z}_C^- // \boldsymbol{Z}_{LC}^- + \boldsymbol{Z}_{LRL}^-) // \boldsymbol{Z}_{LC}^- // \boldsymbol{Z}_{RC}^- // (\boldsymbol{Z}_{RC}^- // \boldsymbol{Z}_{eq}^- + \boldsymbol{Z}_{RRL}^-) \tag{3-5}$$

$$\begin{aligned}\boldsymbol{U}_A^- = &\left[\left(\frac{E_{N2}}{E_{N1}} \cdot \boldsymbol{I}_{ayy}^- + \frac{E_{N3}}{E_{N1}} \cdot \boldsymbol{I}_{ayd}^- \cdot 1\angle -30°\right) \cdot \frac{\boldsymbol{Z}_C^- // \boldsymbol{Z}_{LC}^-}{\boldsymbol{Z}_C^- // \boldsymbol{Z}_{LC}^- + \boldsymbol{Z}_{LRL}^-}\right] \\ &\cdot \left[(\boldsymbol{Z}_C^- // \boldsymbol{Z}_{LC}^- + \boldsymbol{Z}_{LRL}^-) // \boldsymbol{Z}_{LC}^- // \boldsymbol{Z}_{RC}^- // (\boldsymbol{Z}_{RC}^- // \boldsymbol{Z}_{eq}^- + \boldsymbol{Z}_{RRL}^-)\right]\end{aligned} \tag{3-6}$$

Besides, the expressions of the negative sequence component of the fault point phase-A voltage $\boldsymbol{U}_{Af}^-$ and that of the phase-A commutation bus voltage $\boldsymbol{E}_{Abus}^-$ can be derived as below:

$$\boldsymbol{U}_{Af}^- = \boldsymbol{U}_A^- - \boldsymbol{I}_{Af}^- \cdot \boldsymbol{Z}_A^- \tag{3-7}$$

$$\begin{aligned}\boldsymbol{E}_{Abus}^- = \boldsymbol{U}_{Af}^- &+ \left[\left(\frac{E_{N2}}{E_{N1}} \cdot \boldsymbol{I}_{ayy}^- + \frac{E_{N3}}{E_{N1}} \cdot \boldsymbol{I}_{ayd}^- \cdot 1\angle -30°\right) \cdot (\boldsymbol{Z}_C^- // \boldsymbol{Z}_{LC}^-) - \boldsymbol{U}_{Af}^-\right] \\ &\cdot \frac{\boldsymbol{Z}_{LRL}^-}{\boldsymbol{Z}_C^- // \boldsymbol{Z}_{LC}^- + \boldsymbol{Z}_{LRL}^-} \left(\frac{E_{N2}}{E_{N1}} \cdot \boldsymbol{I}_{ayy}^- + \frac{E_{N3}}{E_{N1}} \cdot \boldsymbol{I}_{ayd}^- \cdot 1\angle(-30°) + \frac{\boldsymbol{U}_{Af}^-}{\boldsymbol{Z}_{LRL}^-}\right) \\ &\cdot (\boldsymbol{Z}_C^- // \boldsymbol{Z}_{LC}^- // \boldsymbol{Z}_{LRL}^-)\end{aligned} \tag{3-8}$$

3) Zero Sequence:

Zero sequence components of the transformers vary with the transformer types and their winding connections. Based on the benchmark model, the impedance between the ground and the neutral point of the Thevenin Equivalent voltage source is neglected. According to [37], the zero sequence diagram can be plotted as shown in Figure 3-6:

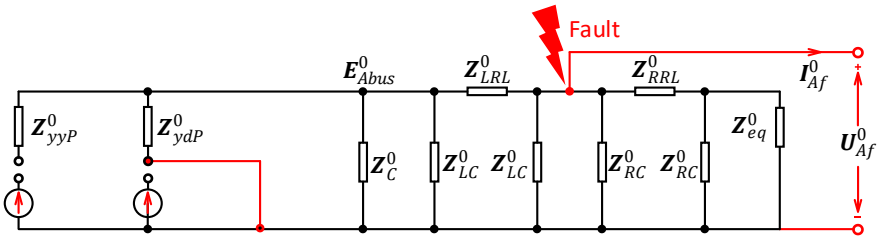


Figure 3-6 The zero sequence diagram of the system

where $\boldsymbol{Z}_{yyP}^{0}$ and $\boldsymbol{Z}_{ydP}^{0}$ are the zero sequence component of the primary side equivalent leakage impedance of the YY and YD transformers, respectively; $\boldsymbol{E}_{Abus}^{0}$ is the zero sequence component of the phase A potential of inverter bus; $\boldsymbol{U}_{Af}^{0}$ is the zero sequence component of the fault point potential $\boldsymbol{U}_{Af}$; $\boldsymbol{I}_{Af}^{0}$ is the zero sequence component of the fault point current to the ground $\boldsymbol{I}_{Af}$; $\boldsymbol{Z}_{LRL}^{0}$, $\boldsymbol{Z}_{LC}^{0}$, $\boldsymbol{Z}_{C}^{0}$, $\boldsymbol{Z}_{RRL}^{0}$, $\boldsymbol{Z}_{RC}^{0}$, and $\boldsymbol{Z}_{eq}^{0}$ are the zero sequence components of $\boldsymbol{Z}_{LRL}$, $\boldsymbol{Z}_{LC}$, $\boldsymbol{Z}_{C}$, $\boldsymbol{Z}_{RRL}$, $\boldsymbol{Z}_{RC}$, and $\boldsymbol{Z}_{eq}$, respectively.

Then the Thevenin Equivalent circuit of the zero sequence diagram can be plotted as shown in Figure 3-7.

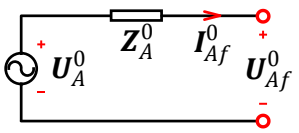


Figure 3-7 Thevenin Equivalent Circuit of the zero sequence diagram looking into the fault point

According to Figure 3-6, the variables in Figure 3-7 can then be calculated as below:

$$\boldsymbol{Z}_{A}^{0} = (\boldsymbol{Z}_{ydp}^{0}//\boldsymbol{Z}_{C}^{0}//\boldsymbol{Z}_{LC}^{0} + \boldsymbol{Z}_{LRL}^{0})//\boldsymbol{Z}_{LC}^{0}//\boldsymbol{Z}_{RC}^{0}//(\boldsymbol{Z}_{RC}^{0}//\boldsymbol{Z}_{eq}^{0} + \boldsymbol{Z}_{RRL}^{0}) \tag{3-9}$$

$$\boldsymbol{U}_{A}^{0} = 0 \tag{3-10}$$

Besides, the expressions of the zero sequence component of the fault point phase-A voltage $\boldsymbol{U}_{Af}^{0}$ and that of the phase-A commutation bus voltage $\boldsymbol{E}_{Abus}^{0}$ can be derived as below:

$$\boldsymbol{U}_{Af}^{0} = \boldsymbol{U}_{A}^{0} - \boldsymbol{I}_{Af}^{0} \cdot \boldsymbol{Z}_{A}^{0} = -\boldsymbol{I}_{Af}^{0} \cdot \boldsymbol{Z}_{A}^{0} \tag{3-11}$$

$$\begin{aligned} \boldsymbol{E}_{Abus}^{0} &= \boldsymbol{U}_{Af}^{0} + \left(0 - \boldsymbol{U}_{Af}^{0}\right) \cdot \frac{\boldsymbol{Z}_{LRL}^{0}}{\boldsymbol{Z}_{ydp}^{0}//\boldsymbol{Z}_{C}^{0}//\boldsymbol{Z}_{LC}^{0} + \boldsymbol{Z}_{LRL}^{0}} \\ &= \boldsymbol{U}_{Af}^{0} \cdot \frac{\boldsymbol{Z}_{ydp}^{0}//\boldsymbol{Z}_{C}^{0}//\boldsymbol{Z}_{LC}^{0}}{\boldsymbol{Z}_{ydp}^{0}//\boldsymbol{Z}_{C}^{0}//\boldsymbol{Z}_{LC}^{0} + \boldsymbol{Z}_{LRL}^{0}} \end{aligned} \tag{3-12}$$

4) Boundary conditions:

The relationships between the phase quantities and sequence quantities are shown below:

$$\begin{bmatrix} \boldsymbol{I}_{Af} \\ \boldsymbol{I}_{Bf} \\ \boldsymbol{I}_{Cf} \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & \boldsymbol{\alpha}^2 & \boldsymbol{\alpha} \\ 1 & \boldsymbol{\alpha} & \boldsymbol{\alpha}^2 \end{bmatrix} \begin{bmatrix} \boldsymbol{I}_{Af}^0 \\ \boldsymbol{I}_{Af}^+ \\ \boldsymbol{I}_{Af}^- \end{bmatrix} \tag{3-13}$$

$$\boldsymbol{\alpha} = 1\angle 120° \tag{3-14}$$

$$\boldsymbol{\alpha}^2 = 1\angle 240° \tag{3-15}$$

where $\boldsymbol{I}_{Af}$, $\boldsymbol{I}_{Bf}$ and $\boldsymbol{I}_{Cf}$ are the currents from the fault points on phase A, B, and C of the transmission line to the ground, respectively; $\boldsymbol{\alpha}$ is the operator which denotes $120°$ of phase shift.

The boundary conditions in the phase-A SLG fault case are shown below:

$$\boldsymbol{I}_{Bf} = \boldsymbol{I}_{Cf} = 0 \tag{3-16}$$

$$\boldsymbol{U}_{Af} = \boldsymbol{I}_{Af} \cdot \boldsymbol{Z}_{Af} \tag{3-17}$$

Applying (3-16) to (3-13), the solutions to the boundary conditions could be derived:

$$\boldsymbol{I}_{Af}^0 = \boldsymbol{I}_{Af}^+ = \boldsymbol{I}_{Af}^- = \frac{1}{3} \cdot \boldsymbol{I}_{Af} \tag{3-18}$$

$$\boldsymbol{U}_{Af} = 3\boldsymbol{I}_{Af}^+ \cdot \boldsymbol{Z}_{Af} = 3\boldsymbol{Z}_{Af} \cdot \boldsymbol{I}_{Af}^+ \tag{3-19}$$

Then the Thevenin Equivalent circuits of the three sequence diagrams should be connected in series with a serial impedance of $3\boldsymbol{Z}_{Af}$ based on (3-18) and (3-19), as shown in Figure 3-8.

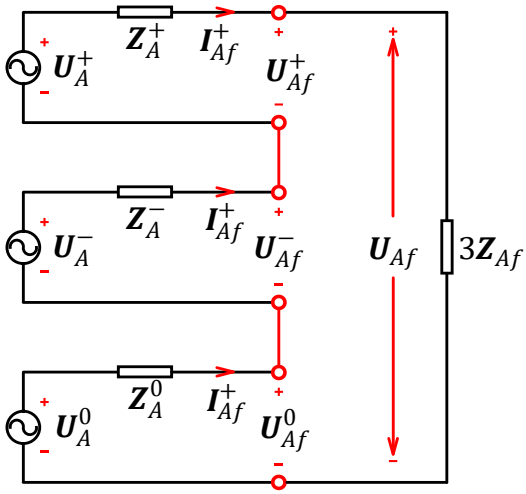


Figure 3-8 The joint circuit derived from boundary conditions

From Figure 3-8, $\boldsymbol{I}_{Af}^{+}$ can be calculated, and then the fault current $\boldsymbol{I}_{Af}$ can be obtained based on (3-13). After obtaining the three sequence components of $\boldsymbol{U}_{Af}$, the three sequence components of $\boldsymbol{E}_{Abus}$ could be calculated by (3-4), (3-8), and (3-12). The three phase inverter bus voltages can be finally calculated utilizing the phase-sequence transform (3-13).

Firstly, according to the KVL Law,

$$\boldsymbol{I}_{Af}^{+} = \frac{\boldsymbol{U}_A^{+} + \boldsymbol{U}_A^{-} + \boldsymbol{U}_A^{0}}{\boldsymbol{Z}_A^{+} + \boldsymbol{Z}_A^{-} + \boldsymbol{Z}_A^{0} + 3\boldsymbol{Z}_{Af}} \tag{3-20}$$

From (3-18), the fault current from the fault point to the ground can be calculated:

$$\boldsymbol{I}_{Af} = 3 \cdot \boldsymbol{I}_{Af}^{+} \tag{3-21}$$

By applying (3-21) to (3-3)-(3-12), the three sequence components of the phase-A commutation voltage $\boldsymbol{E}_{Abus}^{+}$, $\boldsymbol{E}_{Abus}^{-}$, and $\boldsymbol{E}_{Abus}^{0}$ can be derived.

5) Final expressions for three phase commutation voltages:

Then based on the SC theory, the three phase inverter bus voltages (commutation voltages)

could be derived as below:

$$\begin{bmatrix} \boldsymbol{E}_{Abus} \\ \boldsymbol{E}_{Bbus} \\ \boldsymbol{E}_{Cbus} \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & \boldsymbol{\alpha}^2 & \boldsymbol{\alpha} \\ 1 & \boldsymbol{\alpha} & \boldsymbol{\alpha}^2 \end{bmatrix} \begin{bmatrix} \boldsymbol{E}^0_{Abus} \\ \boldsymbol{E}^+_{Abus} \\ \boldsymbol{E}^-_{Abus} \end{bmatrix} \tag{3-22}$$

where

$$\boldsymbol{E}^+_{Abus} = \left(\frac{E_{N2}}{E_{N1}} \cdot \boldsymbol{I}^+_{ayy} + \frac{E_{N3}}{E_{N1}} \cdot \boldsymbol{I}^+_{ayd} \cdot 1\angle 30° + \frac{\boldsymbol{U}^+_A - \dfrac{\boldsymbol{U}^+_A + \boldsymbol{U}^-_A + \boldsymbol{U}^0_A}{\boldsymbol{Z}^+_A + \boldsymbol{Z}^-_A + \boldsymbol{Z}^0_A + 3\boldsymbol{Z}_{Af}} \cdot \boldsymbol{Z}^+_A}{\boldsymbol{Z}^+_{LRL}} \right) \cdot (\boldsymbol{Z}^+_C // \boldsymbol{Z}^+_{LC} // \boldsymbol{Z}^+_{LRL}) \tag{3-23}$$

$$\boldsymbol{E}^-_{Abus} = \left[\frac{E_{N2}}{E_{N1}} \cdot \boldsymbol{I}^-_{ayy} + \frac{E_{N3}}{E_{N1}} \cdot \boldsymbol{I}^-_{ayd} \cdot 1\angle(-30°) + \frac{\boldsymbol{U}^-_A - \dfrac{\boldsymbol{U}^+_A + \boldsymbol{U}^-_A + \boldsymbol{U}^0_A}{\boldsymbol{Z}^+_A + \boldsymbol{Z}^-_A + \boldsymbol{Z}^0_A + 3\boldsymbol{Z}_{Af}} \cdot \boldsymbol{Z}^-_A}{\boldsymbol{Z}^-_{LRL}} \right] \cdot (\boldsymbol{Z}^-_C // \boldsymbol{Z}^-_{LC} // \boldsymbol{Z}^-_{LRL}) \tag{3-24}$$

$$\boldsymbol{E}^0_{Abus} = -\frac{\boldsymbol{U}^+_A + \boldsymbol{U}^-_A + \boldsymbol{U}^0_A}{\boldsymbol{Z}^+_A + \boldsymbol{Z}^-_A + \boldsymbol{Z}^0_A + 3\boldsymbol{Z}_{Af}} \cdot \boldsymbol{Z}^0_A \cdot \frac{\boldsymbol{Z}^0_{ydp} // \boldsymbol{Z}^0_C // \boldsymbol{Z}^0_{LC}}{\boldsymbol{Z}^0_{ydp} // \boldsymbol{Z}^0_C // \boldsymbol{Z}^0_{LC} + \boldsymbol{Z}^0_{LRL}} \tag{3-25}$$

It can be seen from (3-22)-(3-25) that these final expressions of the three phase commutation voltages can be directly derived from the three sequence components of all the parts of the system.

Conclusions can be made that the expressions of the commutation voltages are more simplified than the ones derived by (2-27)-(2-29) in Chapter 2. Besides, the expressions of the three phase commutation voltages contain the negative and zero sequence components of all parts of the system since they are derived from the three sequence diagrams, which makes the calculation results more accurate than the method in Chapter 2 that does not consider the negative and zero sequence components of the devices in the system, e.g., not considering the negative and zero

sequence components of the equivalent current source.

In summary, all the voltage and current variables in the sequence network diagram of the inverter side under asymmetrical faults can be calculated.

3.4 Case Study

To verify the accuracy of the calculation results on the basis of the sequence network diagram, the system shown in Figure 3-1 is built and simulated on RTDS.

3.4.1 Simulation System

As mentioned above, the parameters of this system are listed in Table 3-1, which are based on the detailed CIGRE LCC-HVDC Benchmark system in [107]. The parameters of the transmission line are listed in Table 3-2.

Table 3-1 The parameters of the 12-pulse LCC-HVDC inverter side

Parameters	Value
AC System Frequency	50 Hz
Power Ratings of the YY & YD Transformers	598 MVA
Rated Secondary Side Voltage (Line to Line, RMS) of YY&YD Transformers	211.42 kV
Rated Primary Side Voltage (Line to Line, RMS) of YY&YD Transformers	230 kV
Leakage Reactance of the YY&YD Transformers	0.18 p.u.
Magnitude of the Currents of the Current Sources Connected to the YY&YD Transformers	2.205 kA
Current Phase of the Phase A of the YY Current Source	0 degree

Current Phase of the Phase A of the YD Current Source	30 degree
Capacitance of the Capacitors Connected to the Inverter Bus per Phase	7.522 uF
Thevenin Equivalent Impedance	5.4984+j20.466 ohm
Thevenin Equivalent Voltage (Line to Line, RMS)	215.05 kV
Thevenin Equivalent Voltage Phase	179.1 degree

Table 3-2 The parameters of the transmission line

Parameters	Value
Transmission Line Length	100 km
Positive/Negative Sequence Series Resistance	0.018547 ohm/km
Positive/Negative Sequence Series Inductive Reactance	0.37661 ohm/km
Positive/Negative Sequence Shunt Capacitive Reactance	0.2279e6 ohm·km
Zero Sequence Series Resistance	0.3618376 ohm/km
Zero Sequence Series Inductive Reactance	1.227747 ohm/km
Zero Sequence Shunt Capacitive Reactance	0.34514e6 ohm·km

3.4.2 Simulation Results

To comprehensively demonstrate the accuracy of the sequence network diagram derived in Section 3.3.2, the following six cases are studied:

Case 1: Varying current injections from the valve groups to the transformers by changing ratios of the positive, negative, and zero sequence components of the currents;

Case 2: Varying fault positions on the transmission line;

Case 3: Varying Points on Wave (POWs) of the fault on the phase-A commutation voltage waveform;

Case 4: Varying fault impedance;

Case 5: Varying phases of the Thevenin Equivalent voltage of the AC system;

Case 6: Varying lengths of the transmission line.

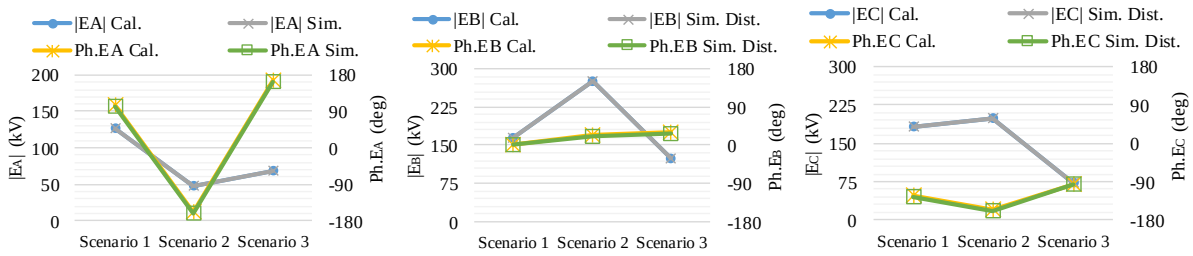
For each case study, three scenarios are developed for verifying the accuracy of the calculation results with varying parameters of the system. The details of the three scenarios for each case study are listed in Table 3-3.

Table 3-3 The details of the six case studies for verifying the calculation accuracy based on SC method

Study Cases	Varying Variable in Each Case	Three Scenarios for Each Case Study		
		Scenario 1	Scenario 2	Scenario 3
1	Current Injection (p.u.)* (Ibase. Mag =2205.5A)	+: $1\angle 0°$ -: $0.3\angle 70°$ 0: 0	+: $0.5\angle 0°$ -: $0.9\angle -150°$ 0: 0	+: $0.2\angle 0°$ -: $0.4\angle 150°$ 0: $0.6\angle -80°$
2	Fault Position on TL (%)*	50%	20%	70%
3	Fault Point on Wave (deg)	0	110	-80
4	Fault Impedance (ohm)	2	0.1	100
5	Esa+ Leading Iayy+ (deg)	179.1	50	290
6	TL Length (km)	100	50	200

*'+', '-', and '0' indicate the positive, negative, and zero sequence components, respectively; 'Fault Position on TL' depicts the percentage of the length from the fault point to the inverter bus out of the whole transmission line length.

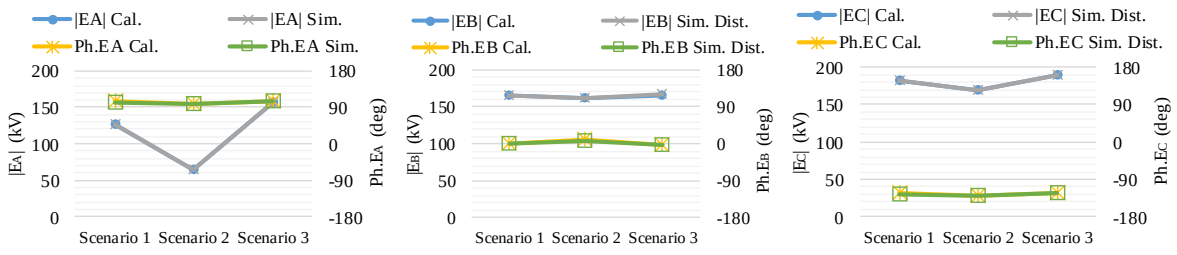
The calculation results based on the sequence network diagram and the simulation results based on RTDS are compared for the six case studies, and the comparison results are shown in Figure 3-9 - Figure 3-14.



(a) Phase A (b) Phase B (c) Phase C

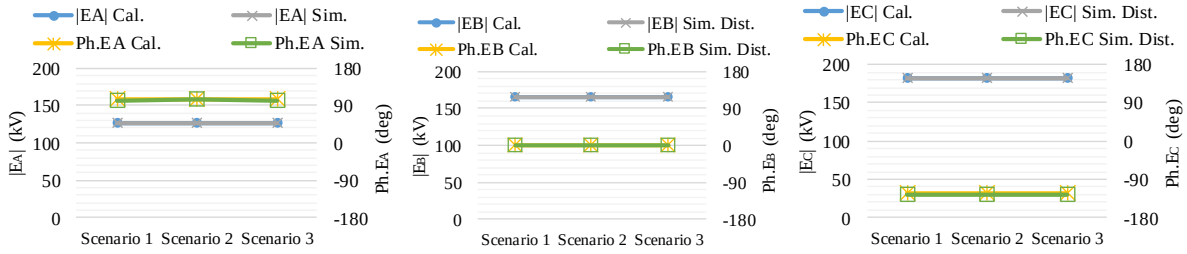
Figure 3-9 Comparisons of calculation and simulation results of the three scenarios of case study 1

Figure 3-9 shows the comparisons under the changing current injections in case study 1. The three scenarios in this case are used to study the accuracy of the calculation results under the normal operation condition and the abnormal status of the system with faults. It can be seen that under the phase-A SLG fault, the calculation results of the magnitudes and the phase angles of both the faulty phase and non-faulty phase commutation voltages are very close to the simulation results, and the error is around 0.5%.



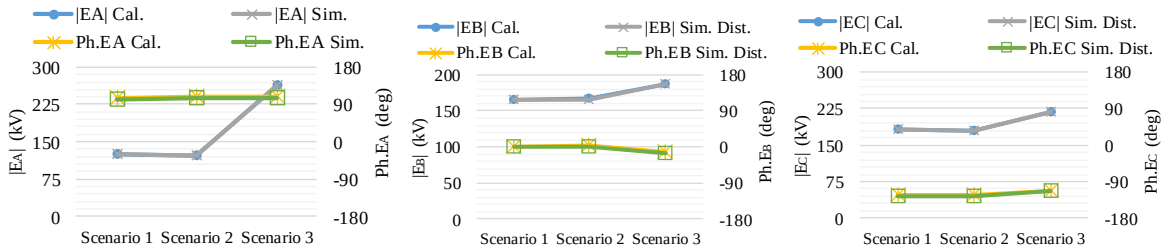
(a) Phase A (b) Phase B (c) Phase C

Figure 3-10 Comparisons of calculation and simulation results of the three scenarios of case study 2



(a) Phase A (b) Phase B (c) Phase C

Figure 3-11 Comparisons of calculation and simulation results of the three scenarios of case study 3



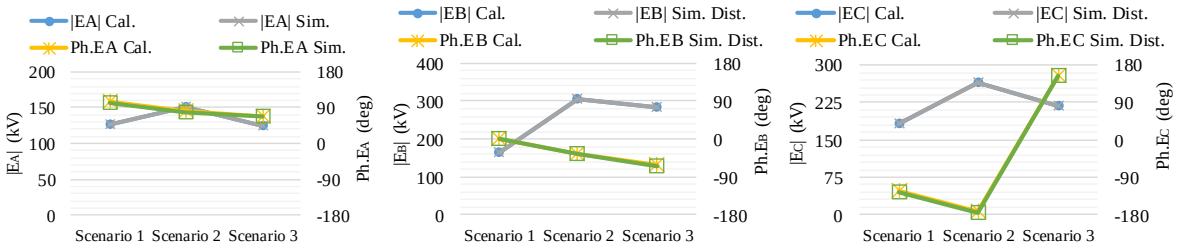
(a) Phase A (b) Phase B (c) Phase C

Figure 3-12 Comparisons of calculation and simulation results of the three scenarios of case study 4

Similar to Figure 3-9, Figure 3-10 presents the comparisons under faults with different fault positions, i.e., 50%, 20%, and 70% in Case 2. The three scenarios in this case are to verify the calculation accuracy under faults with different fault locations. Figure 3-11 shows the comparisons under faults with different POWs, i.e., 0 deg, 110 deg, and -80 deg in Case 3. Figure 3-12 depicts the comparisons under faults with different fault impedance, i.e., 2 ohms, 0.1 ohms, and 100 ohms in Case 4. Figure 3-13 presents the comparisons under faults with different phase shifts between the voltage and current sources, i.e., 179.1 deg, 50 deg, and 290 deg in Case 5. Figure 3-14 presents the comparisons under faults with different transmission line length, i.e., 100 km, 50 km, and 200 km in Case 6.

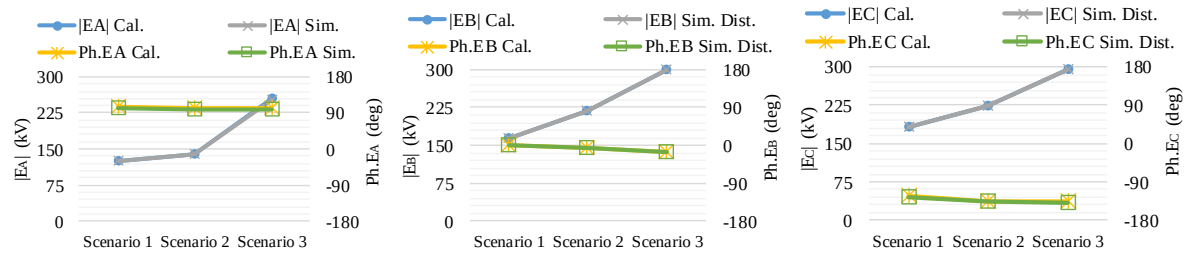
It can be seen from Figure 3-10 - Figure 3-14 that under the phase-A SLG faults with different locations, POWs, fault impedance, phase shifts between the voltage and current sources, and

different transmission line lengths, the calculation results of the magnitudes and the phase angles of both the faulty phase and non-faulty phase commutation voltages are very close to the simulation results, and the error is no more than 0.5%.



(a) Phase A (b) Phase B (c) Phase C

Figure 3-13 Comparisons of calculation and simulation results of the three scenarios of case study 5



(a) Phase A (b) Phase B (c) Phase C

Figure 3-14 Comparisons of calculation and simulation results of the three scenarios of case study 6

To conclude, the simulation results demonstrate that the calculations of the magnitudes and phase angles of the commutation voltages in the 12-pulse LCC-HVDC system under SLG faults based on the sequence network diagram are accurate and the error is less than 0.5%. Compared with the calculation results in Chapter 2 that have around 1% of error, the calculation results based on the SC method are more accurate and can be used to predict the CFs more accurately with the same steps as shown in Section 2.3.

3.5 Summary

This chapter develops the sequence network diagram of the 12-pulse LCC-HVDC inverter side and presents detailed derivations of the commutation voltages of the inverter under asymmetrical faults. Simulation results verify that the calculation results of the magnitudes and phase angles of both faulty phase and non-faulty phase commutation voltages based on the SC method are accurate with an error of 0.5%. The difference between the errors of the calculation results of Chapter 2 and Chapter 3 may be caused by the different transmission line models and that the method in Chapter 2 did not consider the negative and zero sequence components.

By using the accurate calculation results of magnitudes and phase angles of both the faulty and non-faulty commutation voltages in this chapter to predict CFs by following the steps as shown in Section 2.3.2, the accurate CF prediction can be achieved, which means it can be applied to large-scale LCC-HVDC projects to help the system operator forecast the occurrence of CFs under asymmetrical faults. It needs to be noticed that, again, the impact of the control systems and the voltage harmonics are not considered in this chapter, which may cause a larger error when applied in real projects but can be reduced by proper approaches, e.g., installing filters to reduce harmonics.

CHAPTER 4 Continuous Commutation Failure Prediction for Multi-Infeed LCC-HVDC Systems

4.1 Introduction

As mentioned in Section 1.2.2, the imbalance in phase angles and magnitudes of the three phase commutation voltages under asymmetrical faults will significantly affect the commutation process and potentially lead to CCFs. CCFs will bring higher risks to the voltage and frequency stability of the power system compared with NCCFs. However, few existing studies analyse the relationships between CFs, especially CCFs, and the magnitude and phase angle changes of all three commutation voltages under asymmetrical faults.

This chapter firstly delves into the principles of the phase shift and magnitude change of the commutation voltage under faults and analyses their impact on the commutation process. Then this chapter studies the commutation process with different types of CFs considering the impact of the control systems. Based on the above analysis, a new CCF prediction criterion according to the VTA theory is proposed.

The rest of this chapter is organised as follows: Section 4.2 analyses phase shifts and magnitude changes of the commutation voltages, as well as their impact on the commutation process under asymmetrical faults. Section 4.3 studies the detailed commutation process under the regulation of the control systems when CFs occur. Then a CCF prediction approach is raised in Section 4.4 based on the analysis in the above two sections. A case study based on RTDS is conducted in Section 4.5. Section 4.6 discusses CCF elimination approaches based on the achievements of this chapter, and Section 4.7 gives the summary of this chapter.

4.2 The Impact of Phase Shifts and Magnitude Changes on Commutations Under Asymmetrical Faults

To develop the CCF prediction method under asymmetrical faults, two aspects need to be considered: 1) the impact of phase shifts and magnitude changes of commutation voltages on the commutation process; 2) the impact of the control system on the commutation process.

The first aspect is analysed in this section and the second aspect will be studied in Section 4.3.

4.2.1 The Phase Shifts and Magnitude Changes of Commutation Voltages

To illustrate the phase shifts of the commutation voltages under fault conditions, the CIGRE LCC-HVDC Benchmark model [107] is utilised as shown in Figure 4-1. The inverter can be approximately regarded as a current source [34][51] to simplify the analysis.

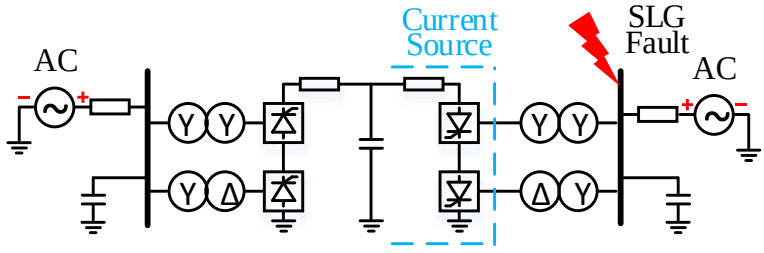
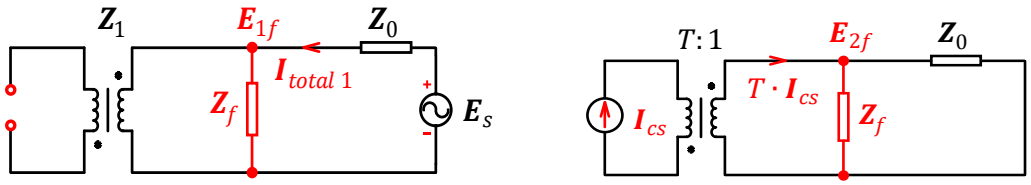


Figure 4-1 The CIGRE LCC-HVDC Benchmark.

When a fault occurs at the inverter bus, the equivalent single-line diagram of the faulty phase can be drawn as shown in Figure 4-2 based on the Superposition Theorem, where $\boldsymbol{Z}_0$ is the Thevenin Equivalent impedance of the AC system; $\boldsymbol{Z}_1$ is the impedance of the transformer; T:1 is the ratio of the transformer; $\boldsymbol{Z}_f$ is the fault impedance; $\boldsymbol{E}_{1f}$ and $\boldsymbol{E}_{2f}$ are the fault point voltages in the two equivalent circuits in the following figure; $\boldsymbol{E}_s$ and $\boldsymbol{I}_{CS}$ are the voltage source and current source values.



(a) Equivalent circuit containing the voltage source. (b) Equivalent circuit containing the current source

Figure 4-2 The single-line diagram of the equivalent circuit.

The commutation voltage $\boldsymbol{E_{CV}}$ can be calculated by summing up the corresponding voltages in Figure 4-2(a) and Figure 4-2(b):

$$\boldsymbol{E_{CV}} = \boldsymbol{E_{1f}} + \boldsymbol{E_{2f}} \tag{4-1}$$

For the circuit including the voltage source (Figure 4-2(a)):

The commutation voltage $\boldsymbol{E_{1f}}$ can be calculated as:

$$\boldsymbol{E_{1f}} = \boldsymbol{I_{total1}} \cdot \boldsymbol{Z_{1f}} = \boldsymbol{E_s} \cdot \frac{\boldsymbol{Z_1} \cdot \boldsymbol{Z_f}}{\boldsymbol{Z_1} \cdot \boldsymbol{Z_f} + \boldsymbol{Z_0} \cdot (\boldsymbol{Z_1} + \boldsymbol{Z_f})} \tag{4-2}$$

where

$$\boldsymbol{I_{total1}} = \frac{\boldsymbol{E_s}}{\boldsymbol{Z_{\text{total1}}}} \tag{4-3}$$

$$\boldsymbol{Z_{total1}} = \boldsymbol{Z_{1f}} + \boldsymbol{Z_0} \tag{4-4}$$

$$\boldsymbol{Z_{1f}} = \frac{\boldsymbol{Z_1} \cdot \boldsymbol{Z_f}}{\boldsymbol{Z_1} + \boldsymbol{Z_f}} \tag{4-5}$$

and $\boldsymbol{I_{total1}}$ is the current flowing through $\boldsymbol{Z_0}$; $\boldsymbol{Z_{total1}}$ is the total impedance; $\boldsymbol{Z_{1f}}$ is the impedance of the left part of the circuit during the fault.

Assuming the fault impedance is resistive, the impedance $\boldsymbol{Z_{\text{total1}}}$ with varying $\boldsymbol{Z_f}$ (from 10

ohms to 0.1 ohms) can be plotted in the phasor diagram based on (4-1):

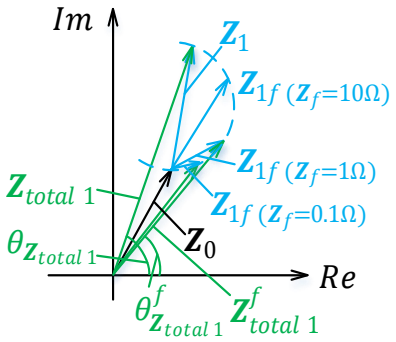
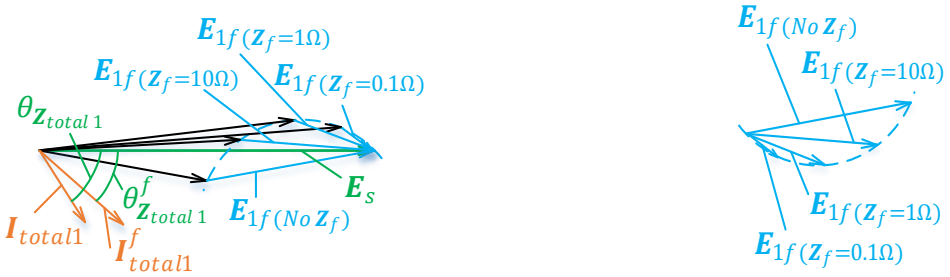


Figure 4-3 The Phasor Diagram of the total impedance $\boldsymbol{Z}_{\text{total1}}$.

where $\boldsymbol{Z}_{\text{total1}}$ and $\boldsymbol{Z}^f_{\text{total1}}$ are the pre-fault and during-fault total circuit impedance, respectively; $\theta_{\boldsymbol{Z}_{\text{total1}}}$ and $\theta^f_{\boldsymbol{Z}_{\text{total1}}}$ are their phase angles.

It can be seen from Figure 4-3 that the magnitude of the parallel impedance $\boldsymbol{Z}_{1f}$ keeps decreasing and its phase angle keeps lagging when faults occur in comparison with that in the pre-fault condition (See the blue vectors and blue trend line in Figure 4-3).

Assuming the phase of the voltage source $\boldsymbol{E}_s$ is zero, the phasor diagrams of the voltages are shown in Figure 4-4 with varying $\boldsymbol{Z}_f$:



(a) The phasor diagram of voltage vectors (b) The phasor diagram of the commutation voltage $\boldsymbol{E}_{1f}$

Figure 4-4 The Phasor diagrams of the equivalent diagram with the voltage source.

$\boldsymbol{I}^f_{\text{total1}}$ is the during-fault current flowing through $\boldsymbol{Z}_0$. It can be observed from Figure 4-4 that

with more severe faults, the voltage at the inverter bus $\boldsymbol{E}_{1f}$ keeps decreasing and lagging, compared with the pre-fault values.

For the circuit with the current source (Figure 4-2(b)):

The commutation voltage $\boldsymbol{E}_{2f}$ can be calculated as

$$\boldsymbol{E}_{2f} = \mathrm{T} \cdot \boldsymbol{I}_{cs} \cdot \boldsymbol{Z}_{\mathrm{total2}} = \mathrm{T} \cdot \boldsymbol{I}_{cs} \cdot \frac{\boldsymbol{Z}_0 \cdot \boldsymbol{Z}_f}{\boldsymbol{Z}_0 + \boldsymbol{Z}_f} \tag{4-6}$$

where

$$\boldsymbol{Z}_{\mathrm{total2}} = \frac{\boldsymbol{Z}_0 \cdot \boldsymbol{Z}_f}{\boldsymbol{Z}_0 + \boldsymbol{Z}_f} \tag{4-7}$$

Assuming the phase angle of the current source is zero, the relationships between $\boldsymbol{Z}_{\mathrm{total2}}$ with $\boldsymbol{Z}_f$ can be plotted in the phasor diagram in Figure 4-5 (a) and the phasor diagram of the commutation voltage $\boldsymbol{E}_{2f}$ is shown in Figure 4-5 (b).

(a) The phase diagrams of impedance. (b) The Phasor Diagram of the Commutation Voltage $\boldsymbol{E}_{2f}$.

Figure 4-5 The Phasor diagrams of the equivalent diagram with the voltage source.

Figure 4-5 shows that with lower fault impedance, the voltage at the inverter bus $\boldsymbol{E}_{2f}$ decreases and lags, compared with the pre-fault values.

By superimposing the two aforementioned circuits together according to (4-1), the phasor diagram of the final commutation voltage $\boldsymbol{E}_{CV}$ can be plotted.

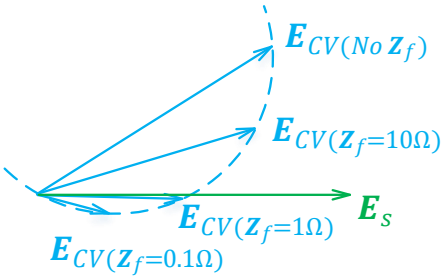


Figure 4-6 The phase diagrams of the final commutation voltage $\boldsymbol{E}_{CV}$

Figure 4-6 illustrates that when the fault impedance decreases, the magnitude of the commutation voltage $\boldsymbol{E}_{CV}$ decreases and the phase of it becomes more lagging as compared with the phase of the Thevenin Equivalent voltage source $\boldsymbol{E}_s$. This explains that when faults occur at the inverter side, the commutation voltages would drop and become lagging, which has been demonstrated in Chapter 2.

The same conclusion can be drawn when the phase angle difference between the voltage source and the current source varies, since the magnitude of the commutation voltage in each circuit of Figure 4-2 decreases and the phase angle lags when fault impedance decreases, no matter what the phase angle difference between the voltage source and current source is.

4.2.2 The Impact of Phase shifts and Magnitude Changes on Commutation Process Under Asymmetrical Faults

This section analyses the impact of the phase shifts and magnitude changes of the commutation voltages on the commutation process.

Under asymmetrical fault conditions, the phasor diagram of the three phase commutation voltages is shown in Figure 4-7.

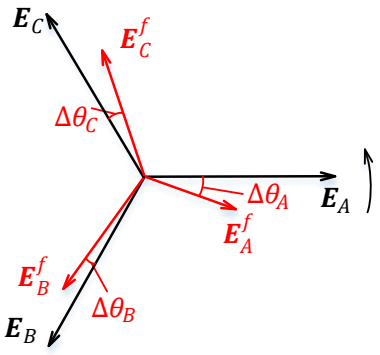


Figure 4-7 The phasor diagram of the phase commutation voltages before and during faults

Figure 4-7 shows that 1) All three phase voltage magnitudes decrease and their phase angles become lagging under asymmetrical faults, which has been proved in Chapter 2; 2) The voltage changes and phase shifts of the three phase commutation voltages under asymmetrical faults are different from each other due to the imbalance of the power system.

The asymmetry of phase shifts and magnitude changes of the three phase will lead to the imbalance among the commutation voltages, i.e., the three Line-to-Line voltages. Based on Figure 4-7, the phasor diagram of the three L-L commutation voltages can be plotted in Figure 4-8.

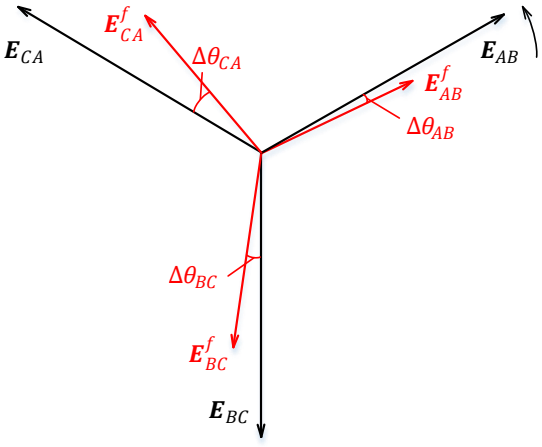
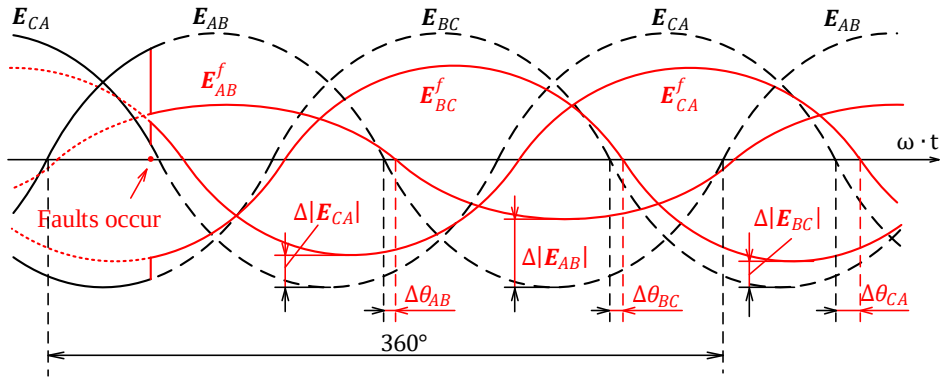


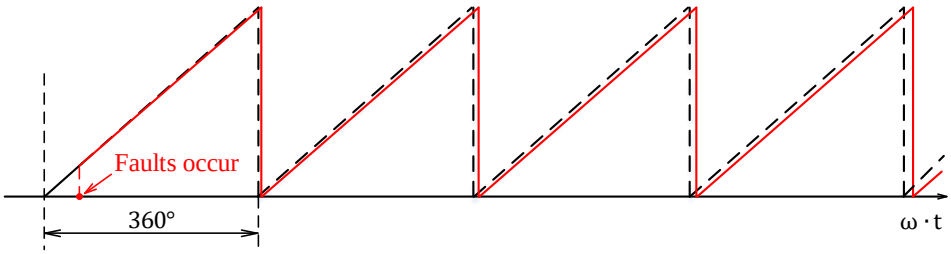
Figure 4-8 The phasor diagram of the Line-to-Line commutation voltages before and during faults

As can be seen from Figure 4-8 that 1) The phase shifts and magnitude changes of the three L-L commutation voltages are different from each other; 2) The phase angle difference between any two L-L commutation voltages no longer equals 120 electrical degrees.

Such changes of the commutation voltages have a significant impact on the commutation process. The commutation voltages before and during the asymmetrical faults are shown in Figure 4-9.



(a) L-L Commutation Voltages before and during Asymmetrical Faults



(b) PLL Output before and during Asymmetrical Faults

Figure 4-9 Commutation voltages and PLL output before and during asymmetrical faults

The black solid and dashed lines in Figure 4-9 (a) and Figure 4-9 (b) are the three L-L commutation voltage waveforms and Phase-Locked Loop (PLL) output before the faults, while the red ones are those during asymmetrical fault cases. It can be seen that:

1) During the first cycle after faults occur, a) the magnitude of the commutation voltage

decreases immediately, which exerts an adverse impact on the commutation process; b) the lagging phases benefit the commutation process; c) the DC current increases to a relatively high level compared with that in normal operation condition; d) CFs will occur if the DC current is not commutated to the next thyristor valve group successfully.

2) During the following several cycles, a) the PLL tracks the phase angles of the commutation voltages under asymmetrical faults and generates a phase-shifted saw-tooth reference waveform; b) the phase shift of the saw-tooth reference waveform during the fault keeps increasing; c) asymmetrically distributed zero-crossing points of the three L-L commutation voltages have a considerable impact on the overlap and extinction angles, and thus affect the commutation process; d) to be precise, the phase angle smaller than 120 electrical degrees between two adjacent zero-crossing points of the three L-L commutation voltages can cause insufficient overlap and extinction angles, i.e., an adverse impact on the commutation process; while the phase angle larger than 120 electrical degrees will benefit the commutation process; e) CFs will happen once the extinction angle is smaller than the minimum value required by the thyristor valve groups for maintaining successful commutations.

4.3 The Impact of Control Systems on Commutations Under Asymmetrical Faults

This section explains the impact of the control systems on commutations under asymmetrical faults.

To clearly explain this, CF is classified into three categories: FCF, non-continuous CF (NCCF), and continuous CF (CCF). FCF means the CF happens only for one cycle shortly after the fault.

As explained in section 1.1.2, NCCF indicates the CFs which occur intermittently after FCF, especially during the recovery process, and at least one cycle of successful commutation among the six thyristor valve groups in the inverter exists before NCCFs occur. CCF refers to the CFs which occur continuously after FCF in extreme fault conditions, and any cycles of the commutation process keep failing until the fault is removed, even under the adjustment of the control systems. It needs to be noted that the SCF mentioned before indicates general CFs after FCF, including NCCF and CCF. The impact of the control systems on the FCF, NCCF, and CCF is analysed in the rest of this section.

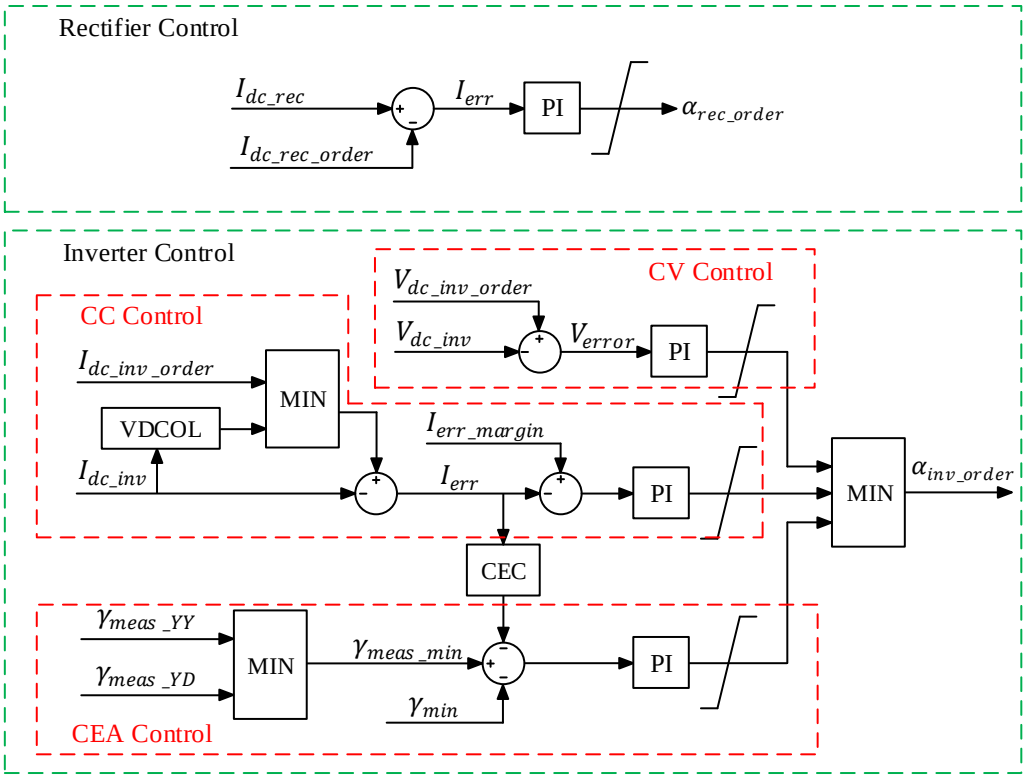


Figure 4-10 Block diagrams of LCC-HVDC control systems

The 6-machine-2-area (6M2A) system as shown in Figure 2-9 is used for the following analysis. The rectifier side of the LCC-HVDC controls the DC current (CC control) and the inverter side controls the DC voltage (CV control). The inverter is also equipped with minimum extinction angle control (CEA control) and CC control. The control system is shown in Figure 4-10, where

$V_{dc\_inv\_order}$, $I_{dc\_inv\_order}$, and γ_{min} are the reference values for the CV, CC, and CEA control systems, respectively; PI is the proportional integral (PI) controller; α_{inv_order}, i.e., AOI, is the minimum value of the outputs of the three control systems and will cooperate with the Phase-Locked Loop (PLL) output to generate firing pulses for thyristor valves.

By setting the reference values for the expected DC current, DC voltage and extinction angle, the CV, CC, and CEA controls are able to generate corresponding AOIs to the firing pulse generators to adjust the firing instant to achieve the goal of maintaining the measured values at their reference value levels by the PI controllers.

4.3.1 Impact of Control Systems on FCF

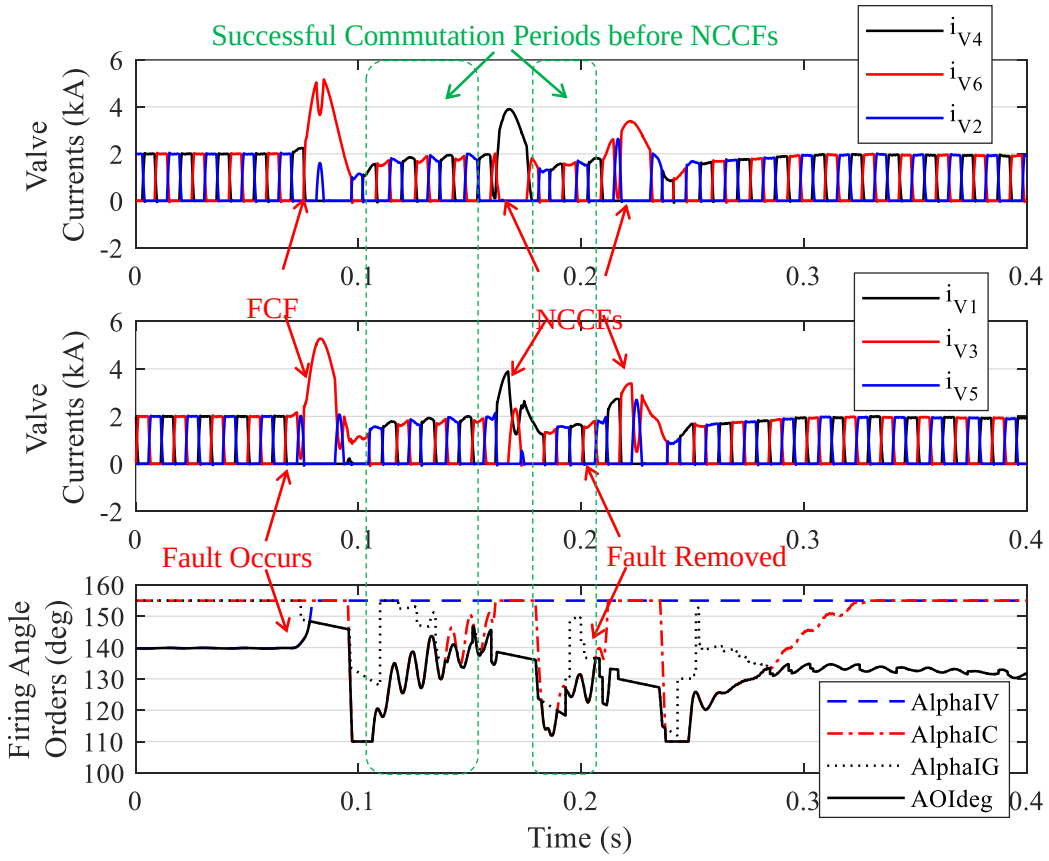


Figure 4-11 The commutation process when NCCFs occur

Figure 4-11 shows the simulation results under a remote SLG fault (on bus 4) with a duration

of 140 ms [110] where 'AlphaIV', 'AlphaIV' and 'AlphaIG' are the firing angle outputs of the CV, CC, and CEA control, respectively. 'AOIdeg' is the minimum value of the above three firing angles. It can be observed from the valve currents $\boldsymbol{i}_{V1}$, $\boldsymbol{i}_{V2}$,…, $\boldsymbol{i}_{V6}$ that there are three CFs after the fault.

When an AC fault takes place in the AC system at the inverter side, the phases of the commutation voltages become lagging according to the analysis in Section 4.2 and calculations in Chapter 2. The lagging phase angles increase the margin of the first commutation process after the fault compared with the margin in the pre-fault status, and hence benefit the commutation process. However, the commutation process will be affected adversely in the following aspects:

1) The inverter bus voltages drop and the DC side current surges. Both these two factors will increase the commutation time (the overlap angle μ) to achieve a successful commutation, based on the Voltage-Time Area (VTA) theory:

$$\int_{\alpha}^{\alpha+\mu} \boldsymbol{E}_{CV}\, dt = 2 \cdot \boldsymbol{I}_{dc} \cdot L_m \tag{4-8}$$

where $\boldsymbol{I}_{dc}$ is the DC current and L_m is the commutation inductance.

2) During the first period after the fault occurs, the firing angle order at the inverter side (AOI) is governed by the CV control. The CV control aims to maintain the DC voltage by adjusting the firing angle. As analysed in Section 4.2.2, the fault causes a sharp drop in the commutation voltages. Due to the relationship between the DC side voltage and the commutation voltages as shown in (4-9) [108], the DC voltage will decrease at the same time as the commutation voltages drop.

$$E_{dc} = \frac{3\sqrt{2}}{\pi} \cdot B \cdot T \cdot E_{L-L,RMS} \cdot \frac{\cos(\gamma) + \cos(\gamma + \mu)}{2} \quad (4\text{-}9)$$

where E_{dc} is the DC voltage; $E_{L-L,RMS}$ is the RMS value of the L-L commutation voltages; B is the number of 6-pulse bridges; T is the turns ratio of the converter transformer.

To maintain the DC voltage to the reference value, the firing angle α is raised by the CV control during the first 10 ms after the fault, as shown in Figure 4-11.

Overall, the extended overlap angle μ and the increasing firing angle α compress the extinction angle γ. Once the extinction angle γ is reduced to be smaller than the minimum value γ_{min} which is required by the valve groups for successful commutations, FCF will occur.

It needs to be pointed out that when FCF happens, the commutations are automatically recovered which does not cause sustained power interruptions to the AC system.

Under asymmetrical fault cases, the imbalance of the voltage magnitudes of the three phase commutation voltages will change the zero-crossing points of the L-L commutation voltages and consequently affect the commutation process. In the meantime, the phase shift of each phase commutation voltage will also influence the commutations. Detailed analysis will be presented in Section 4.4.

4.3.2 Impact of Control Systems on NCCF

As illustrated in Figure 4-11, during the first several periods after the FCF, the AOI provided is controlled firstly by the CV control for 10 ms, and then by both CEA and CC control systems. The detailed control process can be described as:

1) Firstly, the reason why the commutation process of the valve groups can recover from

the FCF and become successful for several periods before the NCCF is that the firing angle of the inverter valve groups is tuned to the minimum value by the CC control.

2) Once successful commutations are measured and the DC side current is lower than the rated value, the AOI will be raised by CC control until being governed by CEA control which aims to decrease the firing angle order to maintain the extinction angle at the pre-set value.
3) Although the commutation voltages will also increase due to the larger firing angle order, the higher DC side current (valve currents) and the smaller extinction angle may finally compress the extinction angle.
4) At the end of the first several successful commutation periods, the extinction angle γ finally drops down below the minimum value γ_{min}, and thus leads to the NCCF.
5) Once NCCF happens, the valve groups in one phase are short-circuited and the CC control will take over the firing angle order ('AOIdeg' in Figure 4-11) by outputting the minimum value of the firing order to achieve decreasing the DC side current.
6) The minimum firing angle order output by CC control can bring the valve groups back to successful commutating status and then the above 1)-5) steps will be repeated until the fault is removed.

However, considering the fact that AC faults are normally cleared within 100-200 ms, faults will disappear or get removed shortly. In this case, control systems are capable of adjusting the firing angle based on various measurement values to bring the system back to normal operation in time.

In conclusion, NCCFs are mainly caused by the control systems and can be regarded as harmless to the system since the system can automatically recover.

4.3.3 Impact of Control Systems on CCF

CCFs mean that the HVDC cannot transfer active power during the faults, thereby causing large frequency and voltage variations in the connected AC systems.

Figure 4-12 shows a zero-impedance 140 ms SLG fault at bus 4 where CCFs happen. It can be seen from Figure 4-12 that the inverter is under CV control at the very beginning, then under CEA and CC control during the first two cycles after the faults, and then under CEA control after t=0.15s.

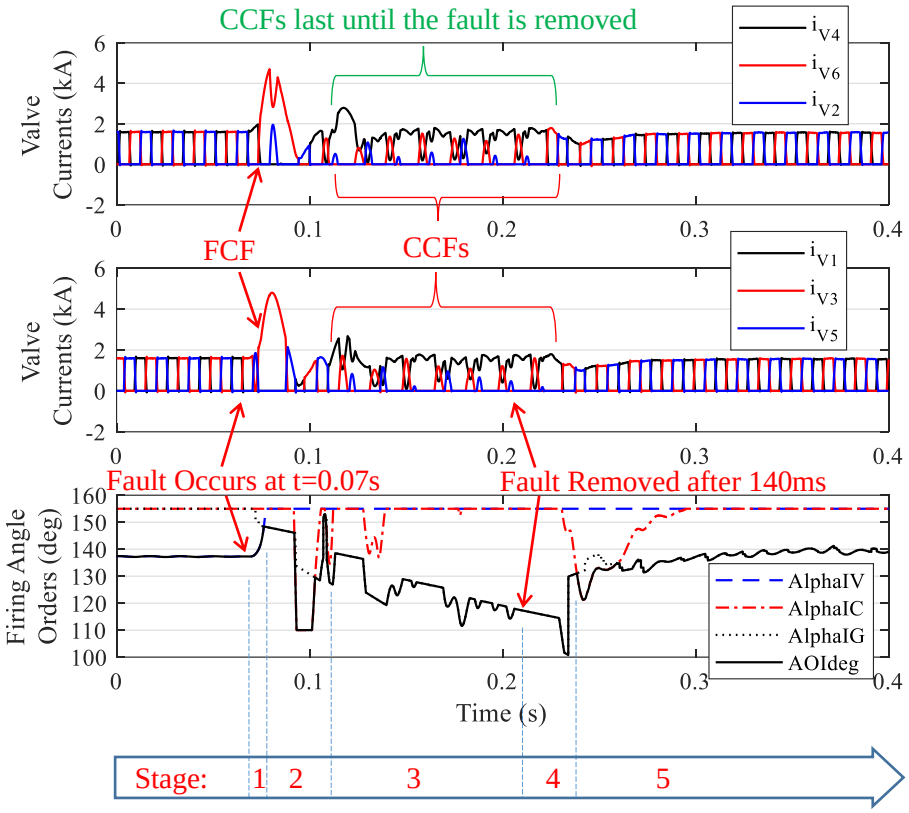


Figure 4-12 The commutation process when CCFs occur

To explain the process in detail, the fault case can be divided into the following stages:

Before the fault occurs:

The firing angle order of the inverter valve groups is controlled by the CV control to maintain

the rated level of the DC voltage. The firing angle order outputs from the other two control systems are higher than CV control due to the settings of the DC current margin and the constant extinction angle reference.

After the fault occurs:

Stage 1 (Half period after faults - FCF): This stage is the same as that described in Section 4.3.1. A. In summary, the increasing DC current and the decreasing commutation voltages will prolong the commutation process and thus compress the extinction angle. Also, the firing angle order will be raised by the CV control to maintain the DC voltage level, which can further reduce the margin of the extinction angle. Although the phase of the commutation voltages may become lagging, which will increase the margin of the extinction angle, FCFs may still occur when the minimum value of real extinction angles drops below the minimum required angle.

Stage 2 (Two periods after faults – Recover from FCF): After the FCF occurs, the output of the CV control keeps increasing while the CEA control output continues dropping. As a result, the final AOI will be coming from CEA control, as shown in Figure 4-12 at t=0.08s.

However, CEA control can only change the output slowly due to the parameter settings, and consequently, the commutation process cannot recover from the FCF in a short time until the firing angle order of the CC control drops to its minimum value.

The output of the CC control decreases sharply owing to the increase of the DC current and the drop of the DC side voltage. In this way, CC control then governs the final AOI, as shown in Figure 4-12 at t=0.09s, and this minimum AOI brings the commutation process back to be successful from the FCF.

After the system recovers from FCF, the DC current varies around the reference value due to the control systems. This may further lead to the varying firing angle order between the upper and lower limits in the CC control to maintain the DC current to the pre-setting reference value.

Meanwhile, the firing angle order from CEA control decreases gradually on account of the rate limiter built within it.

As a result, the firing angle order outputs of the CC control and CEA control could have several crossing points before the CC control output reaches its maximum limit when the DC current trends to the reference value.

During this stage 2, the AOI for the inverter valve groups is governed alternately by the CEA control and CC control, as shown in Figure 4-12 from t=0.08s to t=1.1s.

Stage 3 (CCFs last until the fault is removed): After the last crossing point of the CC control and CEA control at t=1.1s as shown in Figure 4-12, the AOI is controlled by the CEA control system. Since CCFs occur, CEA control needs to keep decreasing its output to maintain the extinction angle until the output reaches its minimum limit. During this stage, the system operates with CCFs until the fault is removed.

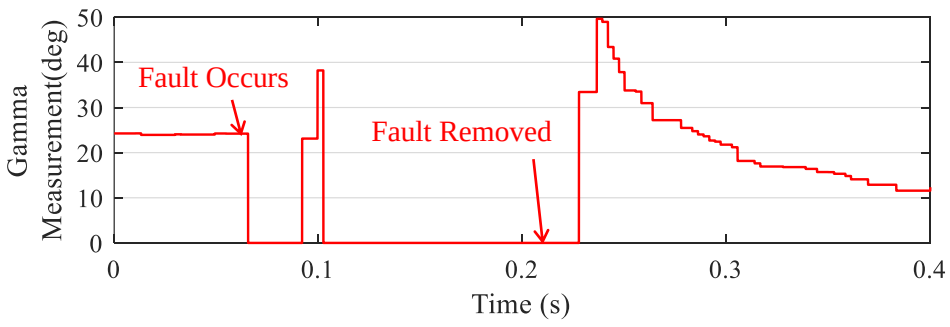


Figure 4-13 The extinction angle measurement value when CCFs occur

Figure 4-13 shows that after the system recovers from FCF at t=0.09s, the minimum measurement value of the real extinction angles of the inverter valve groups reaches zero deg

again at t=0.102s and keeps at zero until the end of the fault. This indicates that during Stage 3, the CCFs cannot be prevented by the adjustment of the control system.

It needs to be noticed that the extinction angle measurement as shown in Figure 4-13 is the minimum value. Under balanced faults, the extinction angles of the valve groups in three phases are nearly the same with each other because the circuits of the three phases are balanced. However, under asymmetrical fault, the minimum value of the extinction angle will be affected significantly by the imbalance of the commutation voltages. The impact of the imbalance on CCFs will be analysed in detail in Section 4.4.2.

Stage 4 (Recover from CCFs after the fault is removed): CCFs cannot be eliminated immediately after the fault is removed. The reason is that the phase angles of the commutation voltages will be leading after the fault is removed, compared with those during the fault, which has been analysed in Section 4.2.2. As a result, the firing angle order from the CEA control keeps decreasing until the CCFs disappear, as shown in Figure 4-12 from t=0.21s to t=0.23s.

Once the CCFs disappear, the AOI governed by CEA control would increase to keep the extinction angle near its reference.

However, increasing the firing angle, which is aiming to increase the DC voltage, will also decrease the DC current since the voltage difference between the two converters is reduced. This is the reason why the firing angle order of the CC control drops sharply at t=2.3s in Figure 4-12.

Besides, the DC side currents will decrease as the equivalent impedance of the whole AC system at the inverter side increases after the fault is removed. The decreasing DC current leads to the reduction of the firing angle order output of CC control which is aiming at keeping the DC current at the pre-setting level, as illustrated in Figure 4-12 at t=2.3s. Consequently, the

lower firing angle order from the CC control will further increase the voltage difference between two converters and then achieve the maintenance of the DC current at the constant DC current reference level.

In conclusion, after the fault is removed, the CCFs are eliminated during this stage.

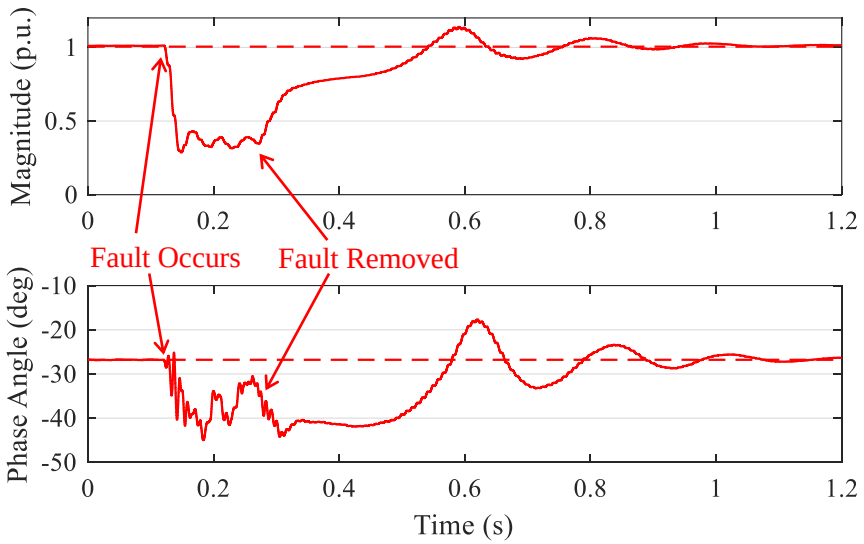


Figure 4-14 The magnitude and phase angle of the phase A commutation voltage

Stage 5 (Recover from unbalanced status to balanced status): This stage will last for a relatively long period of time compared with the four stages before the whole system gets back to the normal operation condition. As demonstrated in Figure 4-14, it takes hundreds of milliseconds for the abovementioned system to recover. The duration of this stage is mainly affected by the parameters of the AC system and the control systems.

Out of the above Stage 1-5, Stage 3 brings the most adverse risks to the power system. Firstly, the thyristors in these valve groups have considerable risks of burning out due to the unexpectedly long time of conduction during CCFs. Secondly, the CCFs may result in the interruption of the active power transmission of the HVDC and consequently lead to the blocking of the HVDC link. Finally, the blocking of the HVDC link may result in the collapse

of adjacent power transmission links and then the blackout of the power system. As a result, Stage 3 needs to be brought to the forefront and analysed in detail, which will be presented in Section 4.4.2.

It needs to be highlighted that the lagging phase angles of L-L commutation voltages under faults will not always benefit the commutation process: 1) They only benefit the commutations in the first period after the fault; 2) During faults, they have no impact on the commutations if faults are symmetrical. However, they can adversely affect the commutation process under asymmetrical faults; 3) They bring adverse consequences to the commutations within the first period after the fault is removed, since the lagging phase shifts can recover to pre-fault status and become zero gradually.

For the above five stages, all the analysis and conclusions are based on the specific above-mentioned three control systems (CV, CC, and CEA). These control systems and their limits can be surely adjusted accordingly, and the conclusions achieved will be similar. For instance, when the Voltage Dependent Current Order Limiter (VDCOL) control system is inserted into the CC control at the inverter side, the firing angle order of the CC control would decrease due to the reduced DC current reference by the CC control when measuring the decreasing DC voltage. Lower CC output will reduce the requirement of the commutation process and the CC control may govern the AOI in Stage 3.

4.4 CCF Prediction Under Asymmetrical Faults

As mentioned above CCF is the most hazardous event for the active power transmission, so it is of great importance to predict the CCF risks for the inverters in power grids. Therefore, this section proposes a CCF prediction approach based on the VTA theory under asymmetrical

faults on account of the analysis in the above two sections.

Firstly, the maximum reduction of AOI caused by the control systems will be analysed, and then the detailed commutation process will be illustrated, followed by the proposition of the CCF prediction approach.

4.4.1 Calculation of the Maximum Adjustment of Control Systems

It needs to be pointed out that the control systems can adjust the firing angle order for the inverter valve groups during and after the faults, and the firing instant will be also changed based on the shifted phases of commutation voltages tracked by PLL.

When faults occur, the firing angle for the thyristor valves will be reduced by the control system which is attempting to eliminate the CFs or maintain related variables around their reference values, as shown in Figure 4-11 and Figure 4-12. Meanwhile, the PLL will output a lagging reference phase signal (saw-tooth waveforms) aiming to track the phase of the commutation voltages which becomes lagging after faults as shown in Figure 4-9. Once the control systems cannot bring the system back to a pseudo quasi-steady state during the fault, CCFs occur.

With faults getting worse, the advancing angle $\Delta\alpha$ of the firing angle order from the control systems will increase.

Thus, to take into account the impact of the control systems when predicting the CCFs, the advancing angle $\Delta\alpha$ of the firing angle order from the control systems during faults needs to be considered.

It is worth noticing that the maximum reduction of AOI $\Delta\alpha_{max}$ caused by the control systems under asymmetrical faults can be obtained under the most extreme fault, i.e., zero-impedance SLG fault on the inverter bus. By using the Multi-Infeed LCC-HVDC system as mentioned in

Section 4.3, the CCFs take place and last until the fault is removed. The firing angle order curves for the inverter are shown in Figure 4-15.

From Figure 4-15, it can be observed that under extreme fault conditions, CCFs occur until the fault is removed. It is the CEA control that governs AOI in Stage 3 as mentioned in Section 4.3.3. The trendline of the CEA output is nearly a straight line with a constant slope. Therefore, the maximum reduction of AOI $\Delta\alpha_{max}$ can be obtained by deriving the slope.

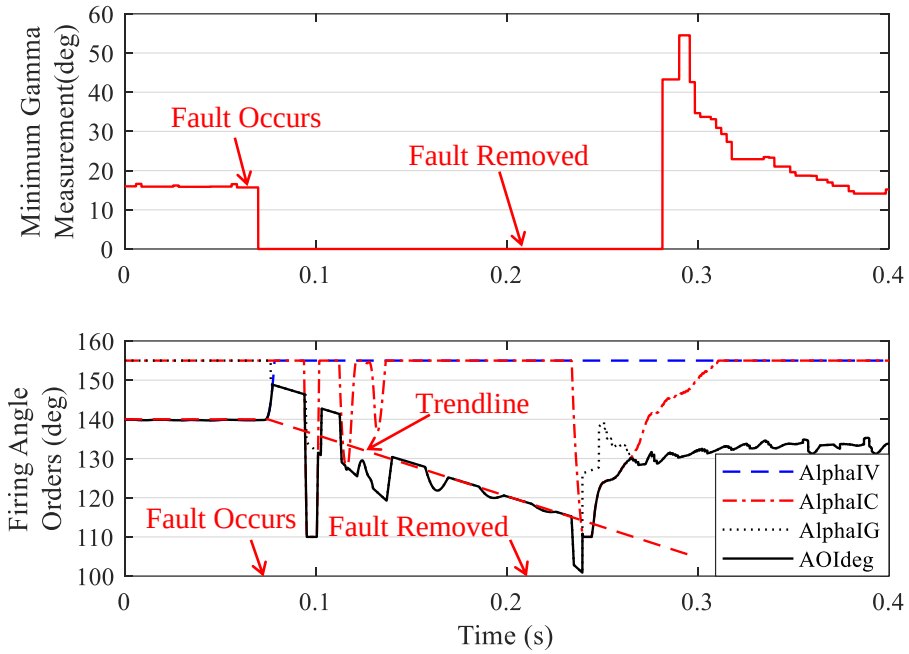


Figure 4-15 Minimum extinction angle measurement and firing angle order at the inverter side when Zero-Impedance SLG fault occurs on inverter bus

Based on the configuration of the CEA control which is commonly applied in the LCC-HVDC Benchmark [43][107][111], the slope of the trendline $a_{trendline}$ can be derived and simplified into (4-10).

$$a_{trendline} = \gamma_{min} \cdot \left(1 + \frac{1}{T_I}\right) \tag{4-10}$$

where T_I is the time constant of the integration part within the PI controller of the CEA control.

Hence the maximum reduction of AOI $\Delta\alpha_{max}$ can be obtained:

$$\Delta\alpha_{max} = a_{trendline} \cdot t_{max} \tag{4-11}$$

where t_{max} is the maximum time duration for the control system to adjust the firing angle order during the fault, which can be considered as the maximum fault duration.

4.4.2 The Detailed Commutation Process When CCFs Occur

To predict CCFs, the following two factors need to be considered when utilizing the VTA theory: 1) the actual overlap angle for the commutation process during the fault; 2) the actual commutation voltages during the fault.

To determine the actual overlap angle, the actual firing instant and the reversing points of the commutation voltages (e.g., from negative to positive) need to be estimated. The calculation method for the commutation voltages in Chapter 2 is utilised in this chapter.

As mentioned in Section 4.2.2, every two adjacent commutation voltages are considered as a 'pair' of commutation voltages which will affect the corresponding commutation processes.

Since the phase shift of the PLL output $\Delta\theta_{PLL}$ is between the maximum and minimum phase shifts of the commutation voltages, i.e., $\Delta\theta_{CA}$ and $\Delta\theta_{AB}$ (as discussed in Section 4.2.2), the reference of firing time instant is earlier than the zero-crossing point of the most relative lagging commutation voltage but later than the most relative leading commutation voltage, as demonstrated in Figure 4-16.

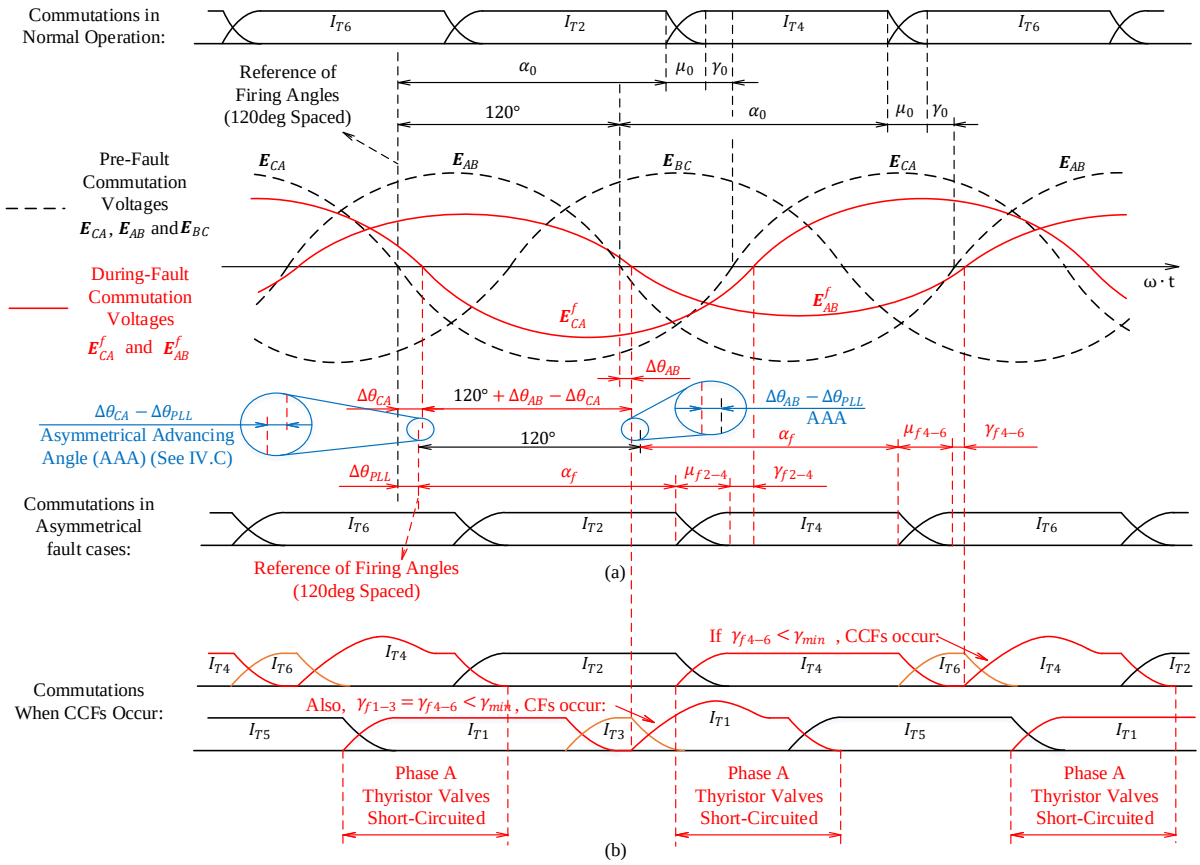


Figure 4-16 Detailed commutation process when CCFs occur (a) The pre-fault and during-fault commutation process of $I_{T2} \rightarrow I_{T4}$ and $I_{T4} \rightarrow I_{T6}$under asymmetrical faults (b) Commutations when CCFs occur

Figure 4-16 (a) shows the comparison of the commutation process of $I_{T2} \rightarrow I_{T4}$ and $I_{T4} \rightarrow I_{T6}$ between per-fault status and during-fault status under asymmetrical faults. It can be seen that:

1) In the normal operation condition, the magnitudes of the three L-L commutation voltages $\boldsymbol{E}_{AB}$, $\boldsymbol{E}_{BC}$, and $\boldsymbol{E}_{CA}$ are the same and their phases are 120° equally spaced, and consequently the extinction angles of all commutations are equal to γ_0;

2) Under asymmetrical fault conditions, the L-L commutation voltages have different magnitudes, and their phases are also unbalanced: the phase shifts of the during-fault voltages $\boldsymbol{E}^f_{CA}$ and $\boldsymbol{E}^f_{AB}$ are $\Delta\theta_{CA}$ and $\Delta\theta_{AB}$, respectively. To clearly illustrate the commutation process, assume$\left|\boldsymbol{E}^f_{CA}\right| > \left|\boldsymbol{E}^f_{AB}\right|$, and $\Delta\theta_{CA}$ is the largest while $\Delta\theta_{AB}$ is the smallest;

3) Assume $\Delta\theta_{PLL}$ during the fault is between $\Delta\theta_{CA}$ and $\Delta\theta_{AB}$ (this assumption will not affect the final conclusion);

4) Since $\Delta\theta_{CA}$ is larger than $\Delta\theta_{PLL}$, the firing instant for I_{T4} in the commutation process $I_{T2} \rightarrow I_{T4}$ is relatively advanced, which will increase the margin of the extinction angle of I_{T2} and benefit this commutation process;

5) The firing angles for the three phase valves will be $120°$ equally spaced in a very short period of time, e.g., 10 ms. Thus $120°$ after I_{T4} is fired, I_{T6} will be fired for achieving the commutation process $I_{T4} \rightarrow I_{T6}$;

6) As $\Delta\theta_{CA}$ is larger than $\Delta\theta_{AB}$, the extinction angle γ_{f4-6} of the commutation process $I_{T4} \rightarrow I_{T6}$ will be smaller than the extinction angle γ_{f2-4} of $I_{T2} \rightarrow I_{T4}$, and the difference between them is $|\Delta\theta_{CA} - \Delta\theta_{AB}|$ if the magnitude changes are the same and the overlap angles are the same, as expressed in (4-12).

$$\gamma_{f2-4} - \gamma_{f4-6} = \Delta\theta_{CA} - \Delta\theta_{AB} \tag{4-12}$$

It needs to be pointed out when considering the magnitude changes and $\left|\boldsymbol{E}_{CA}^{f}\right| > \left|\boldsymbol{E}_{AB}^{f}\right|$, the overlap angle μ_{f4-6} of $I_{T4} \rightarrow I_{T6}$ affected by $\boldsymbol{E}_{AB}^{f}$ will be extended and become larger than μ_{f2-4} of $I_{T2} \rightarrow I_{T4}$ affected by $\boldsymbol{E}_{CA}^{f}$, due to the VTA theory. As a result, the difference between γ_{f2-4} and γ_{f4-6} will be larger than $|\Delta\theta_{CA} - \Delta\theta_{AB}|$, as indicated in (4-13).

$$\gamma_{f2-4} - \gamma_{f4-6} > \Delta\theta_{CA} - \Delta\theta_{AB} \tag{4-13}$$

To consider both (4-12) and (4-13), the ignition advance angle β is utilised, which equals the sum of the overlap angle μ and the extinction angle γ. Then the difference between the ignition advance angles of the two abovementioned commutation processes can be expressed in (4-14).

$$\Delta\beta_{2-4/4-6} = \beta_{f2-4} - \beta_{f4-6} = \left(\mu_{f2-4} + \gamma_{f2-4}\right) - \left(\mu_{f4-6} + \gamma_{f4-6}\right) = \Delta\theta_{CA} - \Delta\theta_{AB} \quad (4\text{-}14)$$

The difference of the ignition advance angles $\Delta\beta_{2-4/4-6}$ indicates the difference between phase angle shifts of the two corresponding commutation voltages under asymmetrical faults. It brings a significant adverse impact and consequently leads to CFs as a result of the mismatch between the reference instant of the firing angle and the zero-crossing point of the commutation voltage;

7) Once the minimum extinction angle γ_{f4-6} is less than the minimum required extinction angle γ_{min}, CFs will occur.

Figure 4-16 (b) shows the six commutation processes within an inverter when $\gamma_{f4-6} < \gamma_{min}$ under asymmetrical faults. It can be seen that the insufficient extinction angle will affect the corresponding commutation processes within both the upper thyristor arms and lower thyristor arms, i.e., $I_{T1} \rightarrow I_{T3}$ and $I_{T4} \rightarrow I_{T6}$. CCFs will last until the fault is removed.

With CCFs, the overlap period of I_{T1} and I_{T4} will make the thyristor valve leg (phase A) short-circuited periodically, which will increase thyristors' conducting time and cause risks of burning them out.

In conclusion, the relative lagging L-L commutation voltage and the next relative leading L-L commutation voltage will result in the phase angle mismatch between the reference instant of the firing angle and the actual zero-crossing point of the commutation voltage under asymmetrical faults. This will significantly reduce the upcoming commutation margin and hereby causing CCF risks.

4.4.3 The CCF Prediction Criterion

Based on the analysis in Section 4.4.2, the commutation voltage and the overlap angle need to be estimated before predicting CCFs.

From Figure 4-16 and (4-14), the ignition advance angle for each commutation process can be derived:

$$\beta_{f2-4} = \mu_{f2-4} + \gamma_{f2-4} = 180° + \Delta\theta_{CA} - \Delta\theta_{PLL} - \alpha_f \tag{4-15}$$

$$\begin{aligned}\beta_{f4-6} = \mu_{f4-6} + \gamma_{f4-6} &= 180° + 120° + \Delta\theta_{AB} - \Delta\theta_{PLL} - 120° - \alpha_f \\ &= 180° + \Delta\theta_{AB} - \Delta\theta_{PLL} - \alpha_f\end{aligned} \tag{4-16}$$

$$\alpha_{f.min} = \alpha_0 - \Delta\alpha_{max} \tag{4-17}$$

where $\alpha_{f.min}$ is the minimum firing angle before the fault is removed, which can enable the AC system to provide the maximum VTA value to the inverter valves.

$$VTA_{if.max} = \int_{\alpha_{f.min}-(\Delta\theta_i-\Delta\theta_{PLL})}^{180°-\alpha_{f.min}+(\Delta\theta_i-\Delta\theta_{PLL})-\gamma_{min}} V_{if}(t)dt \tag{4-18}$$

where $i = 1,2,\dots,6$ is the order of the six commutation processes during a period; V_{if} is the corresponding L-L commutation voltage of the i^{th} commutation process and $\Delta\theta_i$ is its phase shift; $VTA_{if.max}$ indicates the maximum VTA provided by the AC system under the minimum firing angle order of the i^{th} commutation process in fault cases.

It needs to be noticed that the starting point of the integral of the commutation process is not α_{fmin}. The reason is that α_{fmin} is not starting at the actual zero-crossing point of the corresponding L-L commutation voltage. The starting instant of α_{fmin} is leading the zero-crossing point of the actual commutation voltage by $(\Delta\theta_i - \Delta\theta_{PLL})$, named as 'Asymmetrical

Advancing Angle (AAA)', which can be found in Figure 4-16.

Through observation, the $\Delta\beta_{2-4/4-6}$in (4-14) is the AAA difference ($AAAD_{ij}$) between i^{th} and j^{th} commutation process.

$$AAAD_{ij} = AAA_i - AAA_j = (\Delta\theta_i - \Delta\theta_j) \tag{4-19}$$

Through the illustration of (4-15) and analysis, it can be concluded that six commutation processes are affected by the three $AAADs$: $\Delta\theta_{CA} - \Delta\theta_{AB}$, $\Delta\theta_{BC} - \Delta\theta_{CA}$, and $\Delta\theta_{AB} - \Delta\theta_{BC}$, as shown in Table 4-1.

Table 4-1 Corresponding AAAD of the six commutation processes

i^{th} commutation process	Commutating Thyristor Valves	Corresponding Commutation Voltage	Process Affected by $AAAD_{ij}$	$AAAD_{ij}$ Calculation Results
1	$T1 \rightarrow T3$	$\boldsymbol{E}_{AB}$	$AAAD_{51}$	$\Delta\theta_{CA} - \Delta\theta_{AB}$
2	$T2 \rightarrow T4$	$-\boldsymbol{E}_{CA}$	$AAAD_{62}$	$\Delta\theta_{BC} - \Delta\theta_{CA}$
3	$T3 \rightarrow T5$	$\boldsymbol{E}_{BC}$	$AAAD_{13}$	$\Delta\theta_{AB} - \Delta\theta_{BC}$
4	$T4 \rightarrow T6$	$-\boldsymbol{E}_{AB}$	$AAAD_{24}$	$\Delta\theta_{CA} - \Delta\theta_{AB}$
5	$T5 \rightarrow T1$	$\boldsymbol{E}_{CA}$	$AAAD_{35}$	$\Delta\theta_{BC} - \Delta\theta_{CA}$
6	$T6 \rightarrow T2$	$-\boldsymbol{E}_{BC}$	$AAAD_{46}$	$\Delta\theta_{AB} - \Delta\theta_{BC}$

The maximum value $AAAD_{max}$ can be expressed in (4-20).

$$AAAD_{max} = (\Delta\theta_{max} - \Delta\theta_{min}) \tag{4-20}$$

where $\Delta\theta_{max}, \Delta\theta_{min}$ indicate the maximum and minimum values of the phase shifts of the corresponding L-L commutation voltages of the six commutation processes.

Besides, AAA will be equal to zero in symmetrical faults since the three commutation voltages

are balanced.

Due to the imbalance of the three L-L commutation voltages, CCFs will firstly occur in the phase which is provided with the minimum VTA by the AC system. In this case, the minimum value of the six maximum VTAs for the six commutation processes will be utilised to predict the CCFs, as expressed in (4-21).

$$VTA_{prov.min}^{fault} = min\{VTA_{if.max}\}, \qquad i = 1,2,\dots 6 \tag{4-21}$$

It can be seen that to predict CCFs based on the VTA theory, the magnitudes and phases of the commutation voltage and the maximum reduction of AOI $\Delta\alpha_{max}$ are needed.

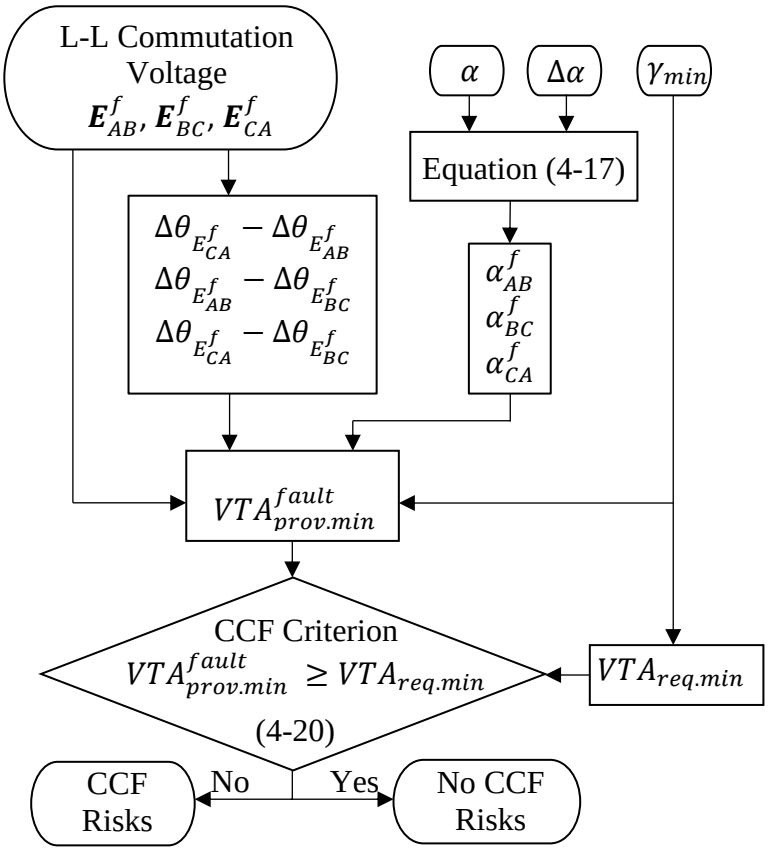


Figure 4-17 The flow chart of the CCF prediction process

On the basis of the commutation voltage calculation methods from previous chapters, and the

$\Delta\alpha_{max}$ obtained from Section 4.4.1, the CCFs can be predicted by comparing the minimum VTA provided by the AC system under asymmetrical faults and the minimum VTA required by the thyristor valves, as shown in (4-22).

$$\begin{cases} VTA_{prov.min}^{fault} \geq VTA_{req.min}, & \rightarrow \ No\ CCF\ risk \\ VTA_{prov.min}^{fault} < VTA_{req.min}, & \rightarrow \ CCF\ risk \end{cases} \tag{4-22}$$

The flow chart of the CCF prediction approach is shown in Figure 4-17.

4.5 Case Study

To demonstrate the accuracy of the proposed CCF prediction method, a modified 6M2A model as shown in **Error! Reference source not found.** which is also used in Chapter 2 is simulated o n the RTDS.

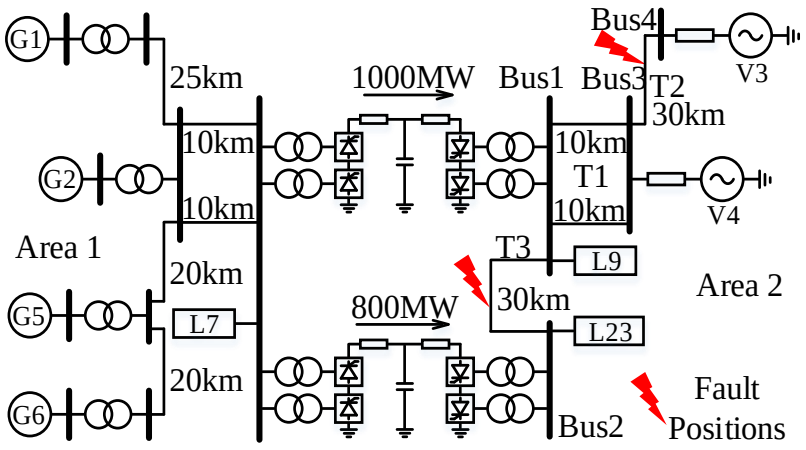


Figure 4-18 The Single-Line diagram of the test system

4.5.1 The synchronous generators at the inverter side in the original 6M2A model are replaced by the Thevenin Equivalent circuits [107]. The equivalent voltages of source V3 and V4 are 230kV∠-15° and 230kV∠-23° respectively, and their equivalent impedance is 1+j20 ohm. Other detailed parameters are listed in Table

2-2 in Chapter 2 and [107]. The control systems at the inverter side include CV, CC, and CEA control. The faults located on transmission lines T2 and T3 as highlighted in Error! Reference source not found. **are considered.Calculation of $\boldsymbol{AAADmax}$ and $\Delta\alpha_{max}$**

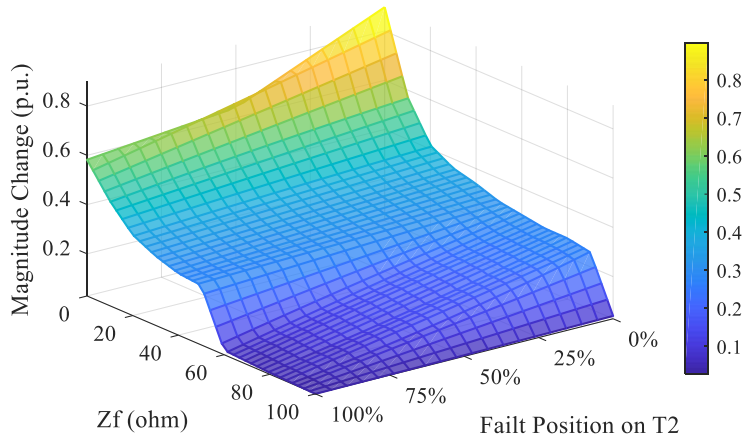
To predict CCFs, the above-mentioned $\Delta\alpha_{\max}$, the commutation voltages and $AAAD_{max}$ need to be calculated. This section will briefly present $\Delta\alpha_{\max}$ and commutation voltage calculations, and then mainly focus on the derivation of the $AAAD_{max}$.

Firstly, for the $\Delta\alpha_{\max}$, the settings of the $\gamma_{min}$and T_I are 7° and 0.0544s, respectively, in the above model. The maximum time duration t_{max} is set to 140ms. Thus, by applying (4-11), the maximum firing angle $\Delta\alpha_{max}$ can be calculated as 25 degrees.

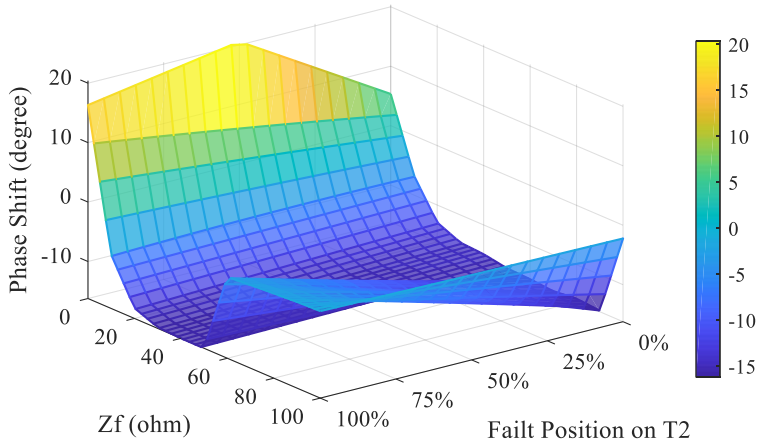
Secondly, the commutation voltages and their changes under faults can be calculated by applying the methods proposed in previous chapters which have been proved accurate. For instance, the calculation results of changes of the commutation voltage $\boldsymbol{E}_{AB}^{f}$ at the inverter bus 1 when faults occur on T2 are shown in Figure 4-19. The percentage shown in Figure 4-19 represents the location of the fault. For example, 25% T2 means the fault is located 25% of the T2 length away from Bus 3.

It can be concluded from Figure 4-19 that 1) With lower fault impedance, i.e., more severe fault, the voltage magnitude change becomes larger, and the phase shift keeps decreasing which means the phase keeps lagging; 2) When the fault is closer to the inverter, the voltage magnitude change also gets larger, and the phase shift becomes lower which means the phase is more lagging; 3) It needs to be noticed that once CFFs occur, the faulty-phase thyristor valve groups including upper arm and lower arm will get short-circuited, and thus the whole system gets unstable. This extreme fault scenario will not be analysed in this chapter since in this case

the inverter loses the characteristics of the current source. This chapter will focus on the critical CCF prediction.



(a). The magnitude changes of L-L commutation voltage $\Delta|\boldsymbol{E}_{AB1}|$ of inverter 1 during faults with varying fault impedance on transmission line T2

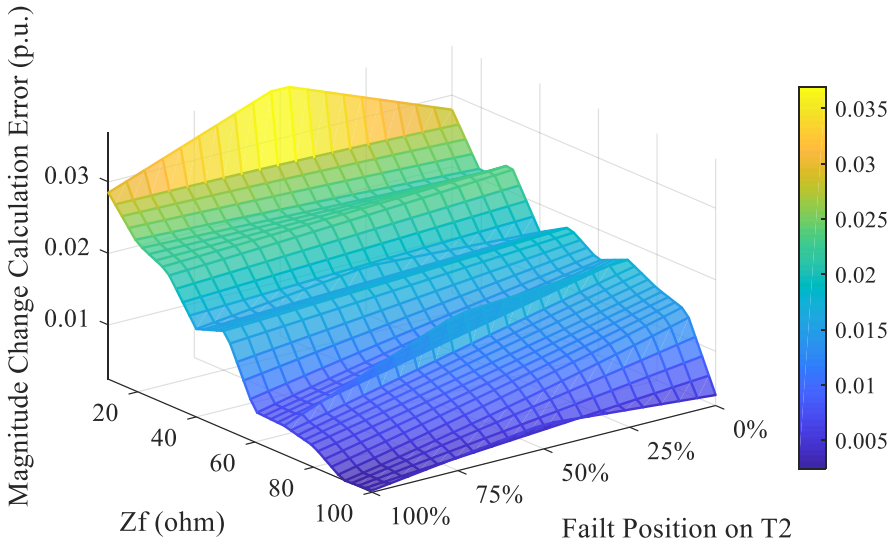


(b). The phase shifts of L-L commutation voltage $\Delta Ph.\boldsymbol{E}_{AB1}$ of inverter 1 during faults with varying fault impedance on transmission line T2

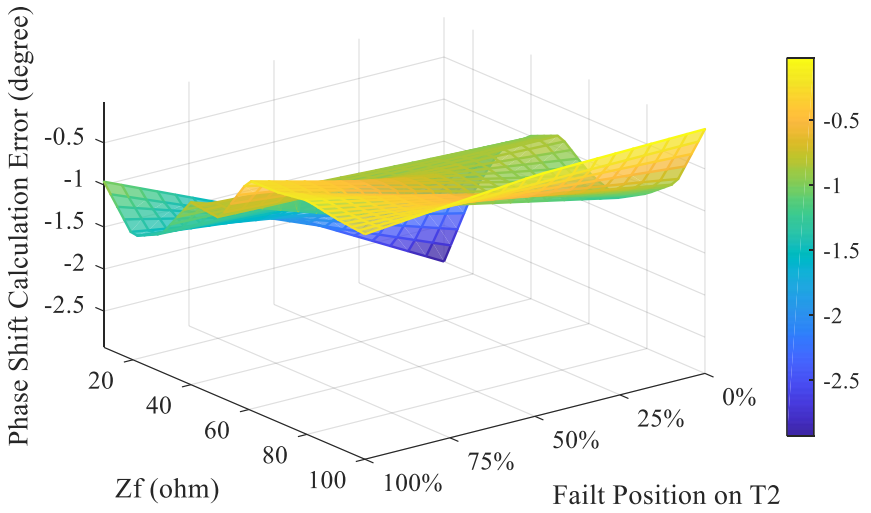
Figure 4-19 Magnitude changes and phase shifts of the L-L commutation voltage $\boldsymbol{E}_{AB1}$

It is worth noting that once FCF occurs, as shown in Figure 4-19 when Z_f is less than 60 ohms, the phase angle of the L-L commutation voltage lags by as many as 20 degrees. Under asymmetrical fault conditions, the imbalance of the phase shifts of the three L-L commutation

voltages will have a great impact on the commutation process, which is illustrated in Section 4.4.2.



(a). The error of the magnitude change $\Delta|\boldsymbol{E}_{AB1}|$ between calculation and simulation results



(b). The error of the phase shift $\Delta Ph.\boldsymbol{E}_{AB1}$ between calculation and simulation results

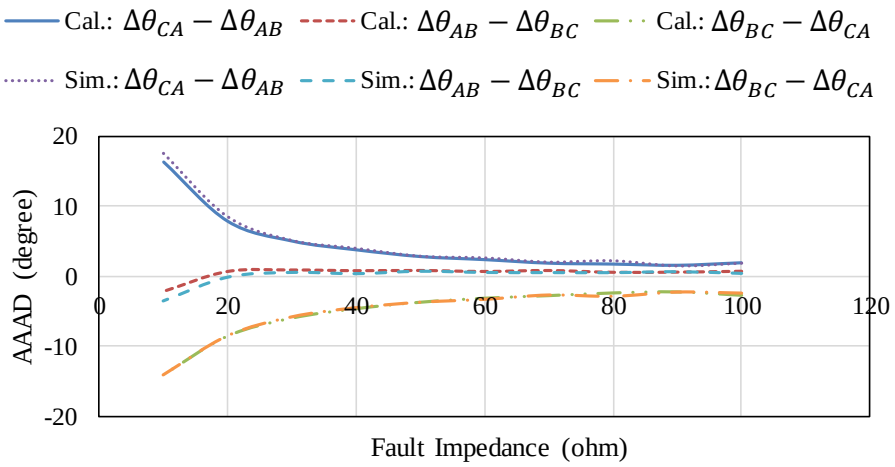
Figure 4-20 The error between calculation results and simulation results

To illustrate the accuracy of the calculation results, the error of the magnitude changes and the phase shifts between the calculation results and simulation results is shown in Figure 4-20.

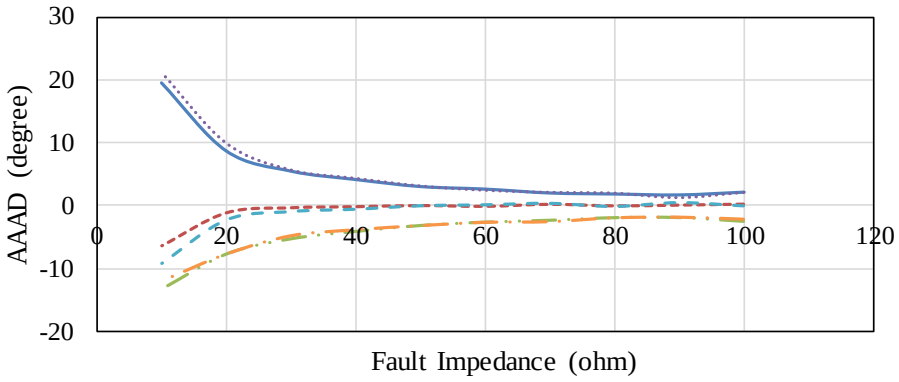
From Figure 4-20, it can be observed that 1) The error of the magnitude changes of the L-L commutation voltage between the calculation results and simulation results is less than 4%; 2) The error of the phase shifts of the L-L commutation voltage between the calculation results and simulation results is less than 3 degrees; 3) The error gets larger when the fault is more severe or closed to the inverter. The comparisons show that the calculation results are relatively accurate compared with simulation results.

Finally, the above commutation voltage calculations are used to derive $AAAD_{max}$. As one of the main reasons for CCFs under asymmetrical faults, $AAAD_{max}$ is not analysed in existing papers. Based on (4-19)(4-20), the $AAAD_{ij}$ and $AAAD_{max}$ can be calculated.

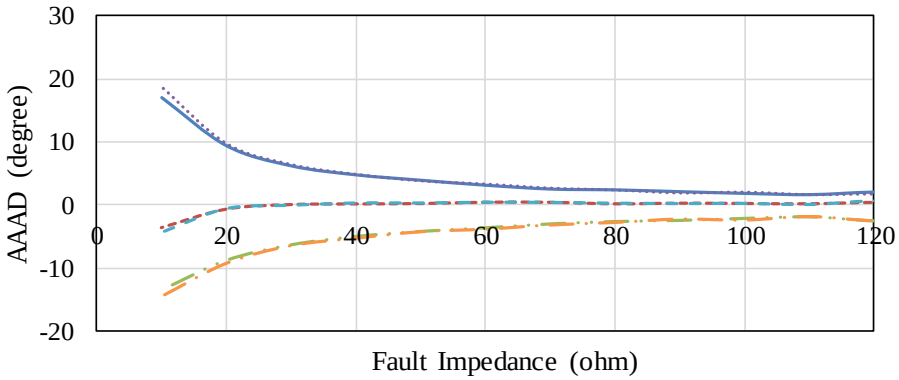
Figure 4-21 shows the three $AAADs$: $\Delta\theta_{CA}-\Delta\theta_{AB}$, $\Delta\theta_{BC}-\Delta\theta_{CA}$, and $\Delta\theta_{AB}-\Delta\theta_{BC}$ of inverter 1 and 2 under SLG faults occurring on T2 and T3, where $AAAD_{max}$ is the largest curve of three $AAAD$ curves.



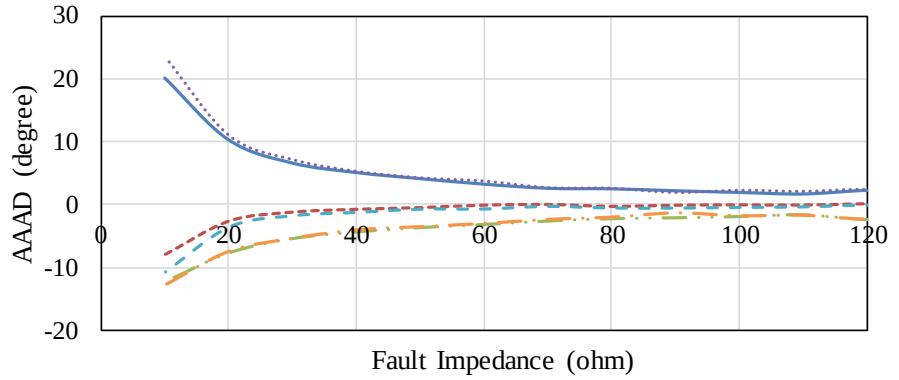
(a) AAADs of Inverter 1 when SLG faults occur on T2 0%



(b) AAADs of Inverter 2 when SLG faults occur on T2 0%



(c) AAADs of Inverter 1 when SLG faults occur on T3 0%



(d) AAADs of Inverter 2 when SLG faults occur on T3 0%

Figure 4-21 Comparisons of AAAD between proposed calculation method and simulation results

It can be concluded from Figure 4-21 that 1) Calculation results match the simulation results, and the maximum error is less than 1%; 2) When SLG faults occur, the *AAAD* for different

commutation processes varies from $-15°$ to $23°$; 3) With lower fault impedance, i.e., severer faults, the absolute values of $AAADs$ increase; 4) $AAAD_{max}$ indicates the curve that has the biggest values among the three $AAADs$ and it can reach 23 degrees when fault impedance drops to 10 ohms; 5) When $AAAD_{max}$ keeps increasing and compressing the margin of the extinction process, CCFs may occur based on (4-22).

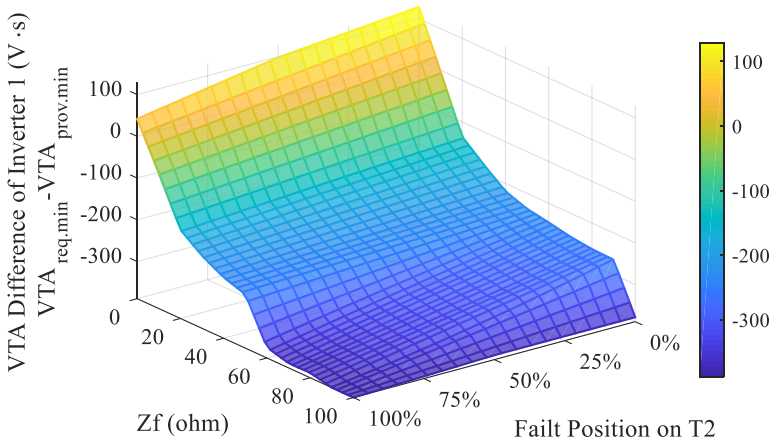
It is worth noticing that the $AAAD_{max}$ that can be as large as 23 degrees is not considered by any published papers. This reduction of the margin of the commutation can cause CCFs.

4.5.2 CCF Prediction

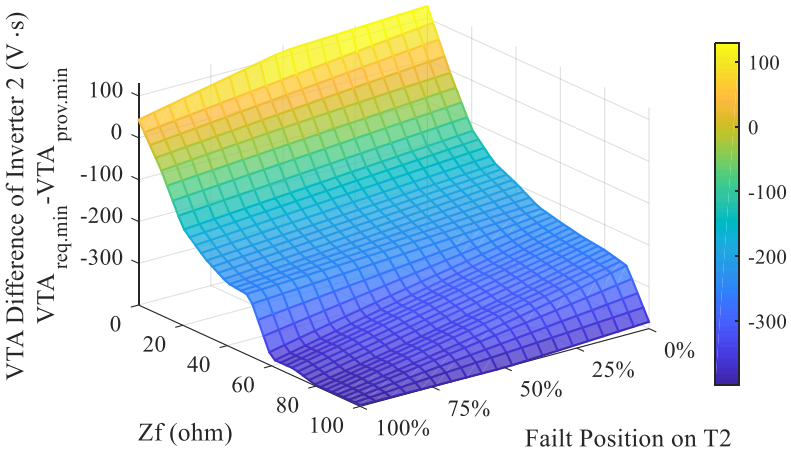
As explained in Section 4.4.2, the minimum VTA required by the inverter valve groups for successful commutations $VTA_{req.min}$ can be obtained in accordance with the minimum extinction angle γ_{min}.

Through calculating the minimum value of the maximum VTAs provided by the AC system $VTA_{prov.min}^{fault}$ in SLG fault cases by integrating the during-fault commutation voltages on the overlap angle, the CCF can be predicted by comparing $VTA_{prov.min}^{fault}$ and $VTA_{req.min}$.

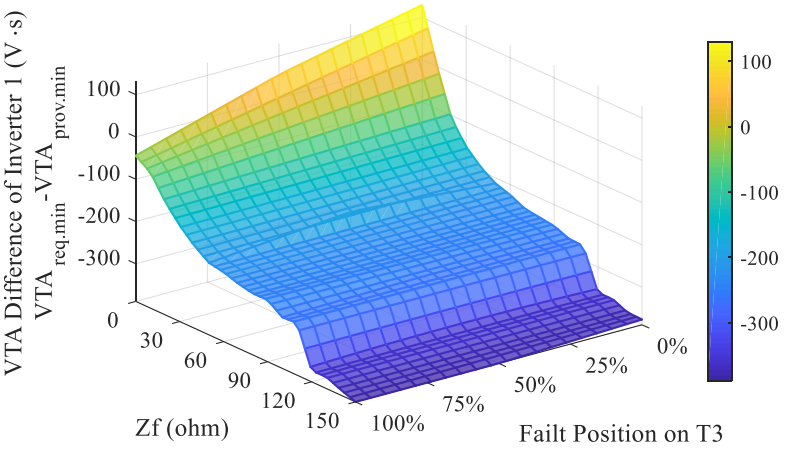
Based on the above calculation results including the L-L commutation voltages and overlap angles, the difference between $VTA_{prov.min}^{fault}$ and the minimum required VTA $VTA_{req.min}$ with different fault impedance and locations is shown in Figure 4-22.



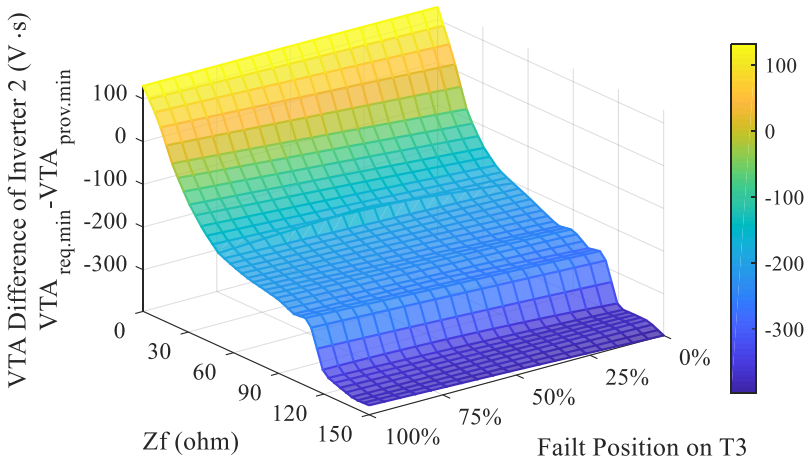
(a). The VTA difference of Inverter 1 with faults on T2



(b). The VTA difference of Inverter 2 with faults on T2



(c). The VTA difference of Inverter 1 with faults on T3



(d). The VTA difference of Inverter 2 with faults on T3

Figure 4-22 The VTA difference $VTA_{req.min} - VTA_{prov.min}^{fault}$

It can be viewed from Figure 4-22 that:

1) With lower fault impedance, i.e., more severe fault, the VTA difference becomes higher, which means the margin of the commutation process keeps being compressed;
2) When the fault is closer to the inverter, the VTA difference becomes higher, which means the margin of the commutation process is also being reduced;
3) When the VTA difference equals zero, i.e., $VTA_{prov.min}^{fault}$ equals $VTA_{req.min}$, the CCF is about to occur. Thus the fault impedance of the zero-crossing points of the curved surface and the flat surface $VTA_{prov.min}^{fault} - VTA_{req.min} = 0$ indicates the critical fault impedance for the CCF with the fault in different locations.

The comparison of the critical fault impedance for the CCF based on the proposed CCF prediction method, the simulation results, and the previous methods is shown in Table 4-2.

It can be seen from the comparison in Table 4-2 that the maximum error between the calculation and simulation results is less than 3 ohms (error accounts for 25% of the simulation result 12

ohms). This error is smaller than the maximum error between simulation results and previous methods (9 ohms, accounting for 75% of the simulation result 12 ohms) that do not consider the phase shift of all three phases and their impact on the commutation process under SLG faults. In this case, the proposed calculation method reduces the error by 67%.

Table 4-2 Comparison of the critical fault impedance for CCF

Critical Fault Impedance for CCF (Ohm)		Proposed CCF Prediction Method	Simulation Results	Previous Methods*
Fault Position	T2 0%	10	12	4
	T2 50%	8	10	3
	T2 100%	5	7	2
	T3 0%	13	12	3
	T3 50%	15	13	4
	T3 100%	15	12	3

*Previous methods: indicate the methods as shown in Section 1.2.2 which do not take into account the phase shift of all three phases and their impact on the commutation process under SLG faults when predicting CCFs.

The abovementioned 'impact' of the phase shifts on the commutation process under SLG faults in Table 4-2 indicates the impact of $AAAD_{max}$ which has been analysed in detail in Section 4.4.3.

In conclusion, 1) the proposed CCF prediction method considers the phase shifts and magnitude changes of not only the faulty phase but also the non-faulty phase commutation voltages; 2) The maximum asymmetrical advancing angle difference $AAAD_{max}$ quantifies the impact of the unbalanced commutation voltage changes on the commutation process: it can reduce the margin of the commutations by as many as 23 degrees; 3) The regulation of the

control systems could increase the margin of commutations by as many as 25 degrees; 4) The proposed CCF prediction method is more accurate than previous methods as it can reduce the error by 67%.

4.6 Discussions

4.6.1 CCF Elimination Approaches

It has been proved in Section 4.4 that CCFs will occur, once the minimum value of the six maximum VTAs provided by the AC system $VTA_{prov.min}^{fault}$ is smaller than the minimum required VTA for the valve groups $VTA_{req.min}$ during the faults. It can be concluded from Figure 4-22 and Table 4-2 that if the fault impedance is lower than the critical impedance, the VTA difference ($VTA_{req.min} - VTA_{prov.min}^{fault}$) will be positive, which means that the inverter needs a certain amount of VTA to achieve successful commutations.

As the most direct variable related to the commutation process, VTA is the integral of the commutation voltage within the overlap angle. Thus, three methods can be utilised to improve the VTA provided by the AC system $VTA_{prov.min}^{fault}$ during faults: 1) Improving the commutation voltage magnitudes by inserting additional devices to provide extra voltage; 2) Advancing the firing instant, i.e., reducing the firing angle, by set proper parameters for control systems; 3) Combining the above two methods.

It needs to be noticed that in some extreme fault cases, the phase shifts are too large that the ignition advance angle is smaller than zero, which means the commutation voltage has already reversed before the upcoming thyristor valve group is fired. In these circumstances, the increase of the commutation voltage magnitudes cannot eliminate CCF risks, unless the firing angle is

reduced at the same time to leave sufficient margin for the commutation and extinction processes.

4.6.2 Potential Applications

This chapter proposes a CCF prediction method by analysing the detailed commutation process considering the control systems. Once system parameters and fault details in LCC-HVDC systems in an area is available, the CCF occurrence can be forecasted for any LCC-HVDC inverters within this zone by utilizing the proposed CCF prediction method. Thus, it can be used to help the system operators identify the CCF risk areas under different faults.

As mentioned before, the proposed mathematical CCF prediction method can be applied to large-scale and complex power systems with LCC-HVDC links which is difficult to be simulated in RTDS and other simulators. Consequently, the effective, fast and accurate mathematical CCF prediction method can assist engineers in designing or upgrading the LCC-HVDC projects.

Besides, although the CCF prediction in this chapter is put forward mainly for describing the performance of the LCC-HVDC systems under asymmetrical faults, it can still be applied to symmetrical fault conditions. For example, since the phase shifts are balanced in Stages 3 as mentioned in Section 4.3 under symmetrical faults, the above analysis can still be applied, and the only difference is that AAAs become zero.

Moreover, when the proposed mathematical CCF prediction method is applied to LCC-HVDC projects, different values of T_I parameter of the control systems due to different manufacturers will affect the maximum adjustment $\Delta\alpha_{max}$ according to (4-10) - (4-11). If the value of T_I is unavailable, potential solution may be to estimate it by the relationships between the measurement values of the input and output signals of the control system, or comparing the

signals with that from another control system where T_I known.

4.7 Summary

This chapter proposes a more accurate and effective mathematical Continuous Commutation Failure (CCF) prediction approach for Multi-Infeed LCC-HVDC systems under asymmetrical faults by putting forward the Asymmetrical Advancing Angle Difference ($AAAD$) that considers the phase shifts and voltage changes of all commutation voltages, and the impact of the control system. The following conclusions can be made:

1) The CCF under asymmetrical faults is mainly caused by the maximum phase shift difference of the three L-L commutation voltages, named the maximum AAAD ($AAAD_{max}$), which reduces the commutation margin by 23 degrees in this chapter;
2) The impact of the regulation of the control systems is quantified, and in this chapter, the control systems can benefit the commutations by increasing the commutation margin by as many as 25 degrees;
3) Higher risks of CCFs will be brought to the two thyristor-valve arms within the same phase which are affected by $AAAD_{max}$; (e.g., T1-T3 & T4-T6 will suffer CCFs if the difference between phase shifts of V_{CA} and V_{AB} is the largest and V_{AB} is less lagging).
4) Based on the analysis and VTA theory, a CCF prediction method is proposed and demonstrated by comparing the calculation and simulation results through the 6M2A model running on RTDS. The proposed method can reduce the prediction error by 67% compared with the existing literature which does not consider $AAAD_{max}$ and magnitude changes and phase shifts of all commutation voltages under asymmetrical faults.

5) The work in this chapter helps researchers understand quantitatively the effect of the imbalance of the phase shifts on the commutation process under asymmetrical faults, and the proposed mathematical CCF prediction method can be used to fast and accurately predict CCFs in actual large-scale and complicated power systems which is essentially impossible to be simulated on RTDS due to the processors' limited computing capability.
6) The limitations that the voltage harmonics are not considered may affect the accuracy and effectiveness of the proposed CCF prediction method when applied to real projects, but can be limited to minimum level if measures are taken, e.g., installing filters to reduce harmonics.

CHAPTER 5 Immunity Index and Interaction Factor for Continuous Commutation Failure in LCC-HVDC Systems

5.1 Introduction

As mentioned before, the existing studies listed in Section 1.2.3 on the immunity and interaction of the inverters in Multi-Infeed LCC-HVDC systems merely focus on the voltage magnitude changes of the inverter buses under the three-phase symmetrical fault, but these studies cannot describe the performance of the interactions under asymmetrical faults. Moreover, the existing research mainly focuses on general CFs, and there exists a great deficiency in the estimation and evaluation of the Multi-Infeed LCC-HVDC systems under CCFs in asymmetrical fault cases.

Thus, by analysing the mechanism of CCFs under asymmetrical faults, this chapter proposes a new Immunity Index for CCF (IICCF), Interaction Factor for CCF (IFCCF), and the Critical IFCCF (CIFCCF), to accurately estimate the CF performance of a Multi-Infeed LCC-HVDC system under asymmetrical faults. IICCF aims to estimate and quantify the immunity of the inverter to CCFs. IFCCF is to quantify the level of interactions between two inverters in a Multi-Infeed LCC-HVDC system under asymmetrical faults. The CIFCCF, which can be calculated by IICCF, is used to identify CCF risks in an inverter when CCFs occur in its adjacent inverter, by being compared with IFCCF.

This Chapter is organised as follows: Section 5.2 introduces the topology of the Multi-Infeed

LCC-HVDC system. Section 5.3 presents the CCF prediction criterion under asymmetrical faults by analysing the impact of phase shifts and magnitude changes of all three phase commutation voltages on the commutation process, as well as the impact of the regulation of control systems. Section 5.4 proposes a new method to calculate the immunity index and the concept of IICCF. Then the interaction factor of the inverters in Multi-Infeed LCC-HVDC systems is re-defined and IFCCF is proposed in Section 5.5, and the Critical IFCCF is put forward to evaluate the interaction of the inverters on CCF risks. A case study is carried out in Section 5.6 by simulating the modified 4M2A model on RTDS. The possible applications of the proposed concepts are discussed in Section 5.7, and Section 5.8 gives the conclusion.

5.2 The Multi-Infeed LCC-HVDC Model

To study the immunity as well as the interaction between the inverters in the Multi-Infeed LCC-HVDC, the model as shown in Figure 5-1 is used in this chapter. In this system, the power ratings of the LCC-HVDC links can be set to different values to expand the application of this topology.

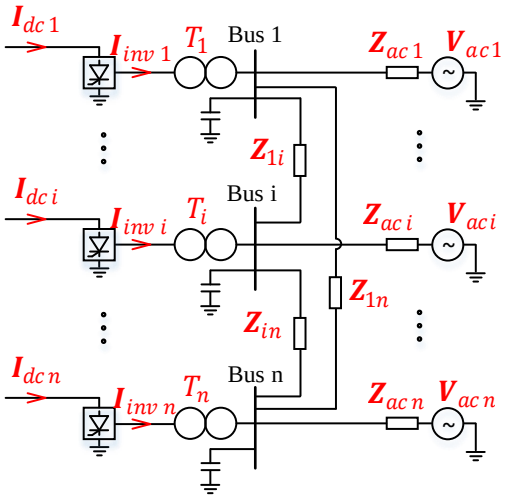


Figure 5-1 The simplified model of the Multi-Infeed LCC-HVDC system

The LCC-HVDC systems are under Constant Current (CC) control at the rectifier sides and Constant Voltage (CV) control, CC control, and Constant Extinction Angle (CEA) control at the inverter sides, which are commonly used in LCC-HVDC systems.

5.3 CCF Prediction

5.3.1 CCF Analysis

As mentioned in Section 1.2.2, CCF is the most serious type of CFs that can lead to inverter blocking, so it's important to predict the CCF for the inverters in power grids. NCCF indicates intermittent CFs after FCF and can be regarded as harmless to the system since the system can automatically recover from NCCFs.

This section briefly introduces the prediction criterion of the CCF under asymmetrical faults which has been explained in detail in Chapter 4.

Recall the detailed commutation process analysed in the last chapter when CCFs occur. Figure 5-2 shows the detailed commutation process of one inverter during the fault when a SLG fault occurs at the inverter-side AC system with detailed instants. It can be seen that:

1) The equivalent zero-crossing points for Phase-Locked Loop (PLL) firings under asymmetrical faults are shifted by $\Delta\theta_{PLL}$(lagging from ωt_0 to ωt_1 in Figure 5-2) during this cycle;
2) The firing angle α_f during fault (starting from ωt_1, ωt_5) is advanced by as large as $\Delta\alpha_{max}$ by the control systems compared with pre-fault firing angle α_0 (starting from ωt_0, ωt_3);
3) The Asymmetrical Advancing Angles (AAAs) between the firing instant and the zero-

crossing point of the real commutation voltage for the six commutation processes are different due to the unbalanced phase shifts and magnitude changes of the commutation voltages;

4) The extinction margin γ_{f4-6} for the commutation process $I_{T4} \rightarrow I_{T6}$ affected by the commutation voltage ($\boldsymbol{E}_{AB}^{f}$) with the minimum lagging phase shift (from $\omega t_3$to ωt_4) is severely compressed as shown in Figure 5-2.

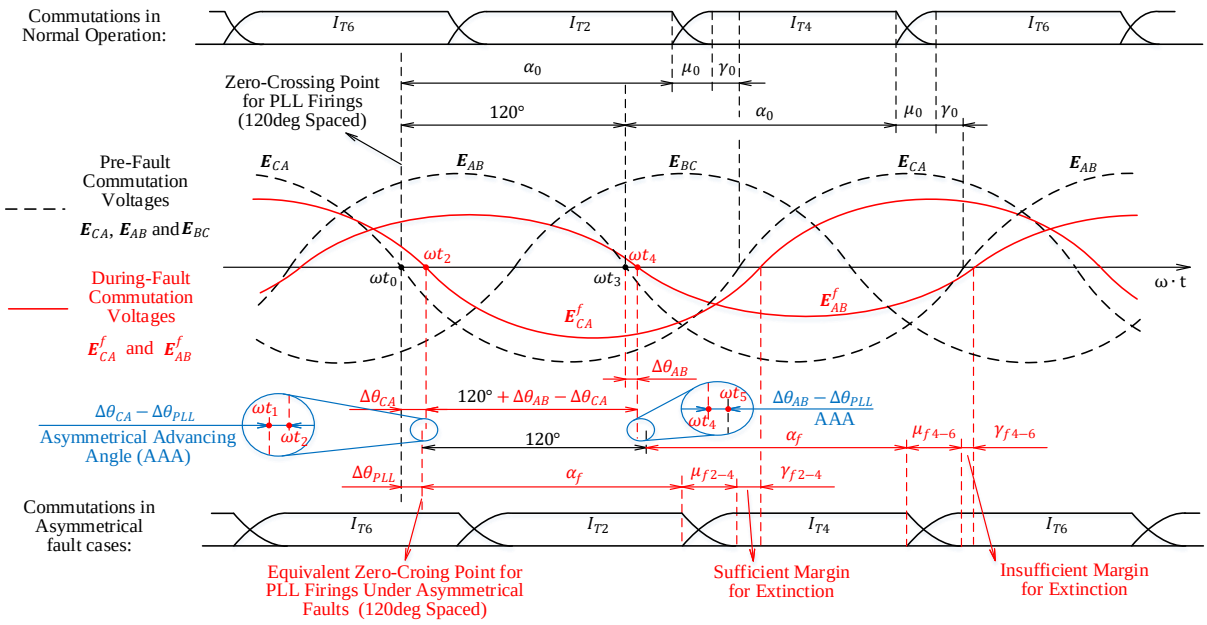


Figure 5-2 The pre-fault and during-fault commutation processes of $I_{T2} \rightarrow I_{T4}$ and $I_{T4} \rightarrow I_{T6}$under asymmetrical faults with detailed time instants

In conclusion, the commutation voltage with the maximum lagging phase shift and the following commutation voltage that has the minimum lagging phase shift will result in high risks of CCFs for the corresponding commutation process. For example, $\boldsymbol{E}_{CA}^{f}$ with the maximum lagging phase shift $\Delta\theta_{CA}$ and $\boldsymbol{E}_{AB}^{f}$ with the minimum lagging phase shift $\Delta\theta_{AB}$ will cause a large phase angle mismatch (named AAA, Asymmetrical Advancing Angle) between the equivalent zero-crossing point output by PLL for firing pulses (ωt_1, ωt_5) and the actual

zero-crossing point of the commutation voltage (ωt_2, ωt_4) under asymmetrical faults. This will significantly reduce the upcoming commutation margin ($\mu_{f4-6} + \gamma_{f4-6}$) and cause CCFs in $I_{T4} \rightarrow I_{T6}$ as well as $I_{T1} \rightarrow I_{T3}$.

However, previous research listed in Section 1.2.3 does not consider the phase shifts of all commutation voltages and the $AAAD$. This will bring large errors when predicting CCFs, which will be demonstrated in Section 5.4.

5.3.2 The Prediction Criterion

Based on the VTA theory and the above analysis, the maximum VTA provided by the AC system during asymmetrical faults can be expressed in (5-1).

$$VTA_{if.max} = \int_{\alpha_{f.min}-(\Delta\theta_i-\Delta\theta_{PLL})}^{180°-\alpha_{f.min}+(\Delta\theta_i-\Delta\theta_{PLL})-\gamma_{min}} V_{if}(t)dt \tag{5-1}$$

where $i = 1,2,\dots,6$ is the order of the six commutation processes during a cycle; $\Delta\theta_i$ is the phase shift of the commutation voltage of the i^{th} commutation process; V_{if} is the corresponding L-L commutation voltage of the i^{th} commutation process; $VTA_{if.max}$ indicates the maximum VTA provided by the AC system under the minimum firing angle order of the i^{th} commutation process in fault cases.

Due to the imbalance of the three L-L commutation voltages, the $VTA_{1f.max}$, $VTA_{2f.max}$, ..., $VTA_{6f.max}$ for the six commutation processes are different. CCFs would firstly occur in the thyristor valves which are provided with the minimum value $VTA_{prov.min}^{fault}$ by the AC system, as expressed in (5-2).

$$VTA_{prov.min}^{fault} = min\{VTA_{if.max}\}, \qquad i = 1,2,\dots 6 \tag{5-2}$$

Thus, the CCFs can be predicted by comparing the minimum VTA under asymmetrical faults and the minimum VTA required by the thyristor valves, as shown in (5-3).

$$\begin{cases} VTA_{prov.min}^{fault} \geq VTA_{req.min}, & \rightarrow \ No\ CCF\ risk \\ VTA_{prov.min}^{fault} < VTA_{req.min}, & \rightarrow \ CCF\ risk \end{cases} \tag{5-3}$$

5.4 Immunity Index for CCF

To accurately study the immunity of the inverter to CCFs, this section proposes a new immunity index (II) to quantify the immunity of a LCC-HVDC system to CCFs. This proposed index is applicable to both single LCC-HVDC and Multi-Infeed LCC-HVDC systems.

5.4.1 Immunity Index Based on VTA Theory

To quantify the inverters' immunity to any types of faults, the Immunity Index (II) is proposed as shown in (4):

$$II_i = \frac{VTA_{i-fault}}{VTA_{i-normal}} \tag{5-4}$$

where $VTA_{i-normal}$ and $VTA_{i-fault}$ are the voltage-time areas of the inverter i in normal operation and during faults, respectively.

It can be seen from (5-4) that the proposed II_i represents the level of VTA that the AC system can provide during the fault compared with the level of VTA that is needed for normal commutations.

By utilizing the critical VTA value as the numerator when a hazard (e.g., FCF, CCF, etc.) is about to occur, the II_i indicates the immunity of the inverter i to this type of faults which has risks of this specific hazard.

It needs to be highlighted that compared with previous research where the ratio of the fault capacity to the DC power is used [49] to represent the immunity of the inverter to the CFs, the proposed II_i can accurately evaluate the immunity by taking into account the direct factors causing CFs – the commutation voltages and the overlap angles.

5.4.2 Immunity Index for Continuous Commutation Failure

The II_i for CCF ($IICCF_i$) indicates the immunity of the inverter i to the faults which will cause CCFs, as expressed in (5-5).

$$IICCF_i = \frac{Critical\ VTA_{i-CCF}}{VTA_{i-normal}} = \frac{VTA_{i-req.min}}{VTA_{i-normal}} \tag{5-5}$$

where $Critical\ VTA_{CCF}$ is the VTA provided by the AC system to inverter i when CCFs are about to happen.

Since $IICCF_i$ is the ratio of VTA under the critical CCF fault condition to the VTA in the normal operation condition, it can reflect the immunity level of inverter i to the faults which will cause CCFs.

It needs to be noted that with lower $IICCF_i$, the $VTA_{i-normal}$ will be larger than $VTA_{i-req.min}$. This indicates that inverter i is operating more reliably and it provides the system with a larger margin to ride through the faults which may have CCF risks. Therefore, a smaller $IICCF_i$ represents the stronger immunity of inverter i to any faults which will cause CCFs.

Previous research on the Immunity Index to CFs (CFII) is defined as the percentage of the worst critical fault MVA out of the rated active power transmitted by the LCC-HVDC system, which only considers the voltage magnitude of the faulty phase under faults. However, the magnitude changes and phase angle shifts of the commutation voltages will significantly affect

the commutation process as illustrated in Section 5.3. The proposed $IICCF_i$ is more accurate than CFII since it considers the most direct factor influencing the commutation process, i.e., the commutation voltage and the overlap angle, in the form of the integration VTA to evaluate the immunity of the inverter to CCFs.

5.5 Interaction Factor for CCF in Multi-Infeed LCC-HVDC System

In Multi-Infeed LCC-HVDC systems, AC side faults may cause CCFs in the local inverter (the nearest inverter) and concurrent CCFs in the adjacent inverters. To research the relationships of CCF risks in two inverters in the Multi-Infeed LCC-HVDC systems when asymmetrical faults occur, a new interaction factor for CCF (IFCCF) is proposed in this section.

5.5.1 Interaction Factor in Multi-Infeed LCC-HVDC Systems

The model of the Multi-Infeed LCC-HVDC grid as shown in Figure 5-1 is used in this chapter to study the interaction between two inverters in a Multi-Infeed LCC-HVDC system when CCFs occur. Same as Chapter 4, the inverters are approximately regarded as current sources to simplify the analysis, and the mutual interactions between the three phases of each device (e.g., transmission line, inverter transformer, etc.) under asymmetrical faults are considered since the SC method could decouple the three phases, as explained in Section 3.2.

Since the phase angle change and the magnitude of each commutation voltage at each inverter bus (i.e., $\Delta\theta_i$ and $V_{if}(t)$, i=A,B,C,) can be calculated through the methods proposed in previous chapters, the critical VTAs required for the two adjacent inverters to avoid CCFs can be calculated through (5-1).

Then the relationship of the VTAs provided to the two adjacent inverters when CCFs are about

to occur in one of them can be used to represent the interactions between the two inverters. Here the per-unit values of the VTA changes are utilised to represent the interaction factor, as shown in (5-6).

$$\mathrm{IFCCF}_{ji} = \frac{\Delta VTA_{j-p.u.}}{Critical\ \Delta VTA_{i-CCFp.u.}} \tag{5-6}$$

where the $Critical\ \Delta VTA_{i-CCFp.u.}$ indicates the change of VTA in per-unit provided to inverter i when CCFs are about to occur in inverter i under a specific fault; $\Delta VTA_{j-p.u.}$ means the change of VTA of the inverter j in per-unit in the same fault case.

This interaction factor reflects the relationships between two inverters regarding CCF risks in a Multi-Infeed LCC-HVDC system by comparing the changes of VTAs which are directly associated with the commutation process.

It needs to be highlighted that previous research on the interaction factor of the Multi-Infeed LCC-HVDC system (MIIF) only considers the voltage change under symmetrical faults, and the denominator of the MIIF in previous research is 1% of the voltage magnitude as the voltage change. This makes it unable to directly illustrate and quantify the interaction of two inverters regarding CF risks under faults, especially in the case of estimating CCF risks, which will cause large error as demonstrated in Section 5.6 below.

5.5.2 The Interaction Evaluation Criterion

By applying the parameters of the system when CCFs are about to occur to (5-6), the Critical IFCCF (CIFCCF) can be obtained. Then it can be compared with IFCCF for studying the interaction between two inverters under faults when they are facing CCF risks.

The CIFCCF is defined as follows,

$$CIFCCF_{ji} = \frac{Critical\ \Delta VTA_{j-CCFp.u.}}{Critical\ \Delta VTA_{i-CCFp.u.}} \tag{5-7}$$

where $Critical\ \Delta VTA_{j-CCFp.u.}$ indicates the change of VTA of inverter *j* when the CCF critically appears on inverter *i*.

By applying (5-5) to (5-7), CIFCCF can also be expressed in (5-8).

$$CIFCCF_{ji} = \frac{1 - IICCF_j}{1 - IICCF_i} \tag{5-8}$$

where $IICCF_i$ and $IICCF_j$ are the $IICCF$ of the inverter i and inverter j, respectively.

Then the criterion for evaluating the interaction between two inverters in terms of CCF risks is shown in (5-9).

$$\begin{cases} IFCCF_{ji} \geq CIFCCF_{ji}, & \rightarrow strong\ interaction \\ IFCCF_{ji} < CIFCCF_{ji}, & \rightarrow weak\ interaction \end{cases} \tag{5-9}$$

If $IFCCF_{ji}$ is equal to or larger than $CIFCCF_{ji}$, it indicates that CCFs occurring in inverter *i* would lead to CCFs in inverter *j*. In this case, the inverter *j* and inverter *i* have a strong interaction.

On the other hand, if $IFCCF_{ji}$ is smaller than $CIFCCF_{ji}$, it implies that CCFs occurring in inverter *i* would not lead to CCF in inverter *j* unless the faults are so significantly severe that $\Delta VTA_{j-p.u.}$ reaches $Critical\ \Delta VTA_{j-CCFp.u.}$. In this case, the interaction between inverter *j* and *i* is weak.

The flow chart of the criterion for the interaction evaluation is shown in Figure 5-3.

It needs to be highlighted that previous studies on the criterion for evaluating the interaction of

two inverters when AC faults occur (e.g., MIIF) merely consider the magnitude changes of commutation voltages under symmetrical faults. This will consequently cause large errors, which can be avoided by the criterion (5-9) proposed in this chapter.

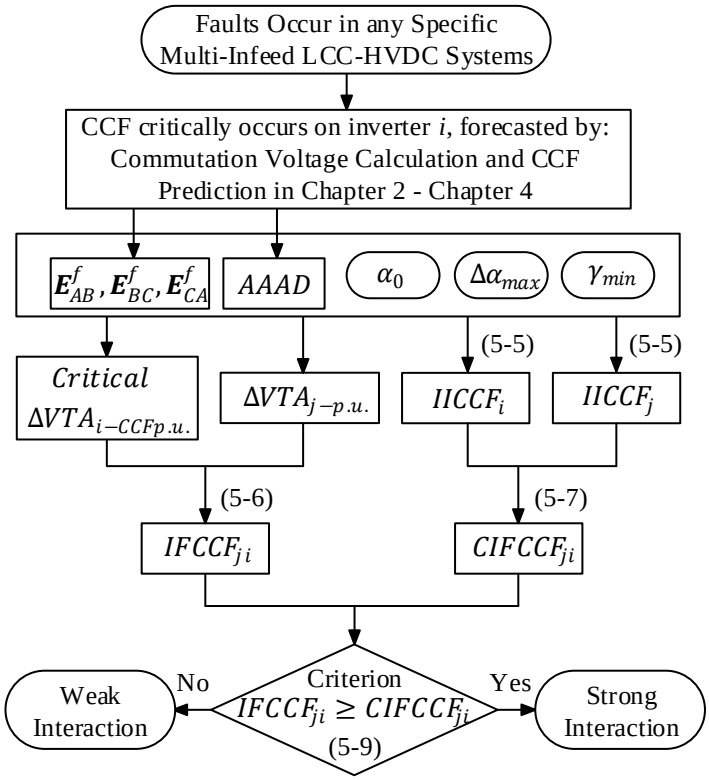


Figure 5-3 The flow chart of the interaction evaluation criterion process for Multi-Infeed LCC-HVDC Systems

5.6 Case Study

To demonstrate the accuracy of the proposed IICCF and IFCCF, the same 6M2A system as shown in **Error! Reference source not found.** is simulated on RTDS. The detailed parameters a re listed in Section 4.5. The SLG fault to be simulated is located on the transmission line T2 at inverter 1 side and on the transmission line T3 connecting bus 1 and bus 2. The control systems at the inverter side include CV, CC, and CEA control. While the control system at the rectifier side is CC control.

5.6.1 IICCF Analysis

This section shows the accuracy of the proposed IICCF under a SLG fault occurring at phase A on T2 and T3.

The extinction angle reference $15°$ and firing angle $143°$ in the normal operating condition are used to calculate VTA_{normal}. The $Critical\ VTA_{CCF}$ can be calculated by applying the minimum extinction angle of $7°$.

By substituting the above values to (5-1)(5-4) and (5-5), the $Critical\ VTA_{CCF}$, VTA_{normal} and IICCF can be calculated for the two inverters as shown in Table 5-1.

Table 5-1 IICCF of the two inverters in the 6M2A system

Inverter	$Critical\ VTA_{CCF}\ (V \cdot s)$	$VTA_{normal}\ (V \cdot s)$	IICCF
Inverter 1	125	178	0.70
Inverter 2	134	187	0.71

From Table 5-1, it can be seen that 1) for inverter 1, once the VTA provided by the AC system drops down below 0.7 p.u. under a fault, CCFs may occur in inverter 1; 2) in the meantime, when VTA provided to inverter 2 decreases and becomes less than 0.71 p.u. in fault cases, inverter 2 has CCF risks.

The IICCF presents a quantified index for the inverter in LCC-HVDC systems to evaluate its capability of riding through faults that may lead to CCFs. The lower the IICCF is, the inverter in normal operation condition is farther away from CCF risks which means the safety margin is relatively large. A lower IICCF can be achieved by a smaller AOI and will need higher reactive power due to the lower inverter AC side voltage.

5.6.2 IFCCF Application

In this section, the interaction between inverter 1 and inverter 2 when CCFs occur will be analysed to demonstrate the proposed interaction factor $IFCCF_{21}$.

The $\Delta VTA_{2-p.u.}$ of inverter 2 will be calculated under faults on different positions distributed on T2 and T3 which critically cause CCFs in inverter 1. The critical fault impedance of faults at different locations is shown in Table 5-1. In these cases, the ΔVTA of inverter 1 in per-unit can be regarded as the $Critical\ \Delta VTA_{1-CCFp.u.}$.

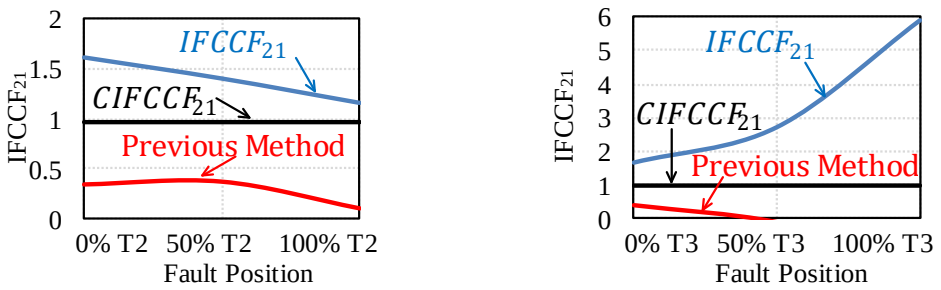
Based on the above values, the interaction factor between inverter 2 and inverter 1 $IFCCF_{21}$ can be expressed by (5-10).

$$IFCCF_{21} = \frac{\Delta VTA_{2-p.u.}}{Critical\ \Delta VTA_{1-CCFp.u.}} \tag{5-10}$$

And by applying Table 5-1 to (5-8), the $CIFCCF_{21}$ can be calculated by (5-11).

$$CIFCCF_{21} = \frac{1 - IICCF_2}{1 - IICCF_1} = 0.967 \tag{5-11}$$

Then the curves of $IFCCF_{21}$ can be plotted under faults at different positions in Figure 5-4, compared with the $CIFCCF_{21}$. The $IFCCF_{21}$ curves calculated by the previous method are also shown.



(a) When faults on T2 (b) When faults on T3

Figure 5-4 The $IFCCF_{21}$ with faults on different positions

where the 'Previous Method' indicates the calculation results of $IFCCF_{21}$ without taking into account the phase shifts of the non-faulty phase commutation voltages and AAADs in asymmetrical fault cases.

Based on the criterion (5-9), it can be seen from Figure 5-4 that the $IFCCF_{21}$ is always larger than $CIFCCF_{21}$ wherever the fault is located. The results indicate that: 1) Inverter 2 and inverter 1 are strongly coupled – any fault that causes CCFs in inverter 1 would result in CCFs in inverter 2, and such a CCF prediction has been proved by the simulation results as shown in Table 5-2; 2) When the fault location is within the inverter 1 AC side and closer to inverter 1 (from 100% of T2 to 0% of T2), the interaction of the two inverters gets stronger. This is because that the voltage reduction on Bus 1 is faster than Bus 2 since Bus 1 is more closer to the fault point, which can be derived from (2-55) - (2-60), and thus results in the change $IFCCF_{21}$ of with different fault locations on T2 according to (5-10); 3) When the fault location is on the transmission line T3 and closer to inverter 2, i.e., from 100% of T3 to 0% of T3 (from inverter 2 bus to inverter 1 bus), the interaction of the two inverters will also get stronger. The reason is that when a fault is far away from Inverter 1, the impedance between Bus 1 and the fault position will maintain the Bus 1 voltage at a certain value rather than zero, and thus Bus 1 voltage can provide a certain amount of VTA to Inverter 1 which consequently reduce $IFCCF_{21}$ according to (5-10); 4) The calculation results of $IFCCF_{21}$ by the previous method that did not consider the phase shifts and magnitude changes of all three phase commutation voltages as shown in Section 1.2.3 are lower than $CIFCCF_{21}$, which means that the faults leading to critical CCFs on inverter 1 will not cause CCFs on inverter 2. This is proved incorrect by the simulation results as shown in Table 5-2. This further demonstrates the importance of phase shifts and AAADs when evaluating the interaction of the inverters under asymmetrical faults with CCF risks.

Table 5-2 Simulation results of CCF on inverter 2 when CCFs are about to occur on inverter 1

Simulation results of Occurrence of CCFs	T2			T3		
	0%	50%	100%	0%	50%	100%
Inverter 1	Critical CCF*	Critical CCF	Critical CCF	Critical CCF	Critical CCF	Critical CCF
CCFs on Inverter 2?	CCF	CCF	CCF	CCF	CCF	CCF

*Critical CCF: CCFs are about to occur on inverter 1 when AC faults take place.

For instance, when a fault located at 100% of T2 is about to cause CCFs in inverter 1, the simulation results of the commutation process and the extinction angle measurements of the two inverters are shown in **Error! Reference source not found.**.

Error! Reference source not found. presents the valve currents and the extinction angle m easurement values of inverter 1 and inverter 2, respectively, when CCFs occur under asymmetrical faults. It can be seen that 1) The fault located at 100% of T2 results in CCFs in inverter 1; 2) CCFs also occur in inverter 2 during this fault; 3) The commutation processes keep failing in both inverters. This is because when CCFs occur in Inverter 1, the VTA provided by the AC system to Inverter 2 is smaller than the minimum VTA required by its valve groups to maintain successful commutations. The simulation results match well with the evaluation and prediction results as shown in Table 5-2. However, $IFCCF_{21}$ obtained by the previous method which does not consider the phase shifts and magnitude changes of three phase commutation voltages is smaller than $CIFCCF_{21}$, which means no CCFs will be predicted in Inverter 2 when there are CCFs in Inverter 1 according to (5-9), which is proved incorrect by the simulation results. Thus, it proves that the proposed criterion as shown in (5-9) is more accurate than the previous method.

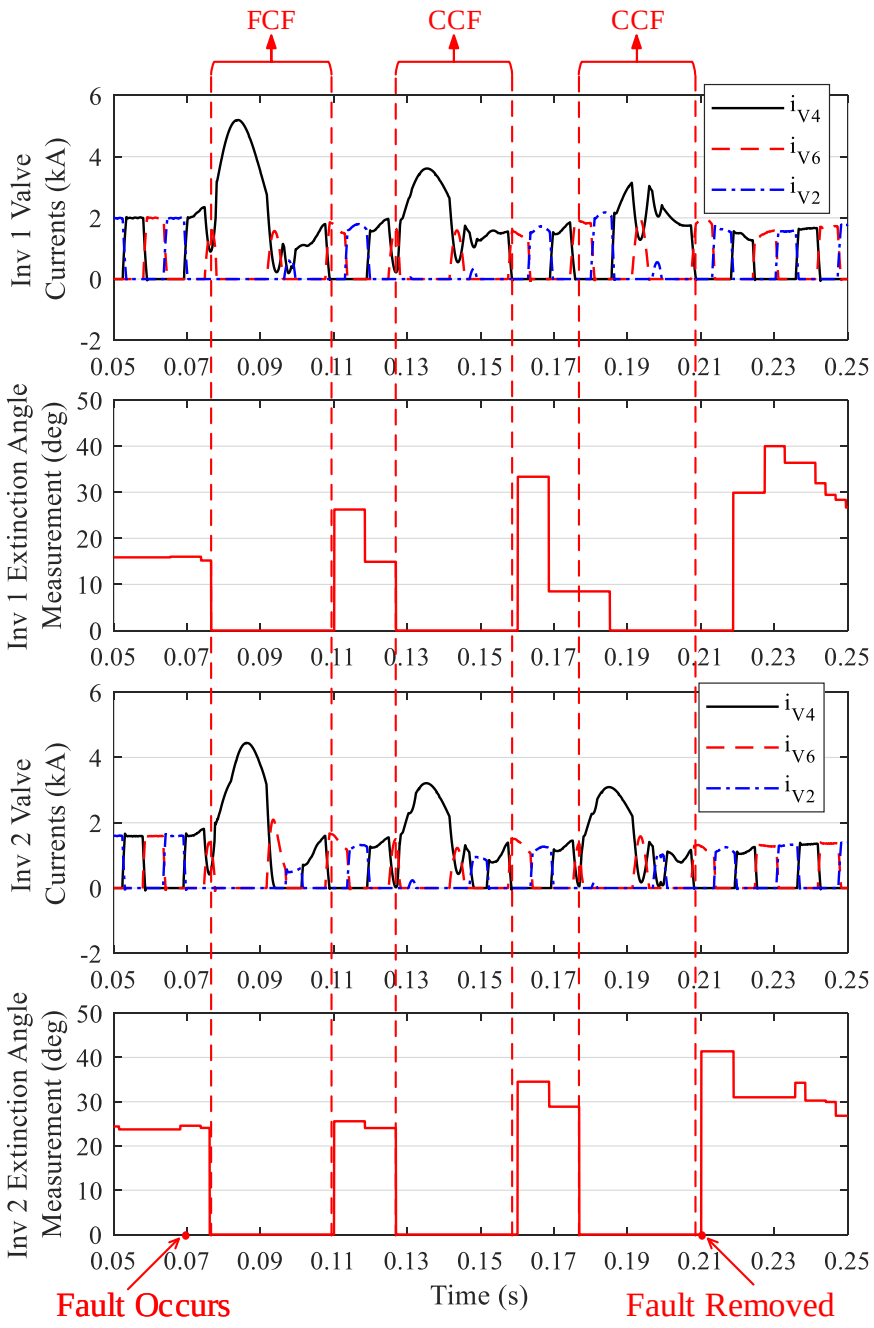


Figure 5-5 Simulation results of the commutation process when CCFs critically occur in Inverter 1.

In conclusion, the interaction between two adjacent inverters (inverter 1 and inverter 2) in Multi-Infeed LCC-HVDC systems in any fault cases can be calculated by comparing $IFCCF_{21}$ with $Critical\ IFCCF_{21}$. The $Critical\ IFCCF_{21}$ can be obtained by the Immunity Index of the two inverters ($IICCF_1$ and $IICCF_2$) which take into account the phase angle shifts and AAADs.

The simulation results demonstrate that the interaction calculation in terms of CCFs proposed in this chapter is accurate, and ignoring the phase shifts and AAADs will result in huge error in evaluating the interaction of the inverters for faults with CCF risks under asymmetrical fault conditions. Considering the proposed method can mathematically estimate the interactions between the inverters under faults with CCF risks and predict CCFs, it can be applied to large-scale and complicated power grids which is difficult to be simulated on RTDS, to help the system operators identify CCF risk areas online.

5.7 Discussions

This section discusses the practical applications of IICCF and IFCCF.

The immunity index IICCF can quantify the immunity of the LCC-HVDC inverter to the faults that may cause CCFs. Lower IICCF means the inverter has a larger margin to ride through the faults. Theoretically, the lower IICCF is, the better performance the system will have in riding through faults. However, a larger margin will bring more costs from the economic perspective, for example, a smaller AOI can result in a larger margin but will require more reactive power compensators. This accurate index, IICCF proposed in this chapter, can quantitatively evaluate the safety margin (from the value of IICCF to 1) of avoiding CCFs for the inverters. It enables power system operators to find out the balance between a proper safety margin and economy when designing new LCC-HVDC projects or upgrading existing ones, by setting specific IICCF values.

The interaction factor IFCCF can accurately quantify the interaction among inverters when they face AC faults that can cause CCFs. By comparing with Critical IFCCF, it can estimate CCF risks on one inverter when CCFs occur in the adjacent inverters. IFCCF higher than 1

means that CCFs will occur in an inverter when CCFs occur in its adjacent inverter. Thus, the criterion can be utilised to identify the CCF risk areas in large-scale power systems. For instance, to reduce the concurrent CCFs in a certain area of a Multi-Infeed LCC-HVDC system, avoiding IFCCF values larger than 1 among inverters within this area may achieve fewer concurrent CCFs.

Although the above concepts are proposed mainly for describing the performance of the LCC-HVDC systems under SLG faults, they may also be applied to other asymmetrical and symmetrical fault conditions by changing the fault circuit part shown in red in Figure A-1 to the corresponding fault circuit under a specified type of faults.

5.8 Summary

By analysing the mechanism of CCFs under asymmetrical faults, this chapter proposes an immunity index for CCF (IICCF) based on the VTA theory to quantify the immunity of an inverter to any type of faults, considering not only the magnitude changes but also the phase shifts of the commutation voltages. This index considers the most severe type of CFs (CCFs) and the most frequent AC faults (asymmetrical faults) and is derived from the variables (voltage and extinction angle) which are directly related to the commutation process. Then an interaction factor for CCF ($IFCCF_{ji}$) that can quantify the interaction of two inverters in Multi-Infeed LCC-HVDC systems under faults with CCF risks is proposed. This factor can accurately predict CCFs in an inverter when CCFs occur in adjacent inverters under asymmetrical faults in Multi-Infeed LCC-HVDC systems. Thus, the two indices can be utilised to quantify the safety margin of the inverters of avoiding CCF risks and identify the CCF risk areas in large-scale power systems.

Since the voltage harmonics are not considered in the proposition of the two indices, the accuracy can be further increased if measures are taken, e.g., installing filters to reduce harmonics, when applied to real projects.

Finally, the accuracy and validity of the proposed factors are demonstrated by sufficient simulations using the RTDS-based EMT simulation program based on the 6M2A system. Considering the limited computing capability of RTDS of simulating large-scale system, the proposed mathematical indices can be applied to large-size and complicated power grids to predict CCFs. They can assist power system operators to make decisions on the $IFCCF_{ji}$ value to achieve a proper safety margin and economy when designing new LCC-HVDC projects or upgrading existing ones.

CHAPTER 6 An Improved PLL Topology to Mitigate Commutation Failures for LCC-HVDC Systems under Asymmetrical Faults

6.1 Introduction

As mentioned in Section 1.2.4, in most studies about CF mitigation, the output of PLL is assumed to be unchanged. But in fact, it will change in fault cases. Only a few studies consider the change of the PLL output, however, the impact of unbalanced commutation voltages and the impact of Point on Wave (POW) on PLL output are not considered.

Therefore, this chapter firstly carries out the theoretical analysis of the impacts of the unbalanced inputs, i.e., the commutation voltages, and the impact of Point on Wave (POW) on the PLL output. Then an improved PLL topology is proposed to eliminate the adverse impact of the phase angle delay of PLL output caused by asymmetrical faults and then mitigate CFs. Finally, the feasibility and effectiveness of the proposed PLL topology are verified by a case study by using the CIGRE LCC-HVDC Benchmark simulated on RTDS and a comparison with the CFPREV control system.

The structure of this chapter is as below: Section 6.2 presents the relationship between the PLL output and the phase angle shifts of the commutation voltages. Section 6.3 depicts the impact of POW of faults on the PLL output, and the improved PLL topology is described in Section 6.4. Section 6.5 shows case studies, Section 6.6 gives a discussion, and Section 6.7 presents the summary.

6.2 Impact of Phase Angle Shift on PLL Output

Figure 6-1 depicts the block diagram of the PLL commonly used in HVDC control systems [112][113]. The inputs of the PLL are the three phase commutation voltages $\boldsymbol{E}_{\mathrm{A}}$, $\boldsymbol{E}_{\mathrm{B}}$, and $\boldsymbol{E}_{\mathrm{C}}$. Its output θ_{PLL} is a saw-tooth waveform.

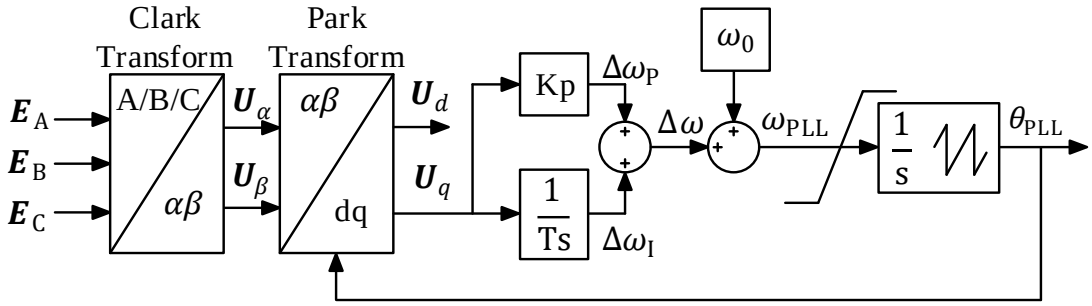


Figure 6-1 The block diagram of the PLL

The equivalent voltages $\boldsymbol{U}_{\alpha}$, $\boldsymbol{U}_{\beta}$, and $\boldsymbol{U}_{q}$ can be calculated through the Clark and Park Transforms:

$$\boldsymbol{U}_{\alpha} = \frac{2}{3} \cdot \boldsymbol{E}_{A} - \frac{1}{3} \cdot \boldsymbol{E}_{B} - \frac{1}{3} \cdot \boldsymbol{E}_{C} \tag{6-1}$$

$$\boldsymbol{U}_{\beta} = \frac{\sqrt{3}}{3} \cdot \boldsymbol{E}_{B} - \frac{\sqrt{3}}{3} \cdot \boldsymbol{E}_{C} \tag{6-2}$$

$$\boldsymbol{U}_{q} = \cos\theta_{\mathrm{PLL}} \cdot \boldsymbol{U}_{\alpha} + \sin\theta_{\mathrm{PLL}} \cdot \boldsymbol{U}_{\beta} \tag{6-3}$$

where $\boldsymbol{U}_{\alpha}$, $\boldsymbol{U}_{\beta}$, $\boldsymbol{U}_{d}$ and $\boldsymbol{U}_{q}$ are the equivalent α, β, d and q axis voltages of the commutation voltages $\boldsymbol{E}_{\mathrm{A}}$, $\boldsymbol{E}_{\mathrm{B}}$, and $\boldsymbol{E}_{\mathrm{C}}$, respectively.

Applying (6-1) (6-2) to (6-3), $\boldsymbol{U}_{q}$ can be described as:

$$\boldsymbol{U}_{q} = \cos\theta_{\mathrm{PLL}} \cdot (\frac{2}{3} \cdot \boldsymbol{U}_{A} - \frac{1}{3} \cdot \boldsymbol{U}_{B} - \frac{1}{3} \cdot \boldsymbol{U}_{C}) + \sin\theta_{\mathrm{PLL}} \cdot (\frac{\sqrt{3}}{3} \cdot \boldsymbol{U}_{B} - \frac{\sqrt{3}}{3} \cdot \boldsymbol{U}_{C}) \tag{6-4}$$

From (6-4), it can be seen that the equivalent q-axis voltage $\boldsymbol{U}_q$ is directly determined by the three phase commutation voltages. In the normal operation condition, system parameters are balanced and $\boldsymbol{U}_q$ equals zero. However, under unbalanced status, phase angle shifts of the commutation voltages will bring large error to the calculation result of $\boldsymbol{U}_q$, and it can be predicted that $\boldsymbol{U}_q$ will vary when the phase angle shifts of the commutation voltages change.

As illustrated in Chapter 2 - Chapter 5, it has been found that all phase angles and magnitudes of the three phase commutation voltages will change under SLG faults. To simplify the following analysis, only the faulty-phase commutation voltage change is considered, as shown below.

$$\boldsymbol{U}_A = \mathrm{U_{Am}} \cdot \sin(\omega t) \tag{6-5}$$

$$\boldsymbol{U}'_A = \mathrm{U'_{Am}} \cdot \sin(\omega t - \Delta\theta_\mathrm{A}) = (\mathrm{U_{Am}} - \Delta\mathrm{U_{Am}}) \cdot \sin(\omega t - \Delta\theta_\mathrm{A}) \tag{6-6}$$

$$\Delta\boldsymbol{U}_A = \boldsymbol{U}_A - \boldsymbol{U}'_A \tag{6-7}$$

where $\boldsymbol{U}_A$ and $\boldsymbol{U}'_A$ are the pre-fault and during-fault phase-A commutation voltage, respectively; $\mathrm{U_{Am}}$ and $\Delta\mathrm{U_{Am}}$ are the magnitudes of $\boldsymbol{U}_A$ and $\boldsymbol{U}'_A$, respectively; ω is the frequency of the system; $\Delta\mathrm{U_{Am}}$ and $\Delta\theta_\mathrm{A}$ are the changes of the magnitude (decreasing) and the phase angles (lagging) of the phase A commutation voltage, respectively; $\Delta\boldsymbol{U}_A$ is the change of $\boldsymbol{U}_A$ during the SLG fault.

Thus, under the phase-A SLG fault, $\boldsymbol{U}_A$ becomes $\boldsymbol{U}'_A$, and $\boldsymbol{U}'_q$ can be expressed as below:

$$\boldsymbol{U}'_q = \cos\theta_\mathrm{PLL} \cdot \left(\frac{2}{3} \cdot \boldsymbol{U}'_A - \frac{1}{3} \cdot \boldsymbol{U}_B - \frac{1}{3} \cdot \boldsymbol{U}_C\right) + \sin\theta_\mathrm{PLL} \cdot \left(\frac{\sqrt{3}}{3} \cdot \boldsymbol{U}_B - \frac{\sqrt{3}}{3} \cdot \boldsymbol{U}_C\right) \tag{6-8}$$

Then the change of $\boldsymbol{U}_q$ can be expressed:

$$\Delta \boldsymbol{U}_q = \boldsymbol{U}'_q - \boldsymbol{U}_q = \cos\theta_{\mathrm{PLL}} \cdot \frac{2}{3} \cdot (\boldsymbol{U}'_A - \boldsymbol{U}_A) = \frac{2}{3} \cdot \cos\theta_{\mathrm{PLL}} \cdot \Delta \boldsymbol{U}_A \tag{6-9}$$

where $\boldsymbol{U}'_q$ and $\Delta \boldsymbol{U}_q$ are the q-axis voltages of the phase A inverter bus and the change of it during the SLG fault.

It needs to be noticed that the angular frequency of both θ_{PLL} and $\Delta \boldsymbol{U}_A$ is ω according to (6-5) - (6-7), and thus the angular frequency of $\Delta \boldsymbol{U}_q$ is two times of , i.e., 2ω, based on its expression in (6-9) and the prosthaphaeresis algorithm.

From the PLL logic in Figure 6-1, the change of the sum of the proportion and integration of $\boldsymbol{U}_q$ can be calculated:

$$\Delta\omega = \mathrm{K_P} \cdot \Delta \boldsymbol{U}_q + \frac{1}{\mathrm{T_I}} \cdot \int_0^t \Delta \boldsymbol{U}_q dt \tag{6-10}$$

where $\mathrm{K_P}$ and $\mathrm{T_I}$ are the coefficient of the proportion part and the time constant of the integration part of the PI controller in PLL, respectively.

Thus the change of the PLL output $\Delta\theta_{\mathrm{PLL}}$ can be expressed as:

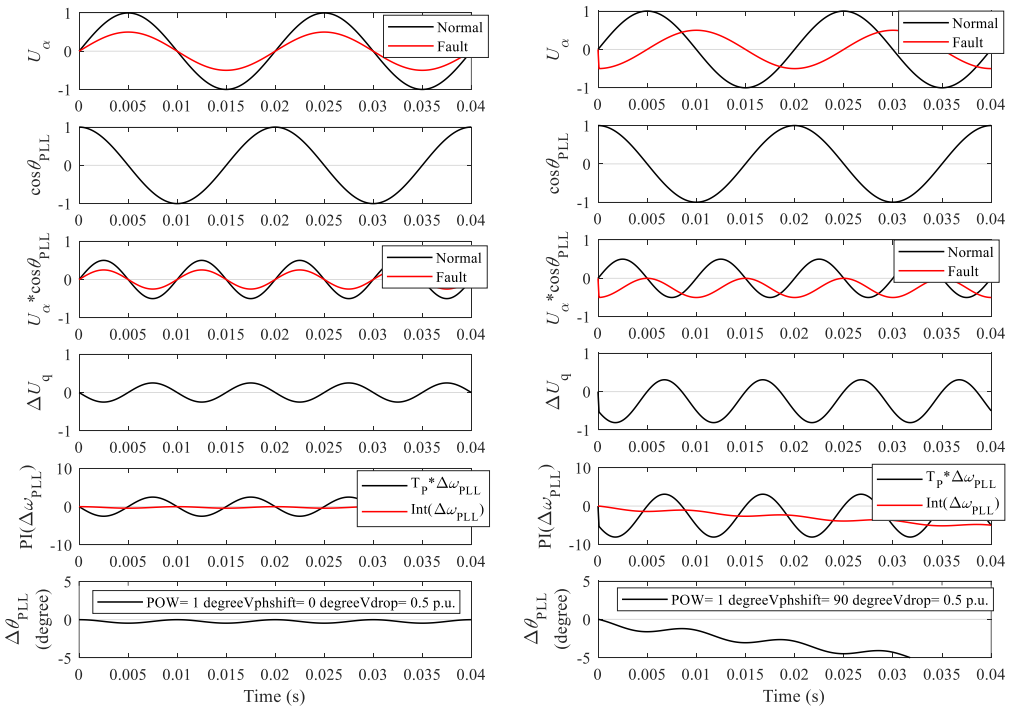
$$\Delta\theta_{\mathrm{PLL}} = \int_0^t \Delta\omega dt = \int_0^t \left[\mathrm{K_P} \cdot \Delta \boldsymbol{U}_q + \frac{1}{\mathrm{T_I}} \cdot \int_0^t \Delta \boldsymbol{U}_q dt \right] dt \tag{6-11}$$

It can be seen from (6-11) that:(1) $\Delta\theta_{\mathrm{PLL}}$ will be non-zero and keep changing when $\Delta \boldsymbol{U}_q$ is a non-zero value; (2) $\Delta\theta_{\mathrm{PLL}}$ is periodic with an angular frequency of 2ω, the same as $\Delta \boldsymbol{U}_q$.

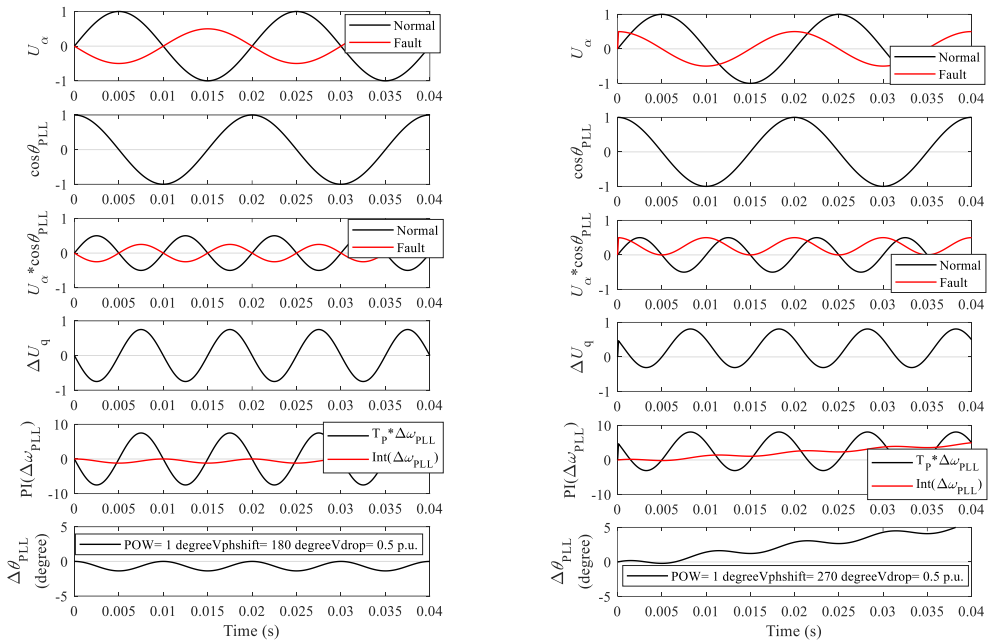
This means the firing pulses generated by the crossing points of the PLL output and the AOI signal would also vary even if the AOI remains unchanged.

Figure 6-2 (a)-(d) shows waveforms of the variables in PLL under SLG faults with different

faulty-phase angle shifts: 0, $\frac{\pi}{2}$, π, and $\frac{3\pi}{2}$ rad. It can be seen that with different phase angle shifts of the faulty-phase commutation voltage, the output of the PLL θ_{PLL} perform differently: θ_{PLL} will remain near zero when the phase angle shift (lagging) equals 0, π, 2π, … rad, but will keep decreasing and increasing when the phase angle shift (lagging) is between 0 to π rad and between π to 2π rad, respectively, as shown in Table 6-1. The reason for the different performances of θ_{PLL} with different phase angles of phase-A voltage is that the value of $\Delta \boldsymbol{U}_q$ affected by the phase-A voltage phase angle will determine the change of θ_{PLL}. For instance, when the phase angle of phase-A voltage is lagging as shown in Figure 6-2 (b), the average value of the sinewave $\Delta \boldsymbol{U}_q$ is negative and then leads to negative average values of the results of the proportion part as well as the integration part, which will finally result in the reduction of θ_{PLL}, i.e., lagging phase angle of the PLL output.



(a) Phase angle of phase-A voltage is zero (b) Phase angle of phase-A voltage is $\frac{\pi}{2}$ rad lagging



(c) Phase angle of phase-A voltage is π rad lagging (d) Phase angle of phase-A voltage is $\frac{3\pi}{2}$ rad lagging

Figure 6-2 The variables in PLL under phase-A SLG faults with different faulty-phase angle shifts

Table 6-1 The Impact of phase angle shift on PLL output and commutation process under SLG faults

Phase angle shift $\Delta\theta_A$ (rad)	$\Delta\theta_{PLL}$	θ_{PLL}	Final Impact on Commutation Process
$(0,\pi)$	Negative	Lagging	Adverse
$(\pi,2\pi)$	Positive	Leading	Beneficial
…	…	…	…

From Figure 6-2, it can be concluded that the phase angle shift $\Delta\theta_{\mathrm{A}}$ of the faulty phase commutation voltage will influence the PLL output θ_{PLL}, and then further affect the commutation process. When $\Delta\theta_{\mathrm{A}}$ is between 0 and π, the PLL output becomes lagging and thus brings an adverse impact on the commutation process. However, when $\Delta\theta_{\mathrm{A}}$ is between π and 2π, the PLL output becomes leading and then benefits the commutation process.

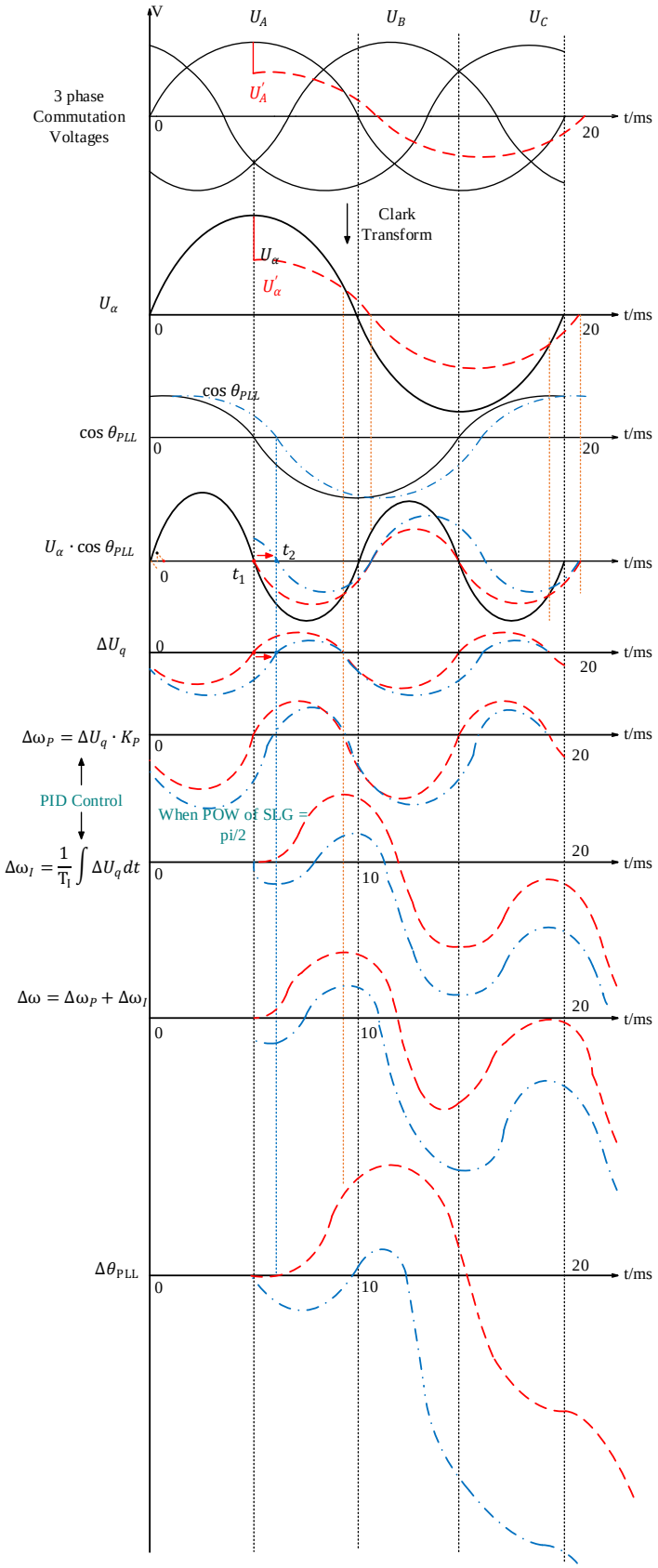


Figure 6-3 The variables in PLL when phase angle shift is $\frac{\pi}{9}$ under a phase-A SLG fault

It needs to be highlighted that in the first several cycles, when the changing θ_{PLL} feeds back to the Clark transform, the change of PLL output $\Delta\theta_{\mathrm{PLL}}$ will become larger. For instance, Figure 6-3 shows the variables in PLL when the phase angle shift of the faulty-phase commutation voltage is $\frac{\pi}{9}$ rad lagging under a SLG fault. The black solid lines are pre-fault values, while the red dashed lines are the curves under the SLG fault.

It can be seen from Figure 6-3 that the lagging PLL output will make the PLL output more lagging, as shown in dot-slashed waveforms (in blue). Conclusions can be made that:

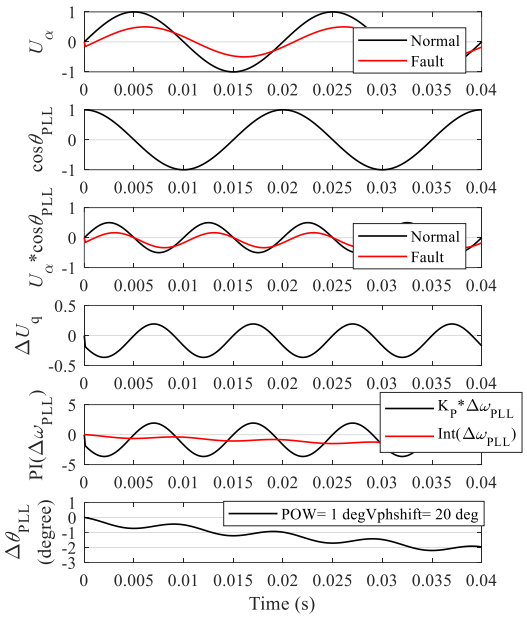
1) The PLL output will be either advanced or delayed in the first several cycles with the same faulty phase angle shift;
2) When $\Delta\theta_{\mathrm{PLL}}$ is larger than zero, it will benefit the commutation process, but when $\Delta\theta_{\mathrm{PLL}}$ is smaller than zero, it brings an adverse impact on the commutations.

6.3 Impact of POW on PLL Output

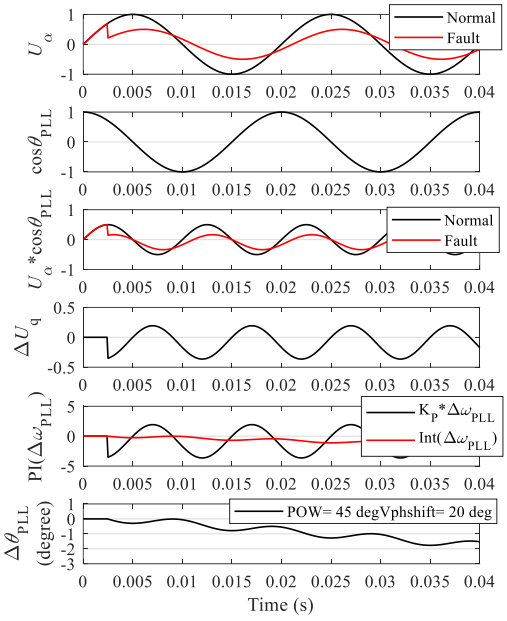
Based on the detailed analysis of the phase angle shifts of the commutation voltages in Chapter 4, the phase angle of the faulty-phase commutation voltage is always lagging, and the shift is within the range of (0, π) rad under SLG fault. This means that the output of the PLL will keep decreasing, as illustrated in Figure 6-2 (b).

To investigate the impact of POW on PLL output, the above-mentioned scenario is used where the phase shift angle is 20 degrees lagging. By recalling Figure 6-3, it can be concluded that the periodic ΔU_{q} which is oscillating around zero will have a significant impact on the value of $\Delta\theta_{\mathrm{PLL}}$ due to the integration part in the PLL loop. This means that faults with the POW in a certain range may lead to positive $\Delta\theta_{\mathrm{PLL}}$ which is beneficial to the commutation process, while

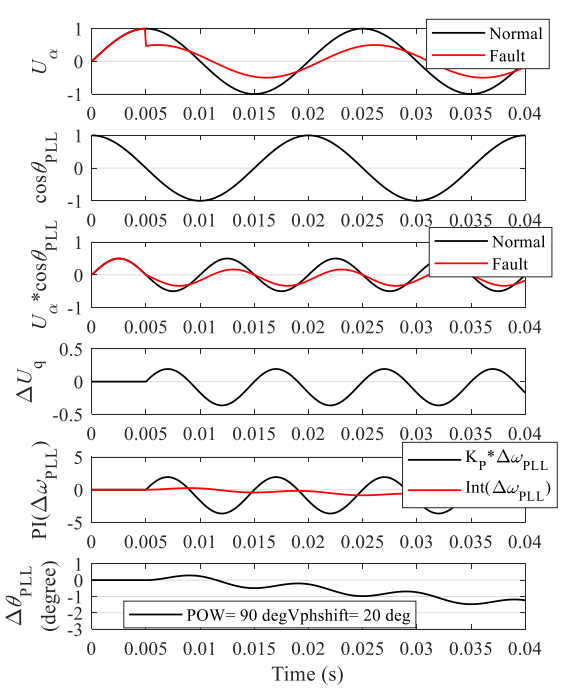
faults with the POW in a different range will lead to negative $\Delta\theta_{\mathrm{PLL}}$ which is detrimental to the commutations. Detailed $\Delta\theta_{\mathrm{PLL}}$ waveforms with different POWs are shown below.



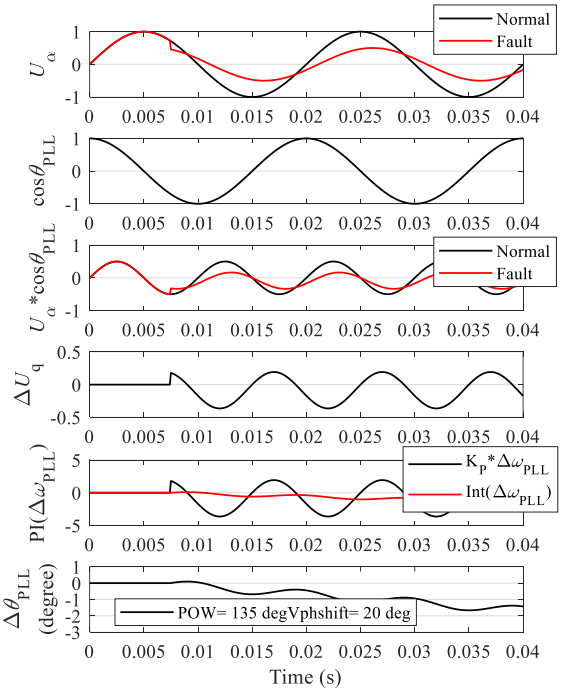
(a) POW=1 deg



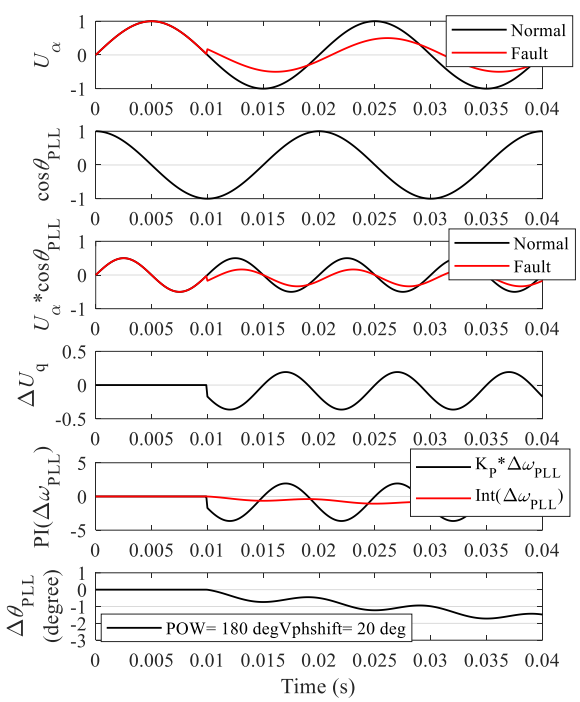
(b) POW=45 deg



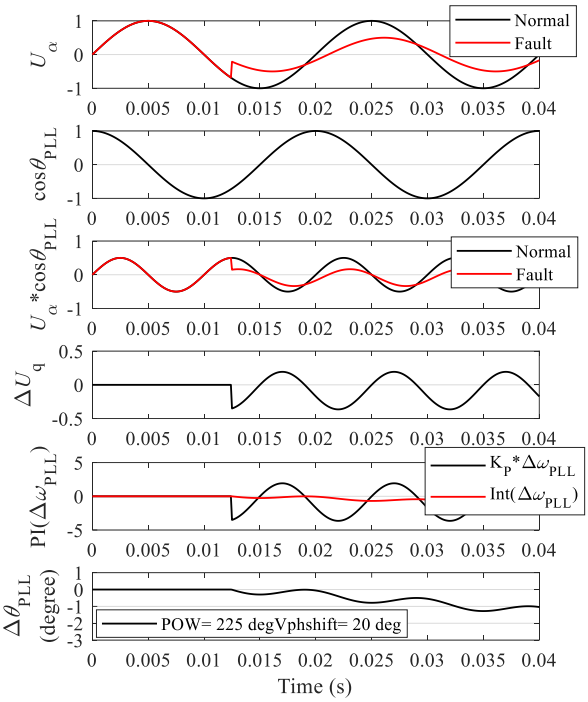
(c) POW=90 deg



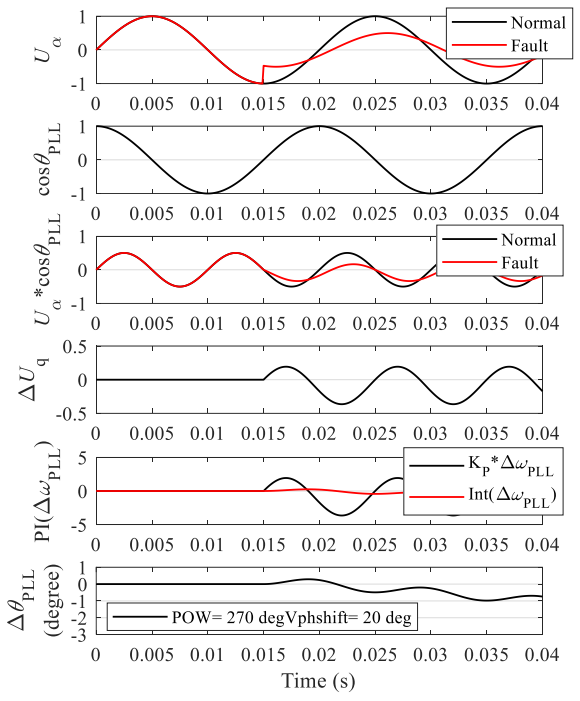
(d) POW=135 deg



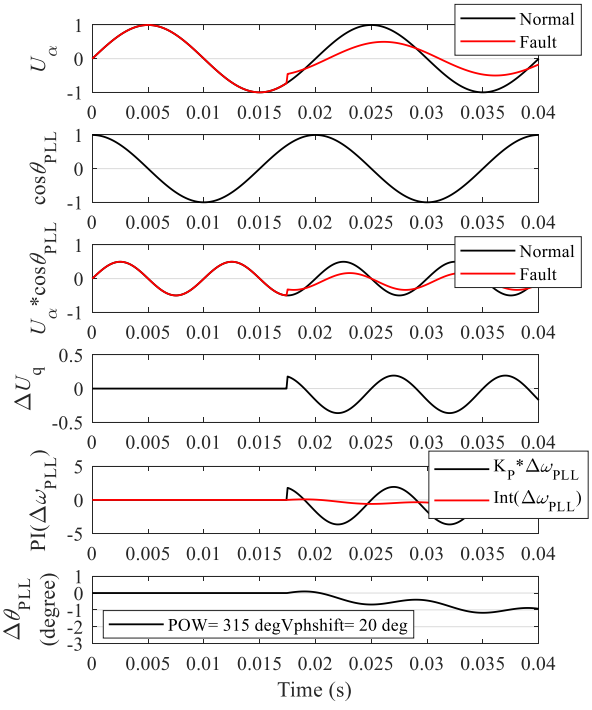
(e) POW=180 deg



(f) POW=225 deg



(g) POW=270 deg



(h) POW=315 deg

Figure 6-4 Variable Values of PLL under SLG faults with different POW

It can be seen from Figure 6-4 that, under the fault with different POW, the change of the PLL output $\Delta\theta_{\mathrm{PLL}}$ differs from positive to negative within the first cycle. Detailed variation is listed in Table 6-2.

Table 6-2 Values of the change of the PLL output $\Delta\theta_{\mathrm{PLL}}$ under SLG faults with different POW

Fault	$\Delta\theta_{PLL}$ (leading deg)				Fault	$\Delta\theta_{PLL}$ (leading deg)			
POW (deg)	0.005s after fault	0.01s after fault	0.015s after fault	0.02s after fault	POW (deg)	0.005s after fault	0.01s after fault	0.015s after fault	0.02s after fault
1	-0.7	-0.5	-1.2	-1	180	-0.7	-0.5	-1.2	-1
45	0	-0.5	-0.5	-1	225	0	-0.5	-0.5	-1
90	0.3	-0.5	-0.3	-1	270	0.3	-0.5	-0.3	-1
135	-0.5	-0.5	-1	-1	315	-0.5	-0.5	-1	-1

It can be seen from Table 6-2 that (1) The $\Delta\theta_{\mathrm{PLL}}$ is periodic with a cycle of 180 degrees, which is half of the cycle of the commutation voltages, as analysed in Section 6.2; (2) The POW will affect the value of the $\Delta\theta_{\mathrm{PLL}}$ but will not change its trend; (3) The $\Delta\theta_{\mathrm{PLL}}$ becomes positive 0.005s (90 degrees) after faults when the POW is 90+180*N degrees (N is integer), and during this period, the change of PLL output is beneficial to the commutation process but will have an adverse effect on commutations afterwards since the PLL output starts to lag.

The reason why the $\Delta\theta_{\mathrm{PLL}}$ is oscillating after faults is that the POW of the fault determines the value of ΔU_{q}, and then further affect $\Delta\theta_{\mathrm{PLL}}$ through the PI controller, which will decide the changing trend of the PLL output. For instance, if ΔU_{q} is positive when a fault occurs, the $\Delta\theta_{\mathrm{PLL}}$ will become positive which will benefit the commutation process. On the other hand, if ΔU_{q} is negative when a fault happens, $\Delta\theta_{\mathrm{PLL}}$ will turn negative and then adversely influence the

commutation process.

It needs to be pointed out that the phase angles between the output of the proportion part $\Delta\omega_P$ and the output of the integration part $\Delta\omega_I$ is around 90 degrees, which means their sum $\Delta\omega$ will change with varying coefficient K_P and time constant T_I, as shown in Figure 6-1 and Figure 6-3. As a result, $\Delta\theta_{PLL}$ is also affected by K_P and T_I. But for a specific LCC-HVDC system, K_P and T_I are pre-set values, and thus will not have impact on $\Delta\theta_{PLL}$ and commutations.

6.4 An Improved PLL Topology for Mitigating CFs

Based on the analysis of the impact of POW on the PLL output and the commutation process in the above sections, it can be concluded that although PLL output can benefit the commutation process, most of the time it will bring adverse impacts on the commutation process. Therefore, to eliminate the adverse impact of PLL on commutations and mitigate CFs under asymmetrical faults, an improved PLL topology is proposed as shown in Figure 6-5.

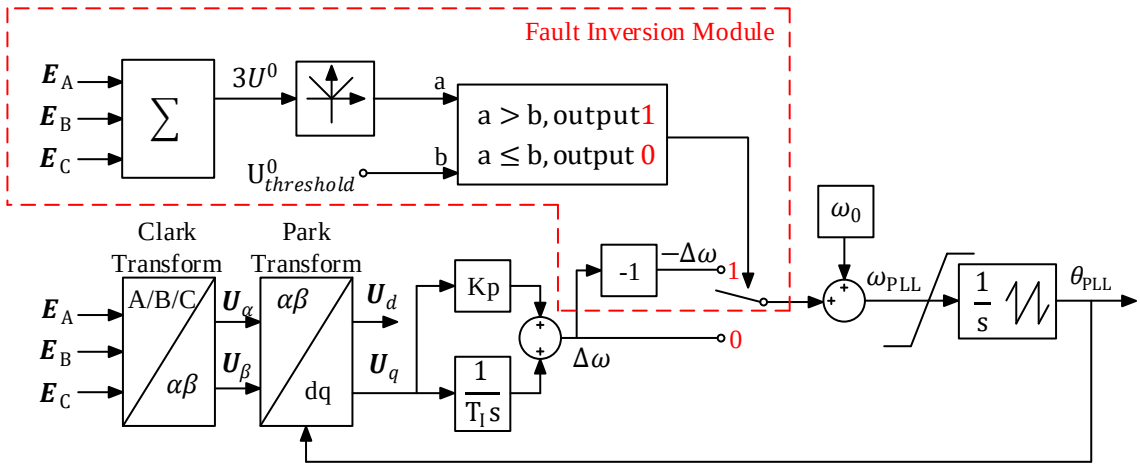


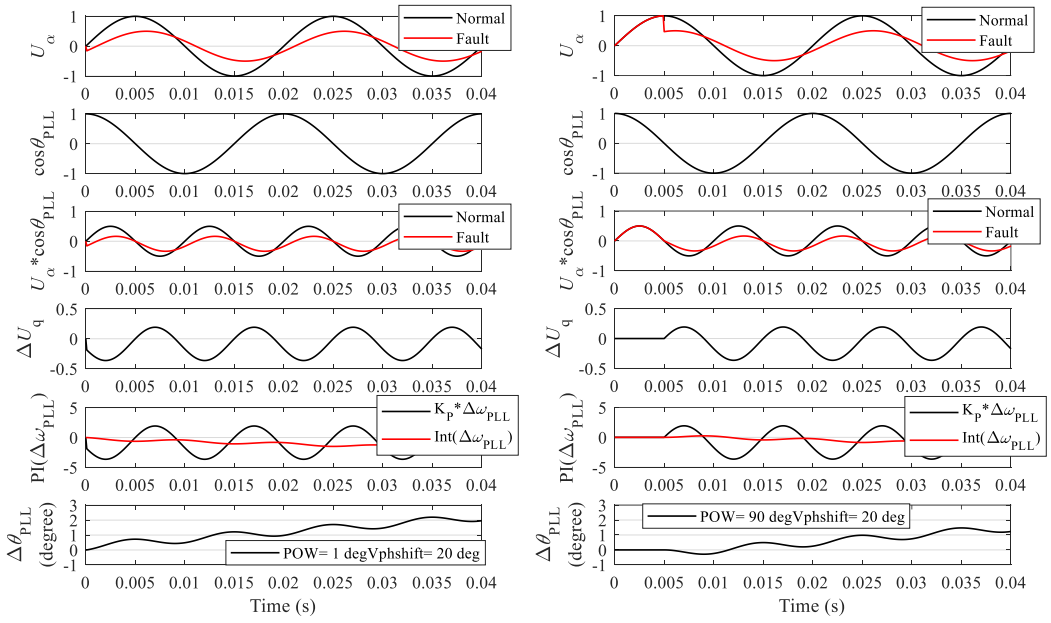
Figure 6-5 The proposed PLL topology

It can be seen from Figure 6-5 that the proposed PLL contains a 'Fault Inversion Module' (FIM) that is inserted into the conventional PLL which is shown in Figure 6-1. The FIM is utilised to

generate a trigger pulse to change the variables in PLL when it detects a certain change of the zero sequence component of the commutation voltages under asymmetrical faults.

The mechanism of this FIM-PLL to eliminate the impact of the PLL output on the commutation process is that when an asymmetrical fault occurs and the sum of bus voltages drops below the pre-set threshold value $U^0_{threshold}$, the FIM will reverse $\Delta\omega$ to achieve the goal of reversing the changing trend of the PLL output θ_{PLL} from negative to positive, as shown in Figure 6-6.

Here, the value of the threshold $U^0_{threshold}$ is determined by the critical fault scenario where two CFs occur in the inverter. A lower threshold value will limit the effectiveness of the proposed PLL in mitigating CFs, while a higher one will not contribute to suppressing CFs when FCF occurs. This threshold value can be calculated from past fault records or simulation results.



(a) POW=1 deg (b) POW=90 deg

Figure 6-6 Variable values of the proposed FIM-PLL under SLG faults with different POW

It needs to be noticed that although the FIM reversed the positive $\Delta\theta_{\mathrm{PLL}}$ to negative when POW equals 90 deg as shown in Figure 6-3 which means this will bring an adverse impact on commutations as shown in Figure 6-6 (b), it still makes sense since this process will only last 90 degrees (5ms) and the lagging phase angle shift is very low – no more than 1 deg at t=0.009s.

Since the output of the proposed FIM-PLL has a positive changing trend, the sawtooth waveforms will become leading, and the crossing point of the saw-tooth waveforms and AOI will be advanced. This will also advance the firing instants for the valve groups under faults and further increase the margin of the commutation and extinction process.

Figure 6-7 shows the FIM-PLL output, the conventional PLL output, and the AOI signal before and during the SLG fault. It can be seen that under the SLG fault, the output of the proposed FIM-PLL is leading the pre-fault output by $\Delta\theta_{\mathrm{PLL}}$, which will accelerate the firing instants and then benefit the commutation process. However, the conventional PLL output is lagging by $\Delta\theta_{\mathrm{PLL}}$ which is detrimental to the commutations.

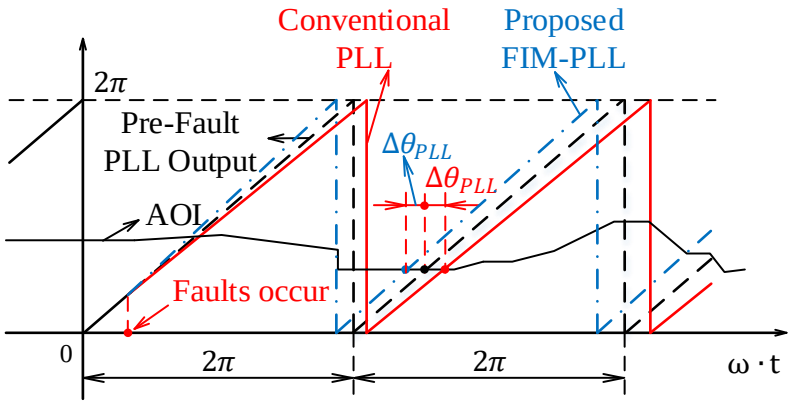


Figure 6-7 The outputs of the proposed FIM-PLL, the conventional PLL and AOI under A-phase SLG fault

It needs to be highlighted that the change of the phase angle shift of FIM-PLL is caused by the reversal of the change of angular frequency $\Delta\omega$, which results in the positive $\Delta\theta_{\mathrm{PLL}}$. Positive phase angle change $\Delta\theta_{\mathrm{PLL}}$ can advance the PLL output and then leave a larger extinction margin

for successful commutations.

As one of the most commonly used CF-suppression schemes, the CFPREV control system aims to prevent CFs by reducing the firing angles sharply once it detects that the commutation voltage is smaller than the threshold value. However, the sharp decrease in the firing angle will cause a surge in the reactive power demand and a large decrease in the commutation voltages. On the contrary, based on Figure 6-7, the proposed FIM-PLL requires less reactive power demand surge and causes smaller fluctuations in the commutation voltages.

6.5 Case Study

To verify the feasibility of the proposed FIM-PLL topology, the modified CIGRE LCC-HVDC Benchmark model as shown in Figure 2-1 is used for the case study. The detailed parameters are listed in presented in Section 1.2.1.

6.5.1 Verification of the Impact of POW on Commutation Process

Firstly, to find out the impact of POW on commutations and verify the above conclusions in Section 6.3, Phase-A SLG faults in the middle of the transmission line at the inverter side with different POWs are considered.

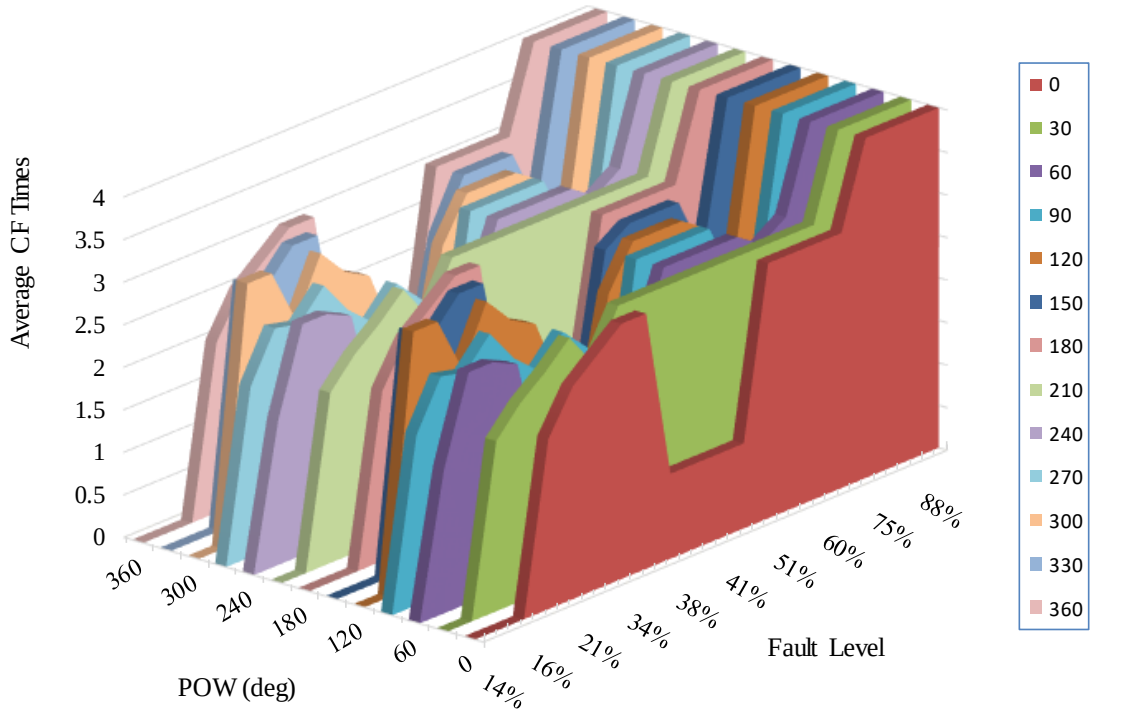
To verify the impact under different fault cases, the fault impedance varies and the corresponding fault level is calculated according to the following equation.

$$\text{Fault Level} = \frac{\text{Fault MVA}}{\text{P}_{dc}} = \frac{\left|\frac{\boldsymbol{E}_{AC}{}^{2}}{\boldsymbol{Z}_{f}}\right|}{\text{P}_{dc}} \tag{6-12}$$

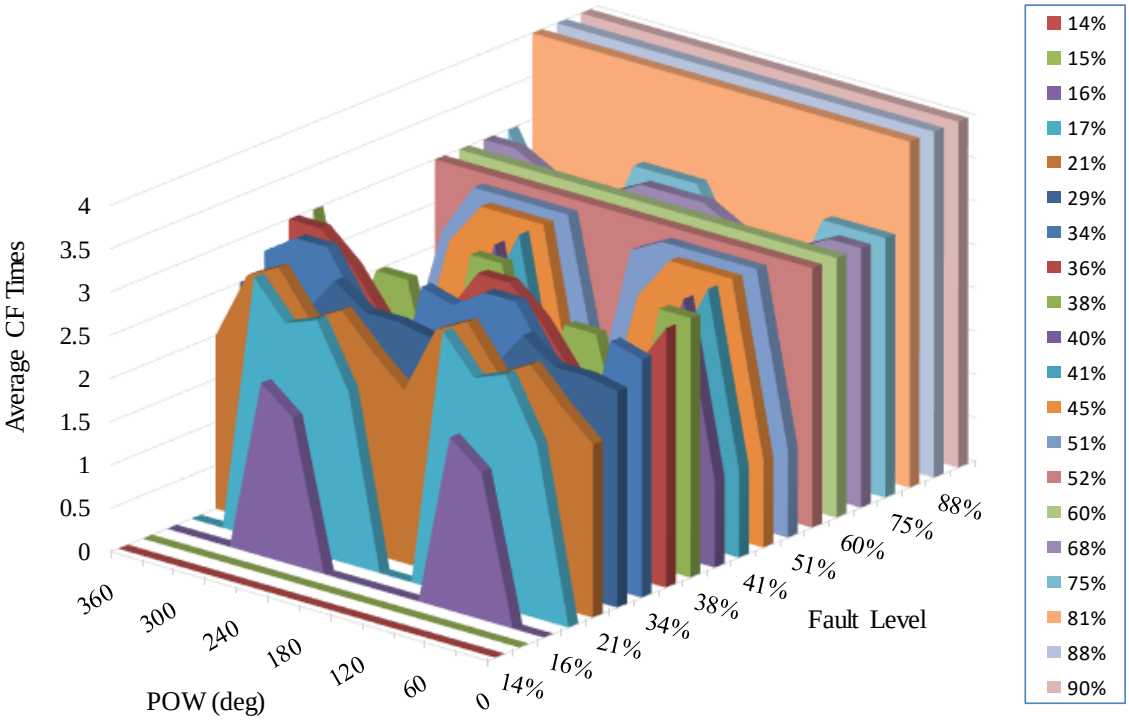
With different POWs and different Fault Levels, each fault case is simulated for 10 times, and the results of average times of CFs in 260 fault cases are shown in Figure 6-8. For instance, for

the average CF times, ‘0’ means no CFs occur during the fault and the recovery process; value between ‘0’ – ‘3’ means 0-3 times of non-continuous CFs (NCCFs) in average occur under the faults; ‘4’ means continuous CFs (CCFs) happen, where the concepts of NCCF and CCF can be found in Section 4.3.

Figure 6-8 (a) illustrates the impact of Fault Level on average CF times under faults with different POWs. It can be seen that with the higher Fault Level, the average CF times are higher. It is interesting to observe that in most cases, the average CF numbers at around 30% Fault Level are higher than those at 40% Fault Level. Such abnormal high average CF times at 30% has been studied in [51] and these CFs defined as “voltage distortion-induced CFs”. Overall, NCCFs start to occur at 15% Fault Level and gradually increase its number until 70% Fault Level where CCFs start to occur. It also can be observed that the impact of the Fault Level on the average CF times is repeated every 180 deg of POW, which also verifies the conclusion that the impact of fault POW on the commutations is periodic every 180 deg which has been analysed in Section 6.3.



(a) Impact of Fault Level on average CF times under faults with different POW



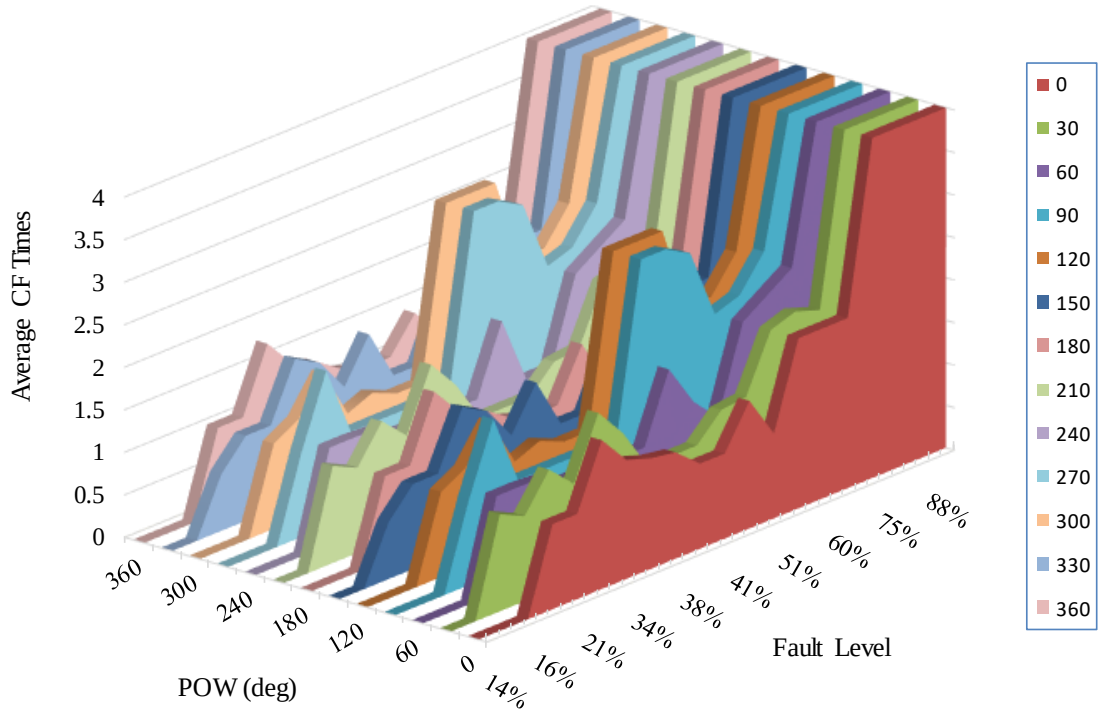
(b) Impact of POW on average CF times under different Fault Levels

Figure 6-8 Relationships between average CF times with POW and Fault Level

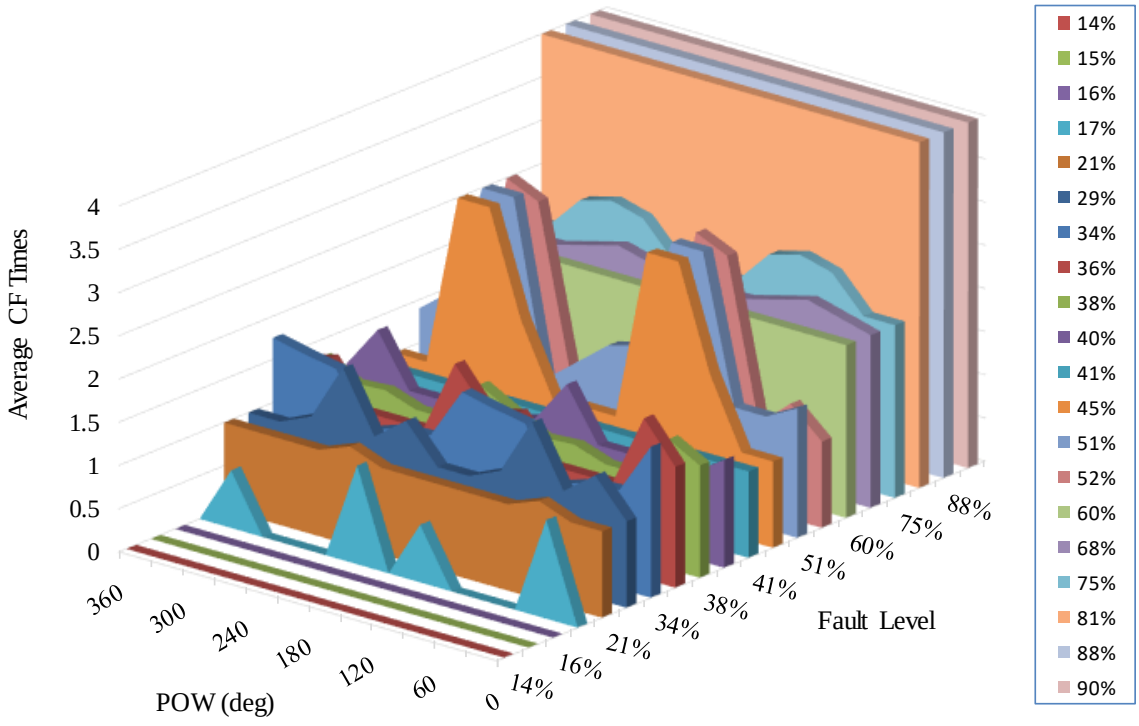
Figure 6-8 (b) depicts the impact of POW on average CF times under different Fault Levels. It can be seen that with the same Fault Level, the average CF times varies with different fault POWs, and the change is periodic with a cycle of 180 electrical deg. For most fault cases with NCCFs, zero and 180 deg of POW will benefit the commutation process, which results in the phenomenon that average CF times under faults with zero and 180 deg of POW is lower than that under faults with 90 and 270 deg of POW. The reason why the most beneficial POW range for the commutation process is not always zero or 180 deg is that it will be affected by the feedback logic loop of PLL, which has been illustrated in Figure 6-3 from Section 6.2. In general, for the fault cases that cause NCCFs, POW has a significant impact on the average CF times under the same Fault Level and the impact is periodic for every 180 deg, and in most cases, the average CF times will also increase under faults with higher Fault Level until CCFs occur.

6.5.2 Verification of the Feasibility of the Proposed FIM-PLL Topology

By applying the proposed FIM-PLL to the CIGRE LCC-HVDC Benchmark system, the fault cases that are demonstrated in the above section are simulated, and the results are compared with the results using the conventional PLL to verify the feasibility of the proposed FIM-PLL topology. The average CF times of the system with the proposed FIM-PLL with different POWs and different Fault Levels is shown in Figure 6-9.



(a) Impact of Fault Level on average CF times under faults with different POW using proposed FIM-PLL



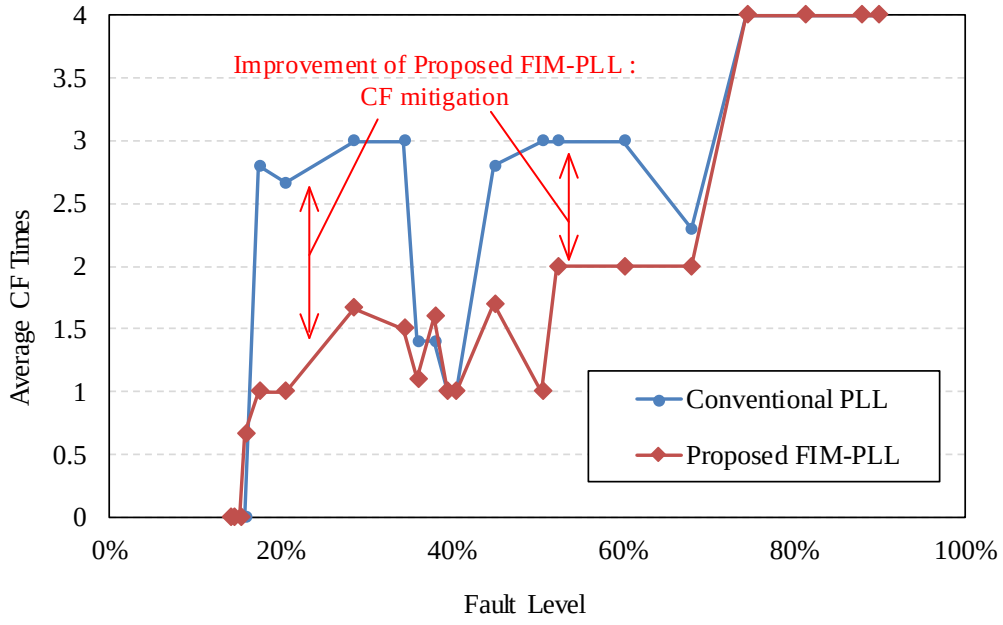
(b) Impact of POW on average CF times under different Fault Levels using proposed FIM-PLL

Figure 6-9 Relationships between average CF times with POW and Fault Level using proposed FIM-PLL

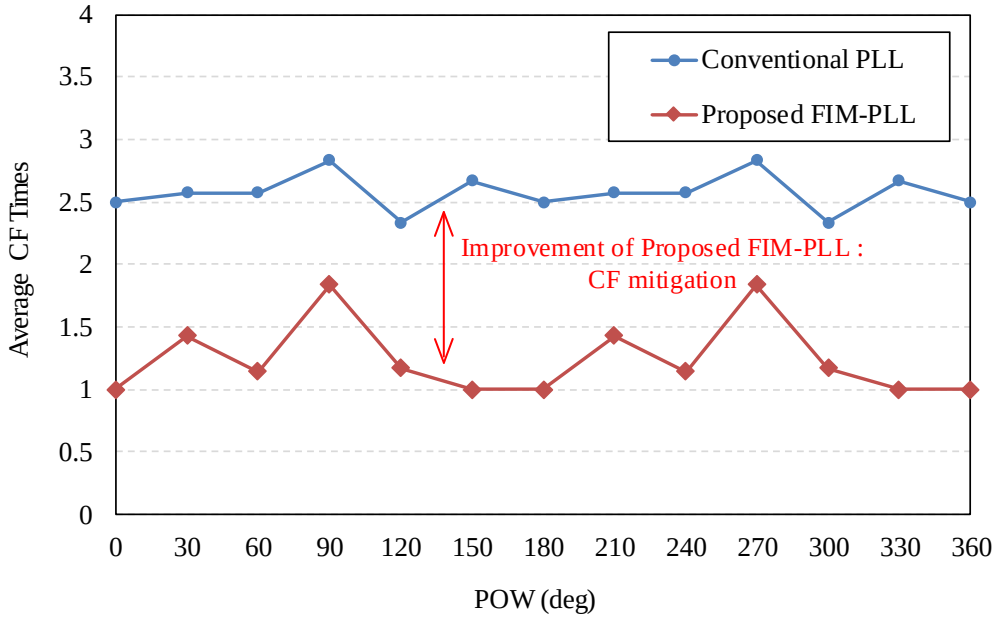
Figure 6-9 (a) presents the impact of Fault Level on average CF times under faults with different POWs. It can be seen that similar to the conclusion obtained from Figure 6-8 (a), the average number of CF times is larger under the higher Fault Level. However, it is interesting to notice that with the proposed FIM-PLL, the abovementioned "voltage distortion-induced CF" at around 30% Fault Level does not exist in most cases. This reflects that the proposed FIM-PLL can effectively eliminate the "voltage distortion-induced CF". Overall, NCCFs start to occur at 17% Fault Level and the number of NCCFs gradually increase until 70% Fault Level where CCFs start to occur. Similar to Figure 6-8 (a), the impact of the Fault Level on the average CF times is repeated every 180 deg of POW.

Figure 6-9 (b) shows the impact of POW on average CF times under different Fault Levels. It can be seen that under the same Fault Level, the average CF times varies with different fault POWs, and the change is periodic with a cycle of 180 electrical deg. Different from conclusions obtained from Figure 6-8 (b), average CF times does not reach a high or low value at a certain POW for all Fault Levels. For instance, average CF times is zero at 90 deg of POW under 17% Fault Level, however, it reaches a relatively high value at 90 deg of POW under 41%-51% Fault Level. In general, for the fault cases that cause NCCFs, POW will affect the average CF times under the same Fault Level and the impact is periodic for every 180 deg, and in most cases, the average CF times will increase under faults with higher Fault Level until CCFs occur. The system with the proposed FIM-PLL can effectively reduce average CF times compared with the CIGRE LCC-HVDC Benchmark using the conventional PLL.

To present a more visualised comparison, the fault case with the Fault Level of 21% and the case with 150 deg POW are compared between the benchmark and the system with the proposed FIM-PLL, as shown in Figure 6-10.



(a) Comparison of average CF times with different Fault Levels when POW = 150 deg



(b) Comparison of average CF times with different POW when Fault Level = 21%

Figure 6-10 Comparisons of average CF times between the benchmark and the system with proposed FIM-PLL

Figure 6-10 (a) shows the comparison of average CF times with different Fault Levels at 150

deg of POW, and Figure 6-10 (b) presents the comparison of average CF times with different POW under 21% Fault Level. It can be seen that the system with the proposed FIM-PLL can reduce the average CF times by as large as 1.5 from 16% to 68% Fault Level under faults with 150 deg of POW. Also, the proposed FIM-PLL can reduce the average CF times by around 1.2 at all values of POW under 21% Fault Level.

After calculating the average CF times for all POW cases under the same Fault Level, the average CF times with different Fault Levels can be compared between the CIGRE LCC-HVDC Benchmark and the system with the proposed FIM-PLL as shown in Figure 6-11.

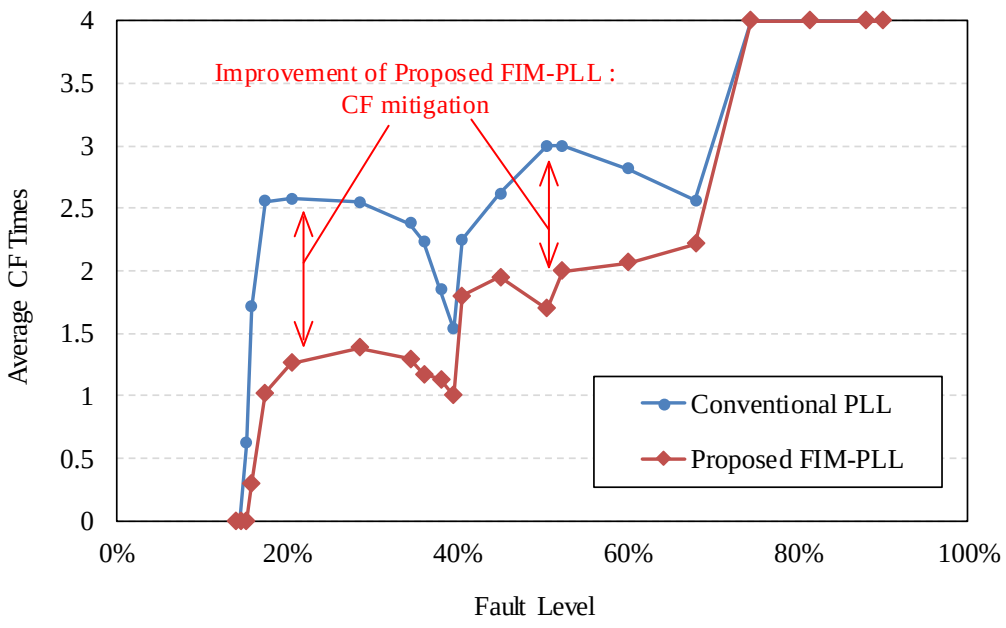


Figure 6-11 Comparison of average CF times under different Fault Levels for all POW cases between the benchmark and the system with proposed FIM-PLL

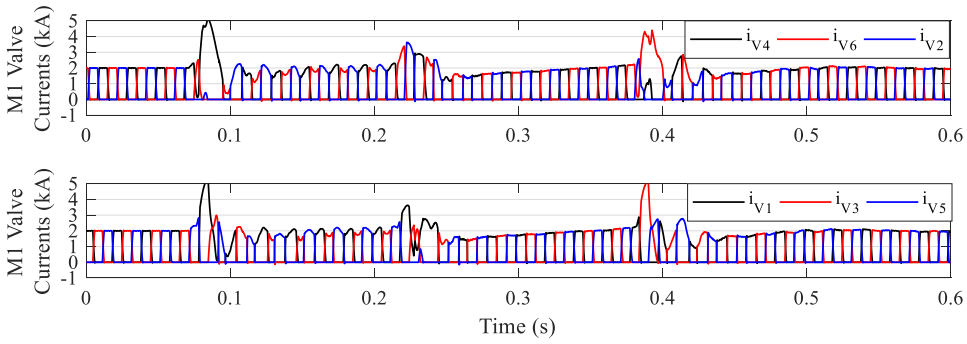
It can be seen from Figure 6-11 that without considering the variation of POW, the average CF times of the system with proposed FIM-PLL is around 1 time lower than the benchmark under the Fault Level from 16% to 68%. The conclusion can be made that the proposed FIM-PLL can bring a significant improvement in mitigating CFs under asymmetrical faults for the LCC-

HVDC systems.

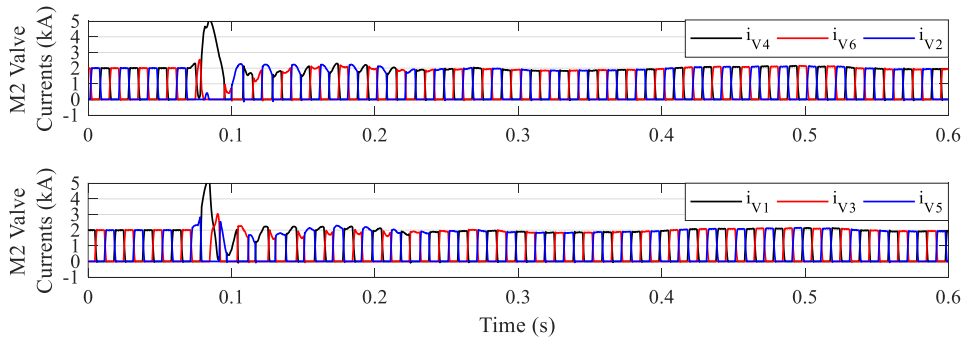
6.5.3 Comparison with the CFPREV Strategy

To further demonstrate the feasibility of the proposed FIM-PLL topology, the simulation results are compared with those using the LCC-HVDC Benchmark system and the benchmark additionally applied with the CFPREV control system [36][90][114]. Parameters of the CFPREV control system used in [114] are utilised in this chapter.

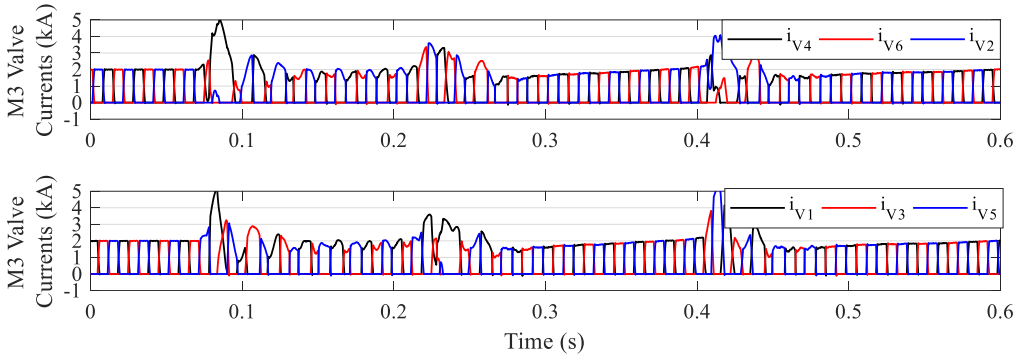
In this case, the fault is a Phase-A SLG fault located in the middle of the 100 km transmission line between the inverter bus and the AC system with 140 ms duration and 50% Fault Level at 30 deg of POW. The valve currents, DC side currents, DC side voltages, the active power transfer, the inverter bus voltages, and the extinction angle measurement γ_{meas} are compared in Figure 6-12 - Figure 6-17.



(a) Valve currents of LCC-HVDC with conventional PLL (M1)



(b) Valve currents of LCC-HVDC with Proposed FIM-PLL (M2)



(c) Valve currents of LCC-HVDC with CFPREV (M3)

Figure 6-12 Comparison of valve currents of LCC-HVDC with conventional PLL, FIM-PLL and CFPREV

where M1, M2, and M3 indicate the CIGRE LCC-HVDC Benchmark system, the LCC-HVDC system with the proposed FIM-PLL, and the LCC-HVDC system with the CFPREV system, respectively.

It can be seen from Figure 6-12 clearly that three intermittent CFs (NCCFs) occur in the CIGRE LCC-HVDC system under this fault condition. The system with the proposed FIM-PLL has only one CF (FCF), which verifies that the proposed PLL topology can successfully suppress CFs. The system with the CFPREV control system also has three NCCFs: the second CF is caused by the sharp increase of the firing angle since the CFPREV control system is switched-out once the measured voltages increase above the pre-set threshold value when the fault is removed; the third CF is caused by the unexpected fluctuations of the commutation voltage and the DC current. This is illustrated by the following figures.

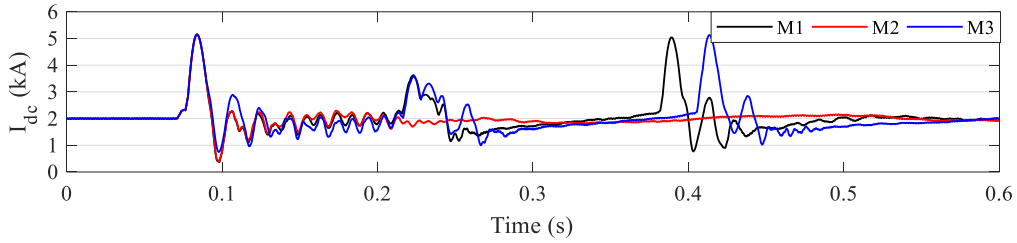


Figure 6-13 Comparison of DC currents of LCC-HVDC with conventional PLL, FIM-PLL and CFPREV

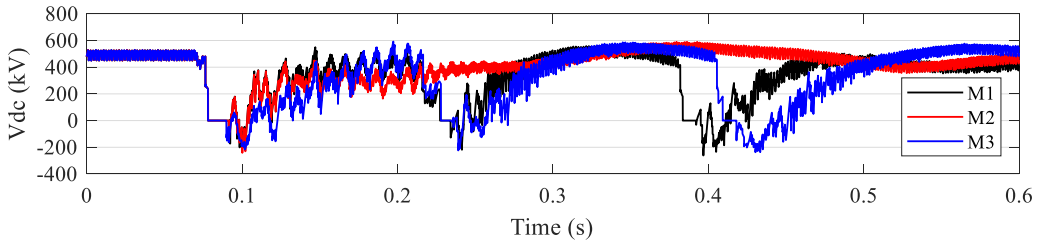


Figure 6-14 Comparison of DC voltages of LCC-HVDC with conventional PLL, FIM-PLL and CFPREV

It can be seen from Figure 6-13 and Figure 6-14 that the CFs result in a voltage sag at the DC side and a sharp increase of the DC current. It also can be seen that in the system with the CFPREV control system, the DC current fluctuations are larger than that in the system with the proposed topology, which is caused by the intermittent switch-out and switch-in of the CFPREV and consequently result in subsequent CFs.

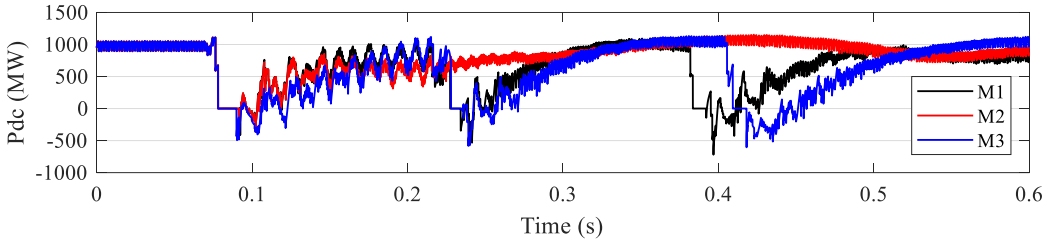


Figure 6-15 Comparison of active power transfer of LCC-HVDC with conventional PLL, FIM-PLL and CFPREV

From the active power comparison in Figure 6-15, it can be concluded that the proposed FIM-PLL can maintain the active power transfer on the DC transmission line after FCF, and enable the system to recover back to the normal operation condition rapidly after the clearance of the fault. However, the system with the CFPREV control system has three times of active power transfer cessations due to the CFs.

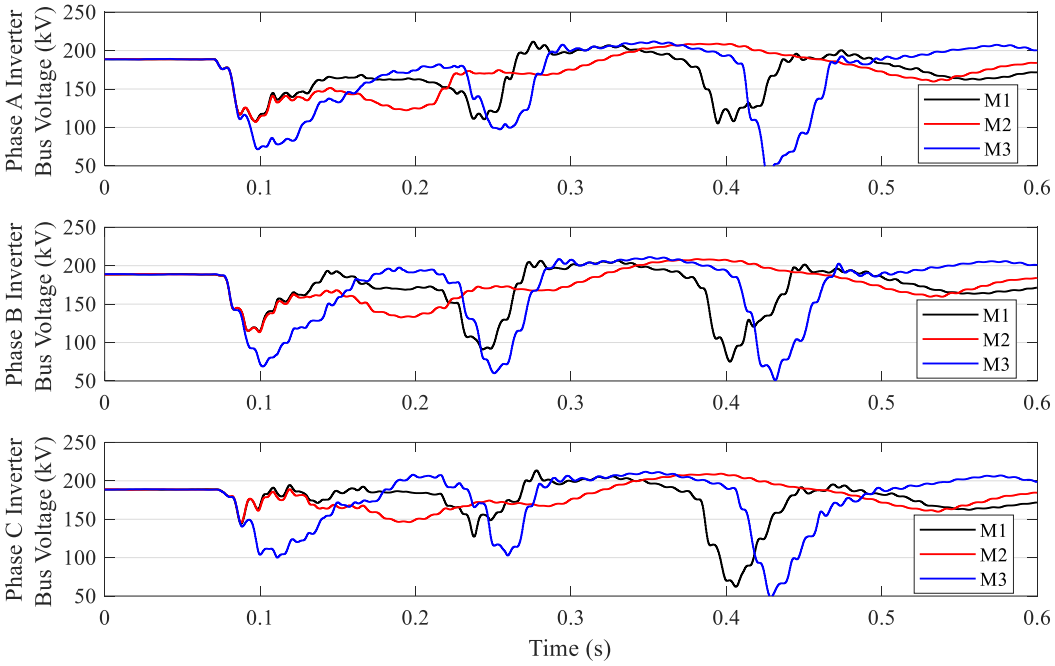


Figure 6-16 Comparison of inverter bus voltages of LCC-HVDC with conventional PLL, FIM-PLL and CFPREV

It can be seen from Figure 6-16 that the inverter bus voltages drop by near 35% when FCF occurs, and the voltages in the system with CFPREV keep decreasing until the voltage reduction reaches 60%, which is caused by the advanced firing instants of the thyristor valves. Then subsequent CFs occur in the LCC-HVDC Benchmark system and the system with CFPREV, and subsequently cause another two times of voltage dip in these two systems after the fault is removed. As illustrated above, the voltage dip occurs not only in the faulty phase but also in the non-faulty phase of the commutation voltages. However, after the FCF, the inverter bus voltages in the system with the proposed FIM-PLL recover to their rated values within 200 ms after the fault, without any sharp reductions afterwards.

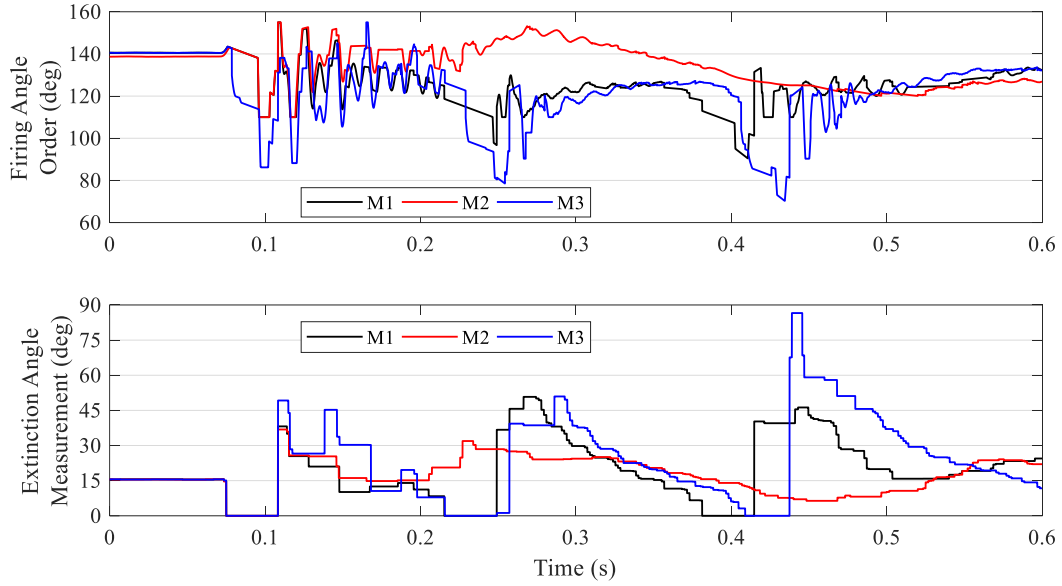


Figure 6-17 Comparison of AOI and γ_{meas} of LCC-HVDC with conventional PLL, FIM-PLL and CFPREV

Figure 6-17 shows the AOI and the measured extinction angles of the three LCC-HVDC systems. It can be seen that the AOI of the proposed system tends to gradually increase after the fault is removed (from t=0.2s to t=0.27s), which is opposite to that of the other two systems. The AOI of the system with CFPREV is quickly reduced from 141 deg to 120 deg under the impact of the CFPREV control system, as mentioned before, and keeps fluctuating after the FCF and finally results in NCCFs. Besides, the measurement value of the extinction angle in the proposed system remains larger than zero after the fault is removed, which proves that the FIM-PLL can suppress CFs effectively. In the meantime, the extinction angles of the system with CFPREV drop to zero for two times after FCF under the impact of the large fluctuations of the inverter bus voltages and insufficient extinction angles due to the sharp change of the AOI.

In conclusion, the proposed FIM-PLL topology can effectively suppress CFs for LCC-HVDC systems under asymmetrical faults and enable the system to recover from the faults more rapidly, compared with the CIGRE LCC-HVDC Benchmark system and the system with the

CFPREV control.

6.6 Discussions

From Section 6.5.2 it can be concluded that the proposed FIM-PLL has remarkable performance in mitigating CFs for LCC-HVDC systems. However, it performs inadequately in terms of CCF suppression. The reason why the CCFs cannot be suppressed is that the faults with CCF risks are too severe, i.e., when Fault Level is larger than 70%, and the FIM-PLL can solely provide a limited advance for the PLL phase angle within the short fault duration. During these extreme fault cases, the magnitude of the faulty-phase commutation voltage is also reduced to a relatively low value. As a result, CCFs will always occur due to the limited value of the phase angle advanced by FIM-PLL. Theoretical analysis can refer to the VTA theory explained in Section 2.3.1, and in these severe fault cases, the VTA provided by the AC system S_{AC_prov} is always smaller than the VTA required by the thyristor valves S_{min_req} for successful commutations.

Potentially three solutions can be carried out to further suppress the CCFs in these severe fault cases. The first solution is to further advance the firing instant of the thyristor valves, which means it can be achieved by decreasing the AOI or further advancing the phase angle of the FIM-PLL output, to enable a larger margin for the commutation and extinction processes. The second solution is to increase the commutation voltage to enable the AC system to provide enough S_{AC_prov} to the thyristor valves for commutating successfully. For example, [24][96] utilize controllable capacitors inserted between the thyristor valves and the transformer to dynamically provide additional voltage for the commutation process to achieve the elimination of CFs. The third solution is to combine the above two solutions – advancing the firing instant

of the thyristor valves and also increasing the commutation voltages. All the above three solutions are designed to enable a larger VTA S_{AC_prov} provided by the AC system to the thyristor valves to attain successful commutations.

6.7 Summary

By analysing the impact of phase angle shifts of the commutation voltages and the impact of POW of the faults on the commutation process, this chapter proposes a Fault Inversion Module (FIM) based PLL to mitigate CFs for the LCC-HVDC systems under asymmetrical faults. Then the proposed FIM-PLL model is built on RTDS and the simulation results verify that:

1) The proposed FIM-PLL can effectively eliminate the impact of POW of asymmetrical faults on the PLL output;
2) The proposed FIM-PLL is able to effectively suppress CFs under faults with 16%-68% Fault Levels;
3) The LCC-HVDC system with the proposed FIM-PLL has better performance in mitigating CFs compared with the CIGRE LCC-HVDC Benchmark system and the system with the CFPREV control;
4) The proposed FIM-PLL enables the inverter bus voltages to recover quickly from the faults, maintains the active power transfer after FCF, and improves the system's stability.
5) The FIM-PLL provides researchers with a better understanding that the commutation voltage phase shifts and POW will affect PLL output and shows the importance of taking into account the phase shifts and AOI when studying the PLL for the purpose of suppressing CFs.

6) The proposed FIM-PLL can be applied in large-scale complex power networks with LCC-HVDC links to achieve CF mitigation, which could not be simulated on RTDS and other EMT simulation platforms due to it processors with limited computational capability.
7) The limitations of applying the FIM-PLL in real projects is that this PLL is designed for mitigating CFs caused by asymmetrical faults.

CHAPTER 7 Economic Analysis of the CF Elimination Strategy based on Controllable Capacitor

7.1 Introduction

As mentioned in Section 1.2.5, most existing CF suppression approaches can only mitigate CFs to some extent, rather than eliminating CFs. Section 6.6 also discusses that advancing the firing instants of the thyristor valves sometimes cannot avoid CFs, and then gives the suggestion that extra commutation voltage calculated by Chapter 2 can be utilised to ensure the ability to eliminate CFs for LCC-HVDC systems.

The Flexible LCC-HVDC proposed by [24] [96] is such a topology that has the capability of eliminating CFs by inserting controllable capacitors to provide extra commutation voltage for the commutation process. However, few published papers have been found to attempt to analyse the cost of these Flexible LCC-HVDC topologies, particularly with detailed calculations and comparisons, which makes it difficult to evaluate the applicability and practicality of the extra voltage approaches that is inserted with additional devices.

Therefore, this chapter aims at analysing the cost of one application of the 'extra voltage' idea proposed in Chapter 2 to maintain successful commutations - the aforementioned Flexible LCC-HVDC topologies which are capable of eliminating CFs. This chapter proposed an economic analysis framework for LCC-HVDC systems based on the Life-Cycle Cost Analysis method and then compare the life-cycle costs of the Flexible LCC-HVDC topologies and the conventional LCC-HVDC system [107] as well as the capacitor commutated converter based HVDC (CCC-HVDC) system.

The structure of this chapter is as follows: Section 7.2 gives the topologies of all LCC-HVDC to be compared; Section 7.3 presents the life-cycle cost analysis model. Section 7.4 shows very detailed case studies that compare the life-cycle costs of the Flexible LCC-HVDC topologies with the conventional LCC-HVDC and CCC-HVDC topologies, and in addition, the impact of redundancy on the costs of the Flexible LCC-HVDC topologies are also considered. The summary of this chapter is presented in Section 7.5.

7.2 LCC-HVDC Topologies

This section presents the topologies of the conventional LCC-HVDC [107], and Flexible LCC-HVDC technologies including CC LCC-HVDC [24], ACFL-CC LCC-HVDC [96], and improved ACFL-CC LCC-HVDC systems. The single-line diagram of conventional LCC-HVDC is shown in Figure 7-1 and the Flexible LCC-HVDC technologies are shown in Figure 7-2 - Figure 7-4.

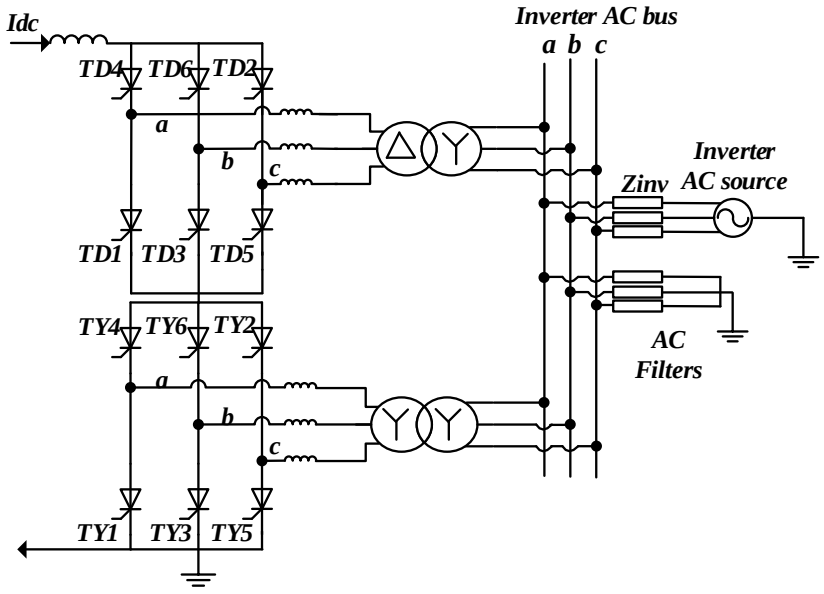


Figure 7-1 Topology of conventional LCC-HVDC [107]

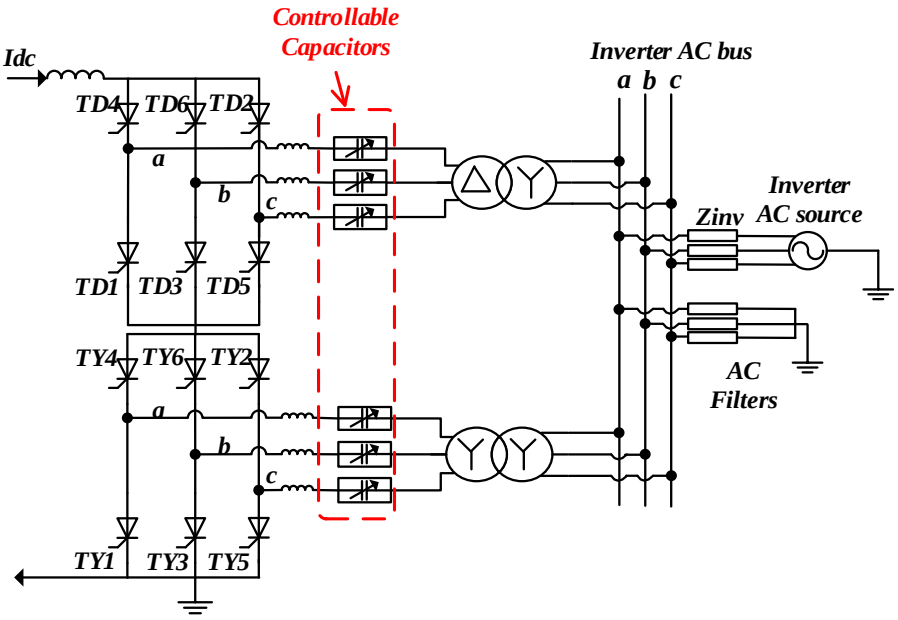


Figure 7-2 Topology of CC LCC-HVDC [24]

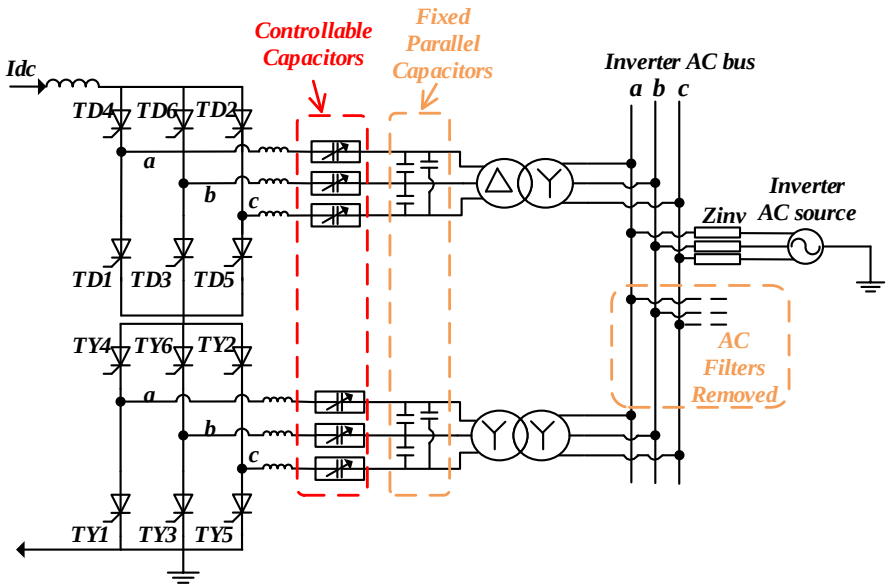


Figure 7-3 Topology of ACFL-CC LCC-HVDC [96]

Topology 1 [107]: Conventional LCC-HVDC system;

Topology 2 [24]: Controllable capacitor based LCC-HVDC system, containing a set of controllable capacitor modules in each phase to eliminate CFs. The working principle of the

controllable capacitors can be briefly described as follows: The controllable capacitors that are connected to the two commutation phases will be inserted in a way that is in favour of the commutation. In this way, the controllable capacitors can provide extra commutation voltages to guarantee the success of commutations and eliminate commutation failure.

Topology 3 [96]: AC Filterless LCC-HVDC system, including fewer capacitor modules and extra parallel capacitors, without passive AC filters that are required in conventional LCC-HVDC systems. The key functions of the parallel capacitors are (1) to accelerate the commutation process; (2) to provide reactive power to the converter and (3) to reduce the harmonics generated by the converter. As a result, the AC filters connected to the inverter AC bus could be removed.

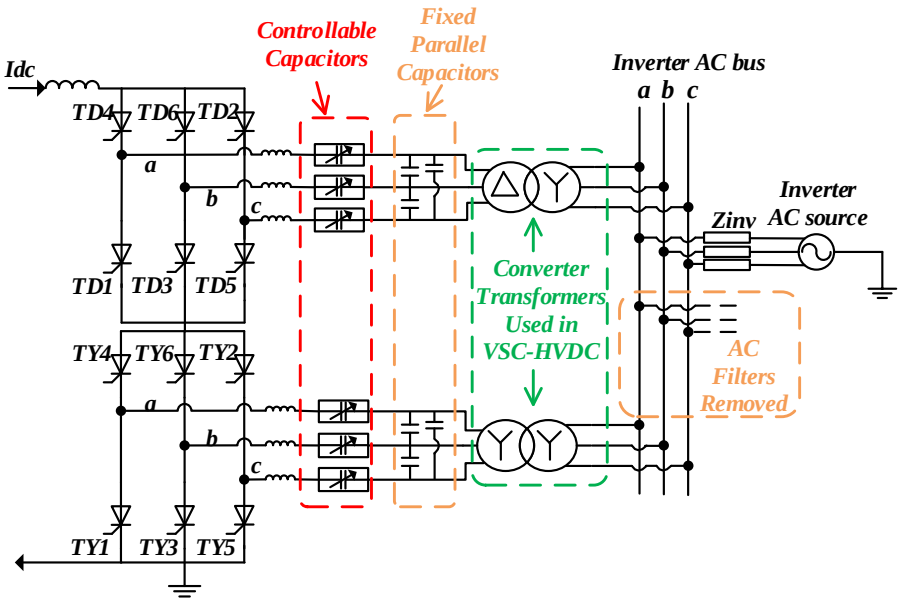


Figure 7-4 Topology of Improved ACFL-CC LCC-HVDC

Topology 4: This is the same as Topology 3 except that the special converter transformers for conventional LCC-HVDC are replaced by converter transformers for VSC-HVDC at a lower cost [115]. Such a replacement is based on the fact that AC filterless LCC-HVDC topology has

lower harmonic currents flowing through than conventional LCC-HVDC [96].

7.3 Economic Analysis Model

The life-cycle cost indicates the total cost of an engineering project from planning and construction to the end of the servicing life cycle. The LCCA model is utilised to analyse all parts of the cost, including the capital investment cost, operating cost, and disposal cost [101][116]–[118]. The expression of the total cost based on LCCA is shown in (7-1):

$$C_{LCCA} = CI + C0 + CM + CFF + CD \tag{7-1}$$

where C_{LCCA} is the total cost based on LCCA; CI is the investment cost; CO is the operating cost; CM is the maintenance cost; CFF is the fault/failure cost; CD is the disposal cost. Detailed breakdown of C_{LCCA} is shown in Figure 7-5.

Considering the time value of money (TVM), different types of costs need to be converted to the same time basis [100]. One of the methods is to annualize all the costs, and another one is to convert all of them to the capital cost. In this chapter, the second method is adopted.

The general expression of the life-cycle cost of the LCC-HVDC projects is shown in (7-2):

$$C_{LCCA} = \sum_{i=1}^{N_{CI}} n_{CI\cdot i} \cdot (CI)_i + \sum_{i=1}^{N_{CO}} n_{CO\cdot i} \cdot (CO)_i + \sum_{i=1}^{N_{CM}} n_{CM\cdot i} \cdot (CM)_i + \sum_{i=1}^{N_{CFF}} n_{CFF\cdot i} \cdot (CFF)_i + \sum_{i=1}^{N_{CD}} n_{CD\cdot i} \cdot (CD)_i \tag{7-2}$$

where N_{CI}, N_{CO} , N_{CM} , N_{CFF} and N_{CD} are the number of types of equipment/service/events which would cause CI, CO, CM, CFF, and CD, respectively; $n_{CI\cdot i}$, $n_{CO\cdot i}$, $n_{CM\cdot i}$, $n_{CFF\cdot i}$ and $n_{CD\cdot i}$ are the numbers of type i equipment/service/events which would cause CI, CO, CM, CFF, and CD, respectively. Detailed calculations for each part will be shown in Section 7.4.

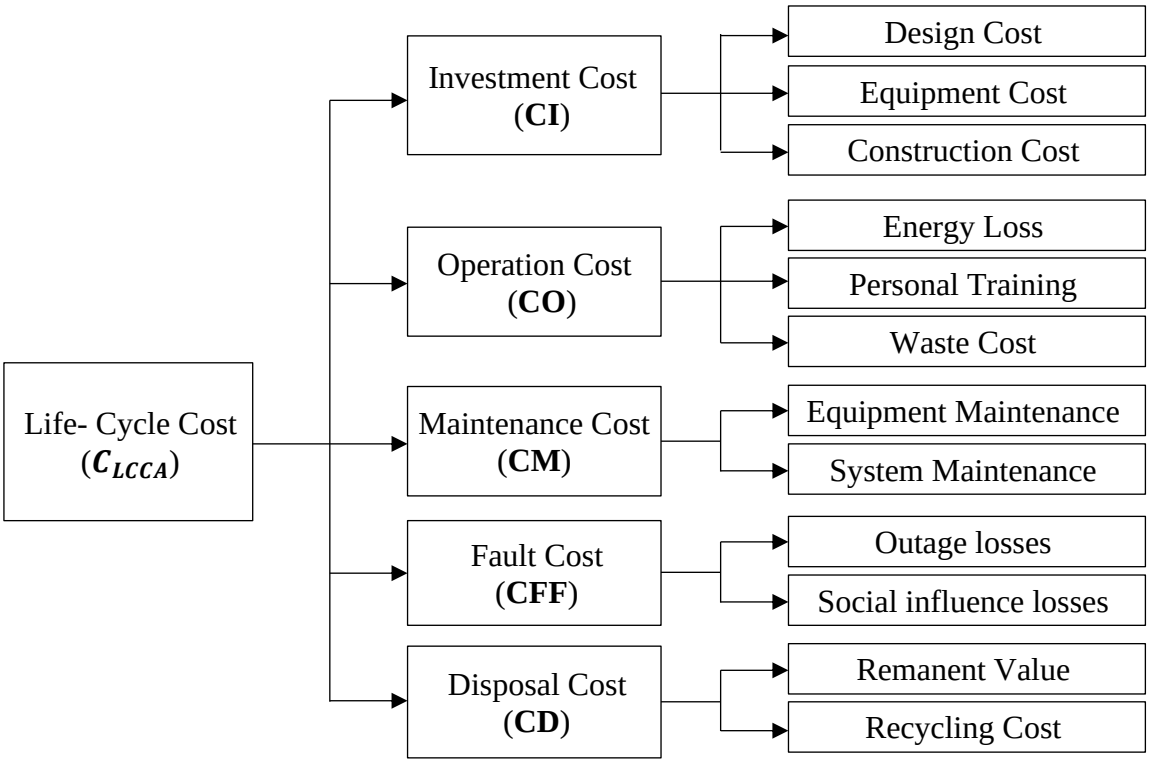


Figure 7-5 Configure of Life-Cycle Cost model

7.4 Economic Case Studies

By applying the LCCA model explained in Section 7.3, the 4 topologies from section 7.2 are studied in this section. Since the main differences among them are at the inverter station, the cost difference in other parts except the inverter station which is caused by the different inverter station configurations is not considered in this chapter. The cost of components at the inverter station are compared using LCCA method based on a typical case of 500kV, 1000MW monopolar LCC-HVDC project. This methodology can be easily applied for LCC-HVDC schemes of different capacities, which can be achieved by inputting different parameters, and the main conclusions remain the same.

7.4.1 Investment Cost of the Inverter Station

This part starts with detailed calculations for each part of the inverter station: converter transformer power ratings, voltage ratings of the controllable capacitors, active power compensations from the parallel fixed capacitors, AC filters, and valve groups.

In the case of a 500kV, 1000MW monopolar LCC-HVDC project:

Topology 1: Conventional LCC-HVDC system;

Topology 2: LCC-HVDC system with controllable capacitors. The voltage rating of the controllable capacitor modules per phase is 28% of the rated DC voltage for CF elimination under zero impedance AC faults [24].

Topology 3: AC Filterless LCC-HVDC system with controllable capacitors. The voltage rating of the controllable capacitor modules per phase is 14% of the rated DC voltage for CF elimination under zero impedance AC faults [96], and the reactive power provided by the parallel capacitor is 82.8% of the rated active power.

Topology 4: The topology is similar to Topology 3 except that the special converter transformers for conventional LCC-HVDC used in Topology 1, 2 & 3 are replaced by converter transformers for VSC-HVDC, which results in a 20% cost reduction on the converter transformers [96].

In addition, since Topology 3 and Topology 4 are AC filterless LCC-HVDC systems, the transformer ratings in their topologies can be reduced as the reactive power required by the converter is compensated locally without passing through the converter transformer. Normally reactive power needed for the converter is around 50%-60% of the rated active power [119][120]. Assuming 60% is applied in this chapter, the apparent power rating for the converter transformer is 1166 MVA for the 1000 MW LCC-HVDC system. Considering that

the efficiency of the converter transformers is as high as 99.85% [121], the converter transformer ratings of Topology 3 and Topology 4 could be reduced by 164 MVA.

Thus, all the above-calculated parameters can be summarised and compared in Table 7-1. The related cost for each component is also shown in Table 7-1.

Table 7-1 Parameters of the main components of the inverters

Component	Topology 1	Topology 2	Topology 3	Topology 4	Cost
Controllable Capacitor Voltage Ratings (kV)	-	140	70	70	50k$/kV [122][123]
Parallel Capacitor Ratings (MVar)	-	-	828	828	3k$/MVar [124]
Converter Transformer Ratings (MVA)	1166	1166	1002	1002	11.9k$/MVA [125]
Converter transformer Cost Coefficient	1	1	1	0.8	11.9k$/MVA
AC Filter & Q Comp.* (p.u.)	1	1	-	-	30% of the transformer [126][127]
Thyristor valves in an Inverter Station (p.u.)*	1	1	1	1	45% of the transformer [127]

* ‘Q Comp.’ indicates reactive power compensators, and the base value of the AC Filter & Q Comp. is 30% of the transformer cost; *Base value of the cost of thyristor valves in the inverter station is 45% of the transformer cost.

Based on the data from Table 7-1, the total cost of each component is calculated and shown in Table 7-2.

Table 7-2 Costs of the main components of the inverters

Cost (M$)	Topology 1	Topology 2	Topology 3	Topology 4
Controllable Capacitors	-	7	3.5	3
Parallel Capacitors	-	-	1.8	1.8
Converter Transformers	13.88	13.88	11.92	9.54
AC Filters & Q Comp.	4.16	4.16	-	-
Thyristor Valves	6.24	6.24	6.24	6.24
Total Cost	24.28	31.28	23.47	21.08

As CI of the inverter station also contains other aspects – the cooling system, DC smoothing reactor, and other auxiliaries, 11% is utilised as the total proportion for these aspects in this chapter [127]. Thus, the final CI comparison is shown in Table 7-3 and Figure 7-6, where 'Proposed Devices' indicates the additional devices, i.e., controllable capacitors and parallel capacitors that are proposed in [24] [96] for the purpose of CF elimination, and the base value for the CI is the CI of Topology 1.

Table 7-3 Investment Costs (CIs) of the inverters

Total Cost	Topology 1	Topology 2	Topology 3	Topology 4
CI (M$)	27.28	34.28	26.47	24.08
Cost Increase Compared with Topology 1 (M$)	-	7	-0.81	-3.2
CI in per-unit (p.u.)	1	1.26	0.97	0.88

From Figure 7-6, it can be seen that the proportion of the converter transformer is 51% of CI in conventional LCC-HVDC and as low as 40%-45% in Topology 2-4. The valve groups of the four topologies take up 18%-26% of their own CIs. The AC filter and reactive power compensator of Topology 1 and 2 account for 15% and 12% of their own CIs, respectively.

Using CI of the conventional LCC-HVDC as the base value, i.e., 1 p.u., the proportions of the cost of additional devices including controllable capacitors and parallel capacitors for Topology 2, 3, and 4 are 26%, 19%, and 19%, respectively.

It can also be concluded that Topology 3 & 4 have lower CIs of the inverter stations than Topology 1 (conventional LCC-HVDC) while these two topologies have the ability to eliminate CFs. This is because the extra fixed parallel capacitors can reduce not only the voltage ratings of the controllable capacitors but also the apparent power of the converter transformers. This shows the applicability of approaches of inserting additional devices to provide 'extra voltage' for maintaining successful commutations from economic perspective.

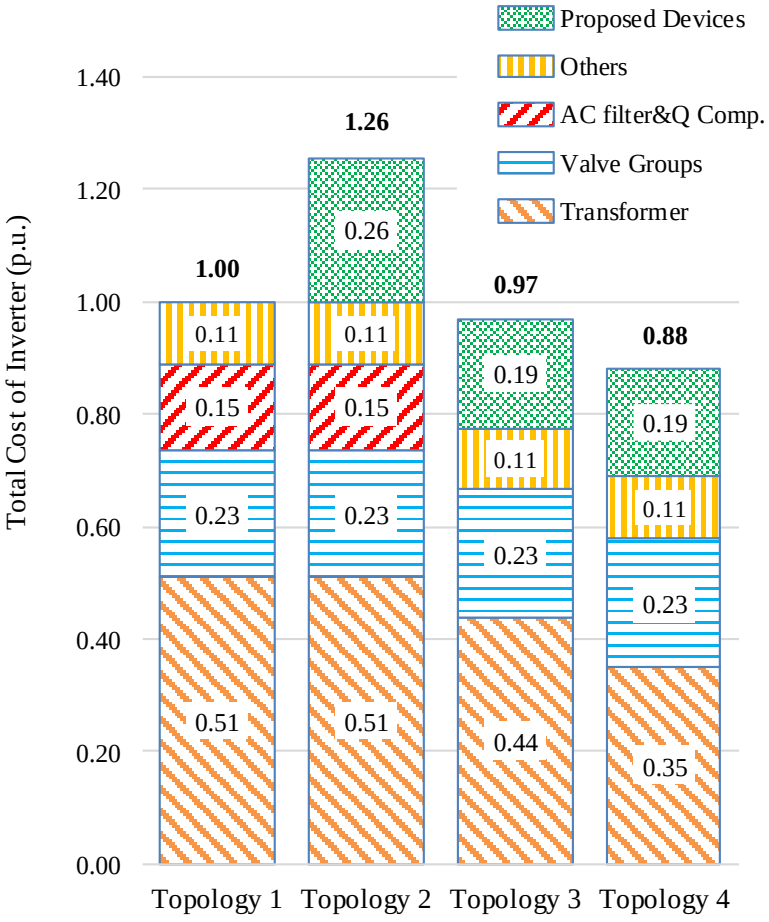


Figure 7-6 Comparison of CIs of the inverter station in P.U.

7.4.2 Other Cost of the Inverter Station

CO&CM: The operation and maintenance cost of a converter station is around 2% of the total CI of the station [126], and the CO&CM difference caused by various maintenance frequency and operation cost due to various inverter topologies is not considered. The additional energy losses caused by the controllable capacitor modules in Topology 2-4 are 2.6 MW, 1.3MW, and 1.3MW, respectively [24]. The efficiency of the converter transformers is normally within the range of 99.6%-99.85% [121][128], then 99.7% of the transformer efficiency is utilised in this chapter. Thus, the power loss reduction on the converter transformers caused by lower apparent power ratings in Topology 3-4 is 0.25MW. Due to the fact that the transmission electricity price varies with different times of the day, transmission capacities, and different areas, a cost rate of 0.05$/kWh for the energy loss is utilised in this chapter [129]. With the assumption of 3200 hours/year of working time for the HVDC systems [105], the annual costs of CO&CMs for the 4 LCC-HVDC topologies are shown in Table 7-4.

Table 7-4 Operation and Maintenance Costs (CO&CMs) of the inverters

Yearly Cost (M$)	Topology 1	Topology 2	Topology 3	Topology 4
Original CO&CM (2% of CI)	0.55	0.69	0.53	0.48
Energy Loss Introduced	-	0.42	0.21	0.21
Energy Loss Reduction	-	-	0.08	0.08
Total Yearly CO&CM	0.55	1.1	0.66	0.61

CFF: According to the CF record shown in Section 7.1 [66], 2-24 CFs caused by AC faults would occur in inverter valves per LCC-HVDC project per year, where 60%-80% i.e. 2-19 times of CFs are caused by transient AC faults [108], and may further result in active power transmission disruptions. The Flexible LCC-HVDC topologies (Topology 2-4) have the ability

to eliminate CFs and could keep 66% rated active power (660 MW) transmission under any type of transient AC faults [122]. Detailed calculations for the improvement on CFF would not be derived in this chapter since the adverse effect of active power cessation is difficult to quantify.

CD: Taking into account the remnant value and disregarding the cost of recycling, 5% of the CI of the inverter station is regarded as the absolute value of CD in this chapter [105]. CDs of the 4 LCC-HVDC topologies are shown in

Table 7-5. The reason why this value is negative is that the CD reduces the life-cycle cost of the inverters.

Table 7-5 Disposal Costs (CDs) of the inverters

Cost (M$)	Topology 1	Topology 2	Topology 3	Topology 4
CD (5% of CI)	-1.36	-1.71	-1.32	-1.2

7.4.3 Life Cycle Cost Comparison for the Inverter Station

Under the 30-year operation condition in the actual cost basis as listed in Table 7-1, the capitalised CO&CM can be calculated as shown in (7-3).

$$CO\&CM_{Capitalized}^{Total} = \sum_{j=1}^{30} \frac{CO\&CM_{year\ j}}{(1+\xi)^{j-1}} \tag{7-3}$$

where j is the year of the life cycle; ξ is the discount rate, assumed constant 7% for the life cycle in this chapter [105], which is used to convert the annual cost during the life cycle to the capital cost; $CO\&CM_{year\ j}$ is the total operation and maintenance cost of each inverter station

in year j, which can be calculated by the operating cost plus the product of maintenance frequency multiply by the maintenance cost each time. In this chapter, $CO\&CM_{year\ j}$ is assumed as 2% of the corresponding CI cost of the inverter station.

It needs to be noticed that the actual cost listed in Table 7-1 will vary in different countries, in different years or even days, under different weathers, for different working teams, etc. The total cost can be obtained by applying actual costs into the above equations and calculations once related data is available.

After applying (7-2) and (7-3) to (7-1), the life-cycle cost C_{LCCA} of the Topology 1-4 is shown in Table 7-6 and Figure 7-7. The base values are the corresponding costs of Topology 1.

Table 7-6 Life-Cycle Cost C_{LCCA} of the inverters

Total Cost (30-year Life Cycle)	Topology 1	Topology 2	Topology 3	Topology 4
CI (M$)	27.28 (1 p.u.)	34.28 (1.26 p.u.)	26.47 (0.97 p.u.)	24.08 (0.88 p.u.)
CO&CM (M$)	7.25 (1 p.u.)	14.63 (2.02 p.u.)	8.75 (1.21 p.u.)	8.11 (1.12 p.u.)
CD (M$)	-1.36 (1 p.u.)	-1.71 (1.26 p.u.)	-1.32 (0.97 p.u.)	-1.20 (0.88 p.u.)
C_{LCCA} (M$)	33.16	47.19	33.89	30.99
C_{LCCA} Increase Compared with Topology 1 (M$)	-	14.03	0.73	-2.17
C_{LCCA} (p.u.)	1.00	1.42	1.02	0.93

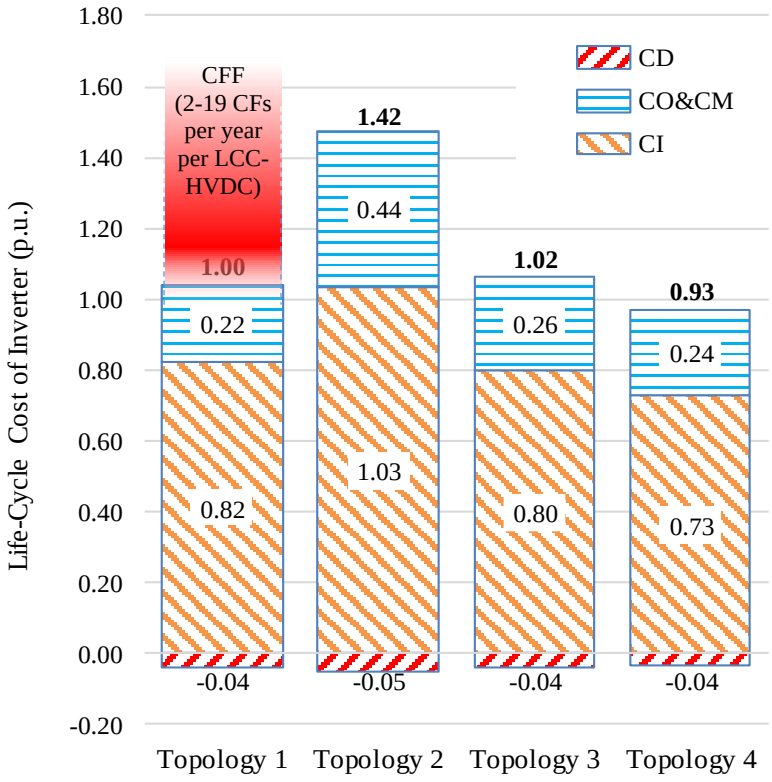


Figure 7-7 Comparison of C_{LCCA} of the inverter station in P.U.

From Figure 7-7, it can be seen that under the abovementioned assumptions of discount rate and CO&CM, 1) C_{LCCA} of Topology 2 is 44% higher than the conventional LCC-HVDC topology, due to the 21% and 22% increase of cost brought by CI and CO&CM, respectively, resulting from the insertion of the controllable capacitors. Its CI and CO&CM are higher than the other 3 topologies; 2) C_{LCCA} of Topology 3 is 29% lower than Topology 2 but 2% higher than Topology 1 and 10% higher than Topology 4. Compared with Topology 1, its CI brings a 2% reduction and CO&CM brings a 4% increase of total cost, resulting in a net 2% increase in the total cost; 3) C_{LCCA} of Topology 4 is the lowest among all topologies, for both CI and CO&CM. Compared with Topology 1, the CI of Topology 4 brings a 9% reduction and CO&CM brings a 2% increase of the total cost, resulting in a net 7% reduction in the total cost; 4) The potential cost of 2-19 times of CFs per year for each LCC-HVDC system can be huge

considering the economic consequences of converter blocking and frequency instability, so it is vital to prevent CFs by inserting additional devices for maintaining successful commutations. Further detailed economic analysis of this will be shown in Section 7.4.8.

7.4.4 Comparisons Considering Different Discount Rate

The discount rate normally ranges from 3% to 10% [130]–[132]. To further analyse the impact of the discount rate on life-cycle cost, the life-cycle cost C_{LCCA} of Topology 1-4 with varying discount rates is shown in Figure 7-8. The discount rate is assumed to be uniform during the life cycle. Again, once there is reliable predictive data of the discount rate, a more actual cost comparison can be obtained by applying each year's predictive discount rate into the calculations.

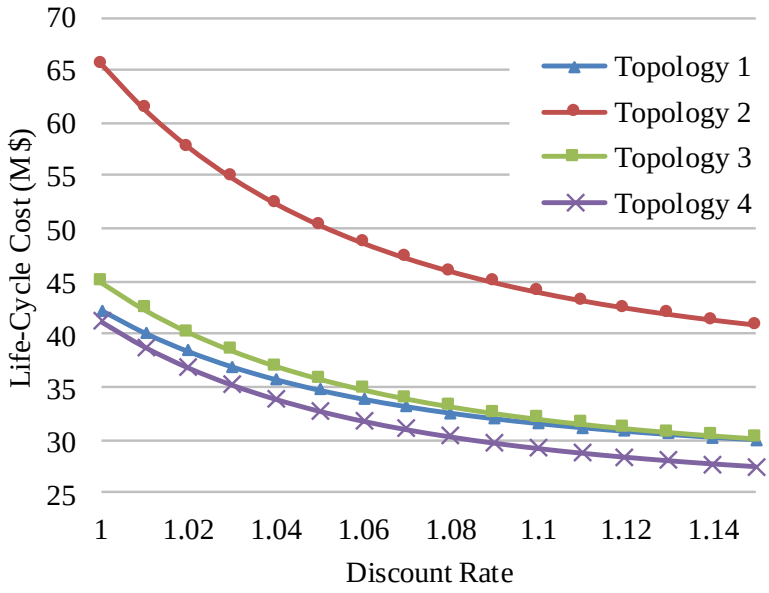


Figure 7-8 C_{LCCA} of the inverter station in M$ with varying Discount Rate

Using C_{LCCA} of the conventional LCC-HVDC (Topology 1) as the base value in each case with different discount rates, the comparison of the life-cycle costs of the four topologies in per-unit is presented in Figure 7-9.

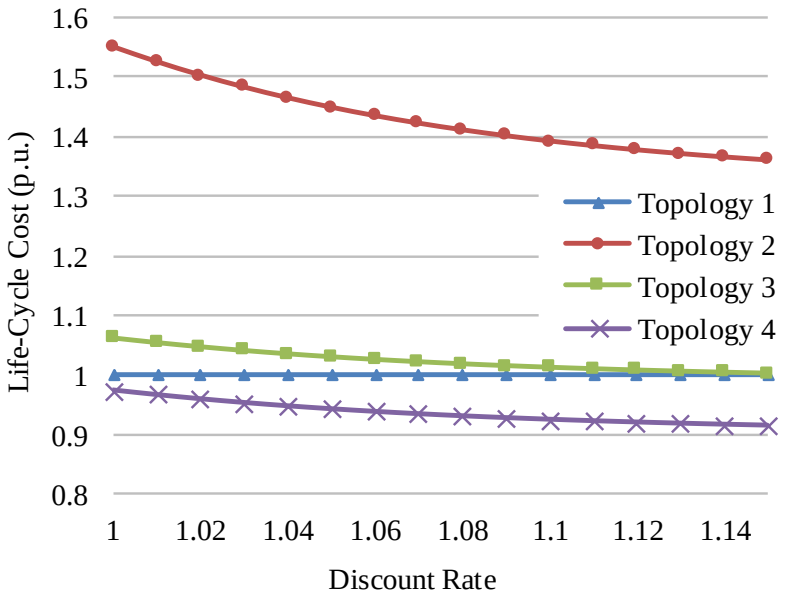


Figure 7-9 C_{LCCA} of the inverter station in P.U. with varying Discount Rate

It can be seen from Figure 7-8 and Figure 7-9 that 1) C_{LCCA} of the four topologies decreases when the discount rate increases; 2) the difference of C_{LCCA} between Topology 3 and Topology 4 nearly remains the same with varying discount rates; 3) C_{LCCA} of Topology 2 is the highest, while C_{LCCA} of Topology 4 is the lowest, and C_{LCCA} of Topology 3 becomes equal to that of Topology 1 when the discount rate reaches 15%. Overall, the conclusions are similar to that from the previous section where a discount rate of 7% is assumed.

7.4.5 Comparisons Considering Practical Fault Impedance

The above analysis is based on the very extreme case – zero impedance grounding faults at inverter AC bus. In reality, the average transmission line fault resistance of most AC faults is 4.39 ohms (rather than zero ohms as used in the analysis in previous sections) based on the measured field data in [133].

The key assumption is that the Flexible LCC-HVDC systems can eliminate commutation failure under the most serious transmission line fault at the inverter side. In this way, a fair

comparison can be made for the 3 Flexible LCC-HVDC topologies. Under such an assumption, the ratings of the controllable capacitors are determined, and the cost comparisons are made. Transmission line faults that are close to the inverter AC bus are considered, as it requires the highest controllable capacitor rating for CF elimination. Given the above considerations, the fault impedance of 4.39 ohms (average transmission line fault resistance) is considered for faults on the inverter bus in this chapter.

By utilizing the analysis and calculations from [95][96], the voltage ratings of the controllable capacitors in Topology 2, 3 & 4 will be reduced to 110kV, 30kV, and 30kV, respectively, to achieve the CF elimination.

Then, by using the similar calculation approach shown in Section 7.4.1-7.4.3, CIs and C_{LCCA} of the inverter stations for the four topologies are listed in Table 7-7, and comparisons are made in Figure 7-10 and Figure 7-11 for CI and C_{LCCA}, respectively.

Table 7-7 Life-Cycle Cost C_{LCCA} of the inverter based on field data

Total Cost (30-year Life Cycle)	Topology 1	Topology 2	Topology 3	Topology 4
CI (M$)	27.28 (1 p.u.)	32.78 (1.20 p.u.)	24.47 (0.90 p.u.)	22.08 (0.81 p.u.)
CO&CM (M$)	7.25 (1 p.u.)	13.04 (1.80 p.u.)	6.64 (0.92 p.u.)	6.00 (0.83 p.u.)
CD (M$)	-1.36 (1 p.u.)	-1.64 (1.20 p.u.)	-1.22 (0.90 p.u.)	-1.10 (0.81 p.u.)
C_{LCCA} (M$)	33.16	44.19	29.88	26.98
C_{LCCA} Increase Compared with Topology 1 (M$)	-	11.02	-3.28	-6.18
C_{LCCA} (p.u.)	1.00	1.33	0.90	0.81

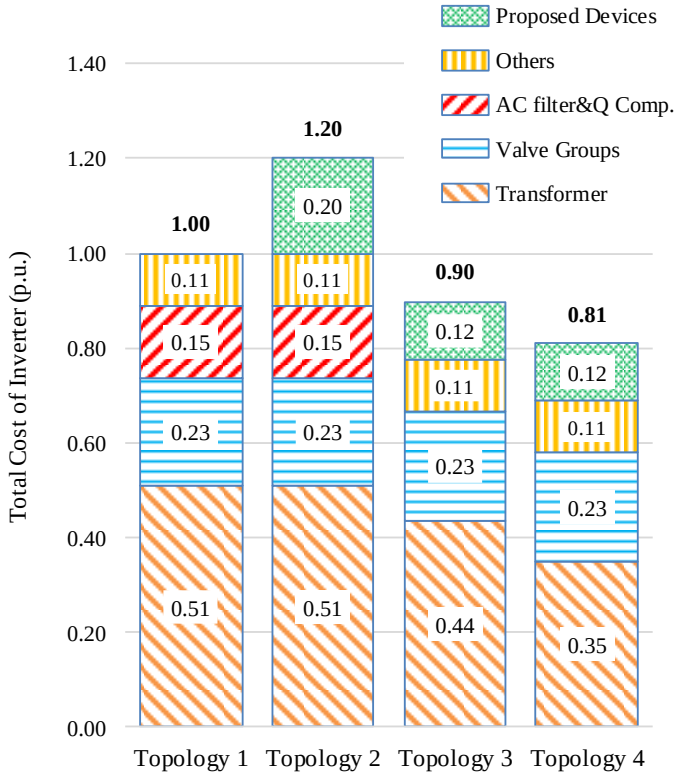


Figure 7-10 Comparison of CIs of the inverter station in P.U. based on field data

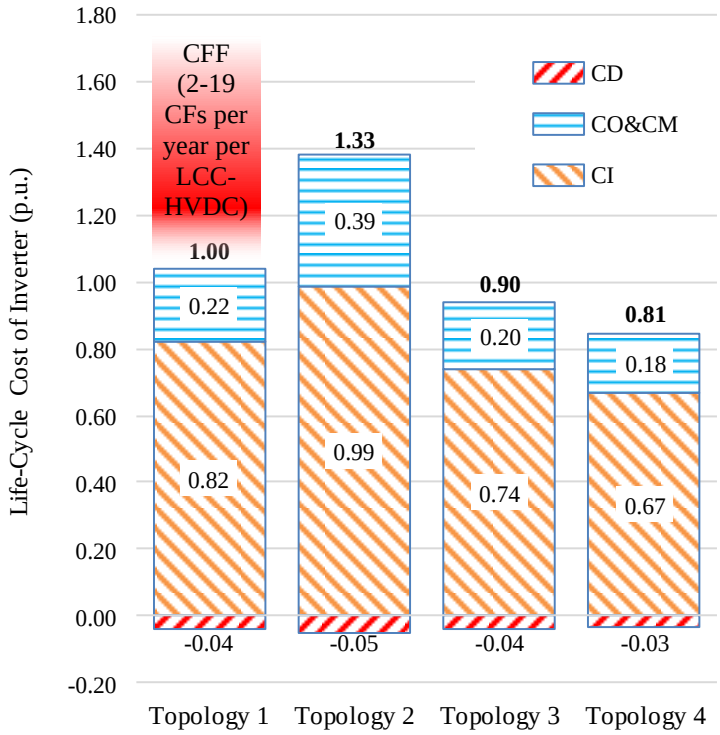


Figure 7-11 Comparison of C_{LCCA} of the inverter station in P.U. based on field data

From Figure 7-10, it can be seen that considering the average AC fault impedance of 4.39 ohm, the extra cost of the proposed devices (i.e., controllable capacitors and parallel capacitors) is reduced from 26% to 20% for Topology 2 and from 19% to 12% for Topology 3 & 4. This decrease saves 6% of CI for Topology 2 and 7% of CI for Topology 3 & 4.

From Figure 7-11, it can be seen that 1) C_{LCCA} of Topology 2 is 39% higher than the conventional LCC-HVDC topology, due to the 17% increase of total cost brought by CI, as well as CO&CM, resulting from the insertion of the controllable capacitors; 2) C_{LCCA} of Topology 3 is 32% lower than Topology 2 and 10% lower than Topology 1 but 11% higher than Topology 4. Compared with Topology 1, CI of Topology 3 causes an 8% reduction and CO&CM brings a 2% reduction of the total cost, resulting in a net 10% reduction in the total cost; 3) C_{LCCA} of Topology 4 is the lowest, for both CI and CO&CM. In comparison to Topology 1, CI of Topology 4 saves 15% of the entire cost, and its CO&CM saves 4%, resulting in a net savings of 19% on the total cost.

By comparing the results in Figure 7-7 and Figure 7-11, it can be concluded that when the practical fault impedance is considered, the cost reduction caused by lowering the controllable capacitor rating could significantly reduce the C_{LCCA} of the Topology 2-4 (9%, 12%, and 12%, respectively). In comparison to Topology 1, the total life cycle costs of Topology 3 & 4 are only 90% and 81%, respectively. In this case, considering the ability to eliminate CFs, Topology 3 & 4 become attractive solutions for future installations of LCC-HVDC systems or upgrades of existing LCC-HVDC systems.

The above comparisons show that the Flexible LCC-HVDC topologies with additional devices to provide ‘extra voltage’ to maintain successful commutations can not only eliminate the CF risks which results in the exemption of CFF, but also reduce the Life-Cycle Cost of the inverter

station by up to 19%, under the same assumptions that the discount rate and CO&CM are uniform in the life cycle, and the difference of the serving life of other pacts caused by different inverter configurations is not considered. In conclusion, the approach of inserting additional devices to ensure successful commutations is applicable in terms of economy.

7.4.6 Comparisons Considering Reliability of Flexible LCC-HVDC Topologies

In the three Flexible LCC-HVDC systems, installed controllable capacitors affect the reliability of the system. It has been studied in [132] that for a MMC converter containing 2562 IGBT submodules (SMs), the converter arms are reliable with availability of higher than 99.99% considering an 8% redundancy rate. Therefore, in order to maintain a similar reliability level for the Flexible LCC-HVDC topologies for a more objective comparison, 8% of redundancy is utilised [134] when comparing the cost as shown below.

The cost increase of the spare parts due to the 8% of redundancy for the Flexible LCC-HVDC topologies and their final life-cycle cost C_{LCCA} are shown in Table 7-8. It can be seen from Table 7-8 that C_{LCCA} of Topology 2-4 increases by 2%, 1%, and 1%, respectively, when using the C_{LCCA} of the conventional LCC-HVDC as the base value (1 p.u.). The increase of C_{LCCA} of Topology 2 is the largest because the voltage rating of its controllable capacitors is higher than that of Topology 3 & 4.

Table 7-8 Cost increase of the inverters based on field data considering the reliability

Cost Increase (M$)	Topology 1	Topology 2	Topology 3	Topology 4
Controllable Capacitors	-	0.44	0.12	0.12
Parallel Capacitors	-	-	0.14	0.14
CI	-	0.44	0.26	0.26

CO&CM	-	0.12	0.07	0.07
CD	-	-0.02	-0.01	-0.01
C_{LCCA}	-	0.53 (0.02 p.u.)	0.32 (0.01 p.u.)	0.32 (0.01 p.u.)
Total C_{LCCA}	33.16 (1 p.u.)	44.72 (1.35 p.u.)	30.20 (0.91 p.u.)	27.30 (0.82 p.u.)

The comparisons of CIs and C_{LCCA} of Topology 1-4 considering the additional cost due to redundancy are shown in Figure 7-12 and Figure 7-13, respectively.

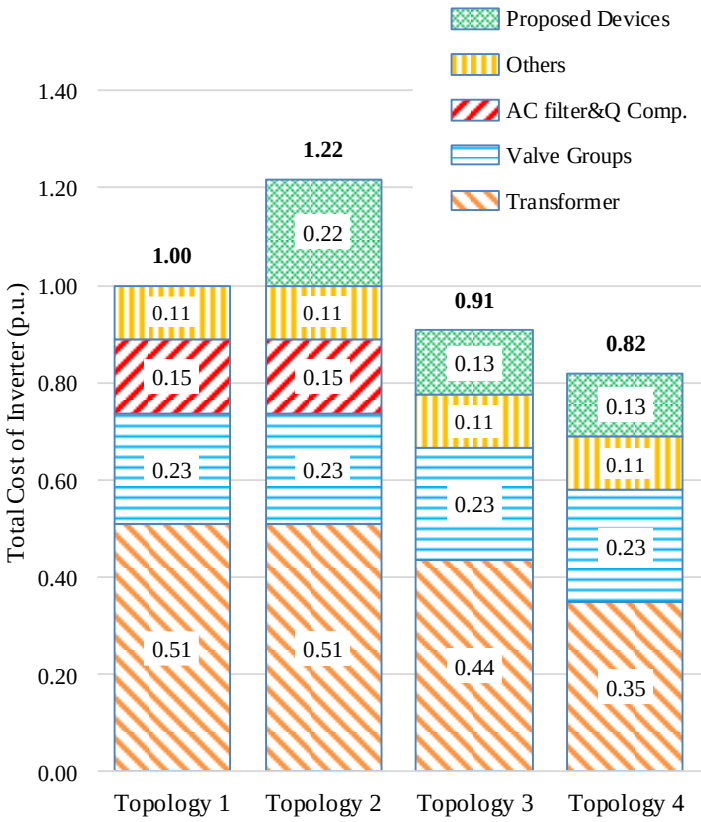


Figure 7-12 Comparison of CIs of the inverter stations in P.U. considering reliability of the Flexible LCC-HVDC topologies

From Figure 7-12, it can be seen that the only difference of CI compared with Figure 7-10 is that the 'Proposed Device' in Topology 2-4 increases by 0.02 p.u., 0.01 p.u., and 0.01 p.u.,

respectively. This is due to the consideration of 8% redundancy to maintain the reliability of the three Flexible LCC-HVDC topologies.

Similarly, it can be concluded from Figure 7-13 that the C_{LCCA} of Topology 2-4 increases by 0.02 p.u., 0.01 p.u., and 0.01 p.u., respectively, compared with Figure 7-11. This increase of costs is due to (1) 8% redundancy of controllable capacitors and parallel capacitors; (2) the increase of losses of redundant components and (3) the increase of CO&CMs of redundant components.

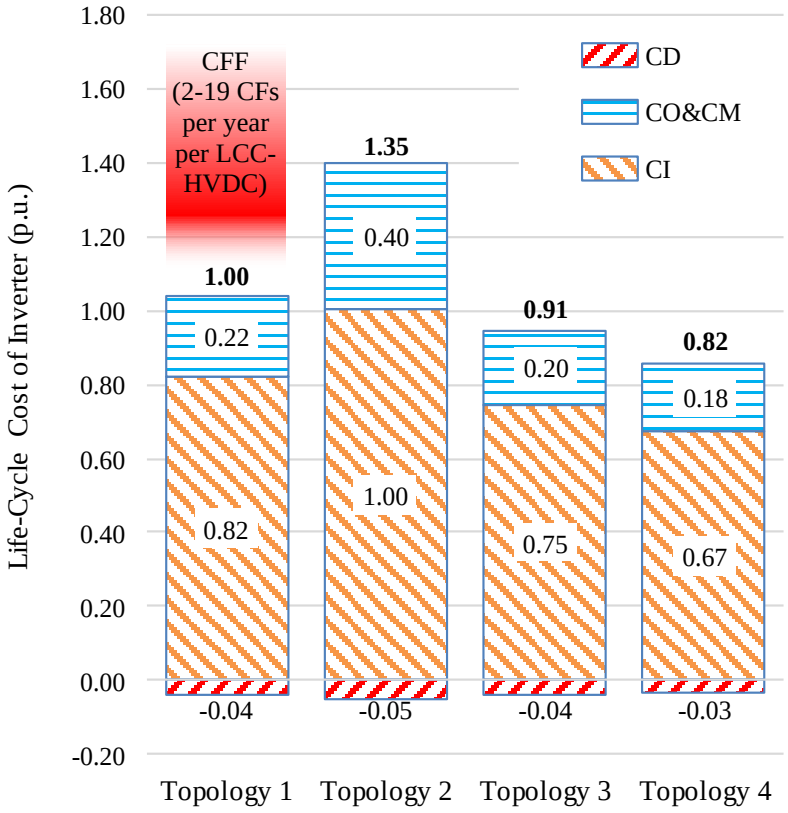


Figure 7-13 Comparison of C_{LCCA} of the inverter stations in P.U. considering reliability of the Flexible LCC-HVDC topologies

7.4.7 Comparison with the CCC-HVDC Topology

This section presents the cost comparison of Capacitor Commutated Converter-based HVDC

(CCC-HVDC) and Topology 1-4 considering the same rating of 500kV and 1000MW.

For CCC-HVDC, due to the installation of fixed series capacitors at the valve side of the converter transformer, the reactive power rating of the series capacitors is 345 MVar, and the AC filter rating is 155 MVar according to [135]. Using 10k$/MVar [122] as the price of the series capacitors, the comparison of costs between the Flexible LCC-HVDC topologies with CCC-HVDC topology (Topology 5) is shown in Figure 7-14 and Figure 7-15. The 'Proposed devices' for Topology 5 (CCC-HVDC) indicate the cost of fixed series capacitors in CCC-HVDC.

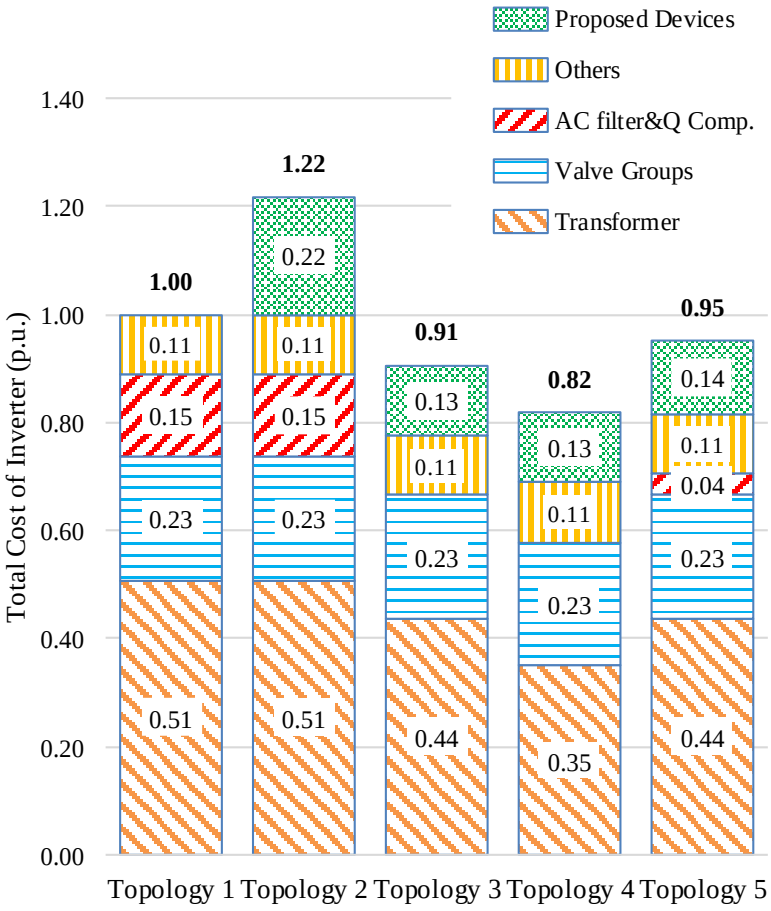


Figure 7-14 Comparison of CIs of the inverter stations in P.U. including CCC-HVDC topology

It can be seen from Figure 7-14 that the CI of the CCC-HVDC is 5% lower than the

conventional LCC-HVDC, but 4% and 13% higher than Topology 3 and Topology 4, respectively. The cost decrease, compared with the conventional LCC-HVDC, is due to the lower ratings of the converter transformer, the AC filter, and the reactive power compensator.

It can be also summarised from Figure 7-15 that the C_{LCCA} of the CCC-HVDC topology is 8% lower than the conventional LCC-HVDC, but 1% and 10% higher than Topology 3 and 4, respectively. Besides, the risk of CFs in the CCC-HVDC topology is similar to that in conventional LCC-HVDC topology.

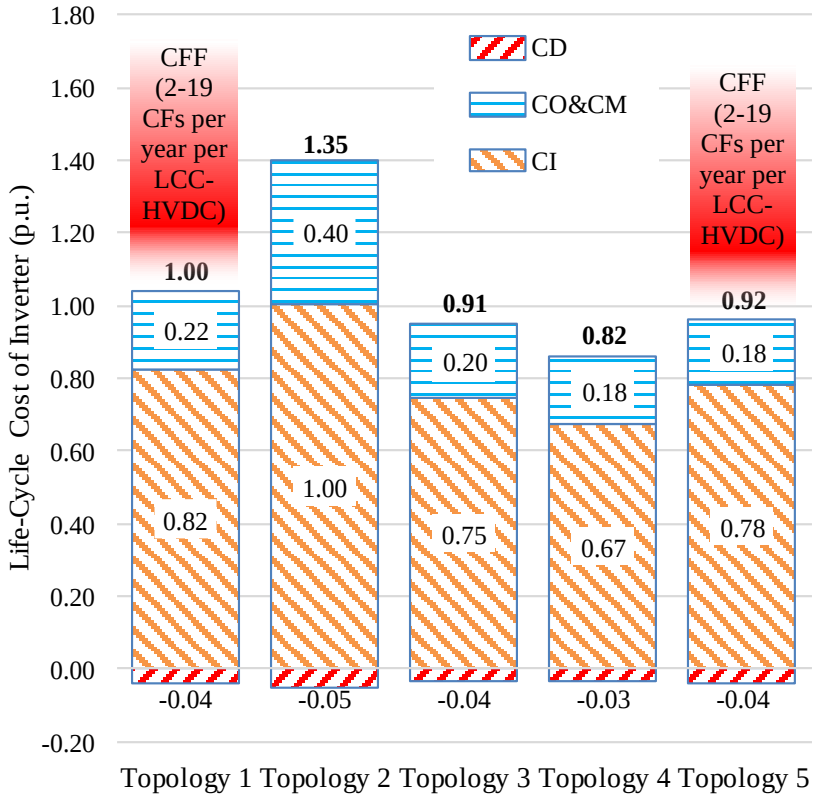


Figure 7-15 Comparison of C_{LCCA} of the inverter stations in P.U. including CCC-HVDC topology

7.4.8 Other Factors Affecting the Cost

1. Land cost saving - Harmonic filtering and reactive compensation make a significant contribution to the size of the converter station, which can take up 50% of the overall

footprint [136]. Topology 3&4 could save even more cost since no AC filters or reactive power compensators shunt on inverter bus are needed, and Topology 4 could save more than Topology 3.

2. Lower harmonics - Conventional Topology 1 has the operation characteristic of generating a significant amount of AC harmonic currents which will increase the energy loss and overheat adjacent devices [22]. Topology 3&4 have better performance on mitigating the harmonic currents flowing through the converter transformer, as the harmonic currents at the secondary side of the transformer have been filtered locally. Therefore, Topology 3 & 4 can reduce the heating of the transformer, slow down the aging of the isolating material, and prolong the transformer's life.
3. Lower costs in preventing CFs - Although the CFF of the LCC-HVDC topologies is difficult to quantify as mentioned in 7.4.2, it has been validated that the three Flexible LCC-HVDC topologies (Topology 2-4) are capable of eliminating the CFs caused by any types of transient AC faults, thereby keeping the power systems operating in a safer status. Without the CF-eliminating LCC-HVDC topologies, the CFs may cause inverter station blocking, rectifier-side generator tripping, and even removal of the load near the fault, which would result in serious oscillation and instability problems in power systems. The instability of the power systems would further jeopardize the safety of lives and property. For example, one million households were left in the dark, and trains were forced to a standstill around the United Kingdom, affected by the major blackout across large areas of England and Wales in August 2019, and this blackout resulted from the cut-off of two power plants by lightning and the sharp drop of the frequency (48.9 Hz) [137]. The estimated cost of this blackout event was more than £15 million [138] and three energy companies paid £10.5 million for this blackout [139]. Besides,

£616 million was spent on controls for managing the frequency of the GB electricity system [140]. Topology 2-4 can sufficiently maintain the power system's stability under AC faults and further significantly reduce the risks and potential costs.

7.5 Summary

This chapter analyses the life cycle costs of inverter stations of 5 HVDC topologies: the conventional LCC-HVDC, 3 Flexible LCC-HVDC topologies, namely, CC LCC-HVDC, ACFL-CC LCC-HVDC and the improved ACFL-CC LCC-HVDC, and the conventional CCC-HVDC. All the 3 Flexible LCC-HVDC topologies are capable of eliminating commutation failure and providing fast dynamic voltage control. Based on the LCCA method with the assumptions that the discount rate is constant in the life cycle and the operation and maintenance cost is not affected by the impact of different inverter topologies, it can be concluded that the Flexible LCC-HVDC topologies can not only eliminate the CF risks, but also can reduce the life-cycle cost by up to 18% and 9% of the conventional LCC-HVDC topology and CCC-HVDC topology, respectively, even in the case that 8% of redundancy for the additional devices (e.g., controllable capacitors and fixed shunt capacitors) is considered. The cost comparisons show that the 'extra voltage' proposed by Chapter 2 by inserting additional devices for maintaining successful commutations is applicable from economic perspective, and the economic analysis in this chapter can help system operators make decisions of the inverter configurations when planning LCC-HVDC projects and upgrading the existing ones.

CHAPTER 8 Conclusions and Future Work

8.1 Conclusions

This research presents two commutation voltage calculation methods for predicting Commutation Failures (CFs) and Continuous CFs (CCFs) in Multi-Infeed LCC-HVDC systems under asymmetrical faults. Then the immunity of the inverters to CCFs and the interaction mechanism of the inverters under asymmetrical faults with CF risks are analysed. Furthermore, an extended PLL topology is proposed to suppress CFs in LCC-HVDC systems by eliminating the detrimental impact of unbalanced commutation voltage inputs.

The first part of this thesis (Chapter 2 - Chapter 4) accurately calculates the commutation voltages in LCC-HVDC systems and demonstrates that all magnitudes and phase angles of both faulty and non-faulty phase commutation voltages will change and become unbalanced under asymmetrical faults, which is not comprehensively considered in existing literature. Accurate calculation results of the commutation voltages have been verified by simulations on RTDS and used to predict CFs and CCFs in Multi-Infeed LCC-HVDC systems based on the Voltage-Time Area (VTA) theory. The new prediction methods are demonstrated by comparisons with simulation results of a six-machine-two-area (6M2A) system that can reduce the prediction error by more than 60% compared with previous research which does not consider the changes of the non-faulty phase commutation voltages under asymmetrical faults. The proposed mathematical CF prediction methods can be applied to complex and large-scale power systems with LCC-HVDC systems which is difficult to be simulated on RTDS and other EMT simulators due to their limited computing capability of the processors. Therefore, the fast, accurate and efficient CF prediction methods proposed in this thesis can help power system

operators design new LCC-HVDC projects or upgrading existing ones. In this part of the study, **Objective 1** was accomplished.

The second part of this thesis (Chapter 5) studies the interaction mechanism of the inverters in the Multi-Infeed LCC-HVDC system under asymmetrical faults. An Immunity Index for the inverters to CCFs (IICCF) is proposed on the basis of VTA theory and it can be used to describe inverter's performance to maintain successful commutations under asymmetrical AC faults, which is not considered in the existing literature. Then an Interaction Factor of inverters under faults with CCF risks (IFCCF) is proposed and it can be used to study the interaction mechanism of inverters in Multi-Infeed LCC-HVDC systems under asymmetrical faults with CCF risks, which is also not considered in previous research. By being compared with the Critical IFCCF (CIFCCF) which can be obtained by IICCFs of the inverters, the commutation performance of an inverter when a nearby inverter is experiencing CCFs in a Multi-Infeed LCC-HVDC system can be forecasted. The feasibility and accuracy of the two factors are validated by simulations of the 6M2A system on RTDS and it shows that they are more accurate under asymmetrical faults compared with not considering the non-faulty phase commutation voltage changes. The two quantitative indices can help the system operator estimate the safety margin of inverters in normal operation conditions without CCF risks and predict CCFs, and then help design and upgrade LCC-HVDC projects. They could also enable researchers to quantitatively learn the interaction mechanism between inverters under asymmetrical faults with CCF risks, and understand the impact of the unbalanced phase shifts and magnitude changes of all three phase commutation voltages on the commutation process. In this part of the study, **Objective 2** was accomplished.

The third part of this thesis (Chapter 6) proposes a Fault Inverse Module based PLL (FIM-

PLL) to mitigate CFs in the LCC-HVDC system. By analysing the impact of the phase angle shifts of the commutation voltages and the impact of POW on the PLL output, it is illustrated that the AC faults are not always detrimental to the commutation process. The FIM module in the proposed PLL can be utilised to eliminate the adverse influence of the unbalanced commutation voltage inputs of the PLL on the commutation process under asymmetrical faults. The effectiveness of the proposed PLL in mitigating CFs is demonstrated by simulations of the CIGRE LCC-HVDC Benchmark on RTDS. The analysis in this part can improve the researchers' understanding of the impact of the unbalanced phase shifts of commutation voltages caused by asymmetrical faults on the PLL output and consequently on the commutation process. The proposed FIM-PLL topology can be applied to LCC-HVDC systems to mitigate CFs and help system operators in design and upgrade the control systems for LCC-HVDC projects. In this part of the study, **Objective 3** was accomplished.

Besides, the final part of this thesis (Chapter 7) carried out the economic analysis of the CF elimination approach. As discussed and demonstrated in Chapter 6, advancing the firing instants of inverter thyristor valves cannot always prevent CFs due to the low commutation voltage. Therefore, a sufficient measure to provide extra voltage levels for the commutation process which can be calculated in Chapter 2. This has been realised by the Flexible LCC-HVDC proposed by [24] with controllable capacitors. To research the applicability of the 'extra voltage' for avoiding CFs from economic perspective, the economic analysis framework based on the Life-Cycle Cost Analysis method is developed for LCC-HVDC systems. The comparisons of the costs show that the Flexible LCC-HVDC topologies can reduce the cost of the LCC-HVDC projects by up to 18% while avoiding suffering from CFs. Thus, the approach to reducing CF risks by providing extra commutation voltage is feasible and applicable in designing new LCC-HVDC projects and upgrading existing ones. In this part of the study,

Objective 4 was accomplished.

The research presented in this thesis has verified the accuracy and effectiveness of the new mathematical CF prediction methods, the IICCF and IFCCF for quantifying inverters' commutation performance in Multi-Infeed LCC-HVDC systems under faults with CCF risks, and the extended PLL topology for mitigating CFs. Therefore, the aim of this research has been achieved.

8.2 Future Work

As presented in Chapter 5, the proposed IICCF and IFCCF based on the CCF prediction methods proposed in Chapter 4 can be utilised to estimate the commutations of inverters in Multi-Infeed LCC-HVDC systems under AC faults with CCF risks. A potential follow-up research direction based on the two new factors will be the CCF risk area identification for the Multi-Infeed LCC-HVDC systems and new measures to minimize the risk areas. Besides, the application of the proposed methods and indices in the future power system where more and more Inverter-Based Resources (IBR) are integrated could be researched. Future work may also include hardware-in-loop experiments based on the proposed CF Prediction methods.

As discussed in Chapter 6, changing the firing order of the thyristor valves to mitigate CFs sometimes does not work, due to the insufficient commutation voltage magnitude. That's why Chapter 2 derives the extra voltage for maintaining successful commutations which is realised by the Flexible LCC-HVDC topology with controllable capacitors analysed in Chapter 7. The combination of advancing the firing instants for thyristor valves and inserting additional devices for providing extra commutation voltages to realise the balance between the CF elimination performance and the economy of new LCC-HVDC topologies will be of interest.

Appendix

A.1 The Three-Line Diagram of the 6M2A System

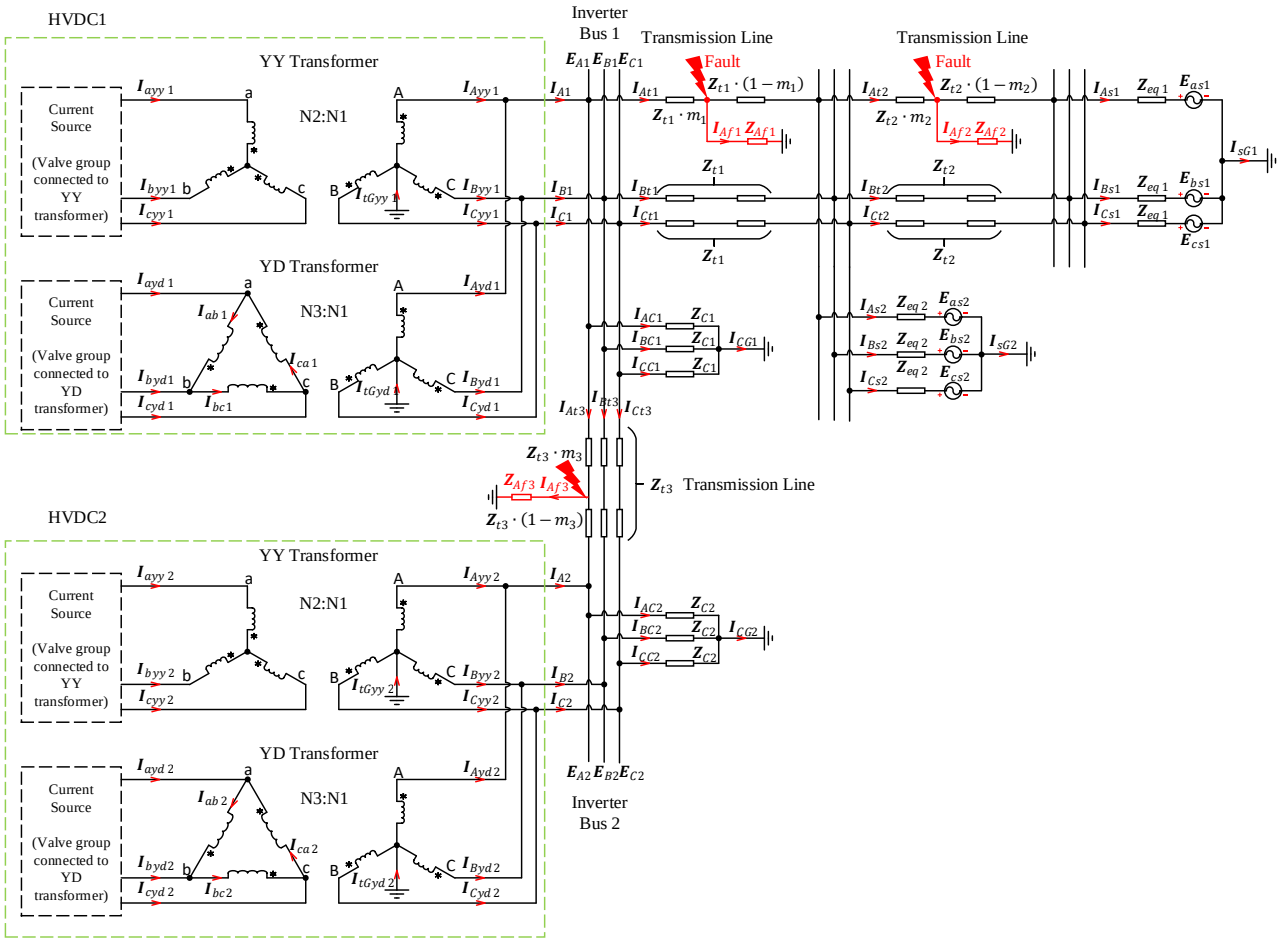


Figure A-1 Three-line circuit diagram of the inverter side of the 6M2A system

A.2 Detailed Equations for Commutation Voltages of 6M2A System in 2.4.2

$$\boldsymbol{I}_{Aac1} = \left(\frac{N3}{N1}\cdot \boldsymbol{I}_{ab1} + \frac{N2}{N1}\cdot \boldsymbol{I}_{ayy1}\right)\cdot \boldsymbol{K}1 + \left(\frac{N5}{N1}\cdot \boldsymbol{I}_{ab2} + \frac{N4}{N1}\cdot \boldsymbol{I}_{ayy2}\right)\cdot \boldsymbol{K}2 - \boldsymbol{E}_{Aeq}\cdot \boldsymbol{K}3 \tag{A1}$$

$$\boldsymbol{I}_{Af3} = \boldsymbol{I}_{Aac1}\cdot \frac{\boldsymbol{Z}_{Aeq} + \boldsymbol{Z}_{t3}\cdot m_3}{\boldsymbol{Z}_{Af3}} - \left(\frac{N3}{N1}\cdot \boldsymbol{I}_{ab1} + \frac{N2}{N1}\cdot \boldsymbol{I}_{ayy1}\right)\cdot \frac{\boldsymbol{Z}_{t3}\cdot m_3}{\boldsymbol{Z}_{Af3}} + \frac{\boldsymbol{E}_{Aeq}}{\boldsymbol{Z}_{Af3}} \tag{A2}$$

$$\boldsymbol{I}_{ab1} = \frac{\boldsymbol{K}_5 \cdot \boldsymbol{K}_9 - \boldsymbol{K}_6 \cdot \boldsymbol{K}_8}{\boldsymbol{K}_4 \cdot \boldsymbol{K}_8 - \boldsymbol{K}_5 \cdot \boldsymbol{K}_7} \tag{A3}$$

$$\boldsymbol{I}_{ab2} = \frac{\boldsymbol{K}_5 \cdot \boldsymbol{K}_9 - \boldsymbol{K}_6 \cdot \boldsymbol{K}_8}{\boldsymbol{K}_4 \cdot \boldsymbol{K}_8 - \boldsymbol{K}_5 \cdot \boldsymbol{K}_7} \tag{A4}$$

$$\boldsymbol{K}_1 = \frac{\boldsymbol{Z}_{t3} \cdot m_3 \cdot \left[\boldsymbol{Z}_{Af3} + \boldsymbol{Z}_{t3} \cdot (1 - m_3) + \boldsymbol{Z}_{C2}\right] + \boldsymbol{Z}_{Af3} \cdot \left[\boldsymbol{Z}_{Af3} + \boldsymbol{Z}_{t3} \cdot (1 - m_3) + \boldsymbol{Z}_{C2}\right]}{\left(\boldsymbol{Z}_{Aeq} + \boldsymbol{Z}_{t3} \cdot m_3\right) \cdot \left[\boldsymbol{Z}_{Af3} + \boldsymbol{Z}_{t3} \cdot (1 - m_3) + \boldsymbol{Z}_{C2}\right] + \boldsymbol{Z}_{Af3} \cdot \left[\boldsymbol{Z}_{t3} \cdot (1 - m_3) + \boldsymbol{Z}_{C2}\right]} \tag{A5}$$

$$\boldsymbol{K}_2 = \frac{\boldsymbol{Z}_{Af3} \cdot \boldsymbol{Z}_{C2}}{\left(\boldsymbol{Z}_{Aeq} + \boldsymbol{Z}_{t3} \cdot m_3\right) \cdot \left[\boldsymbol{Z}_{Af3} + \boldsymbol{Z}_{t3} \cdot (1 - m_3) + \boldsymbol{Z}_{C2}\right] + \boldsymbol{Z}_{Af3} \cdot \left[\boldsymbol{Z}_{t3} \cdot (1 - m_3) + \boldsymbol{Z}_{C2}\right]} \tag{A6}$$

$$\boldsymbol{K}_3 = \frac{\boldsymbol{Z}_{Af3} + \boldsymbol{Z}_{t3} \cdot (1 - m_3) + \boldsymbol{Z}_{C2}}{\left(\boldsymbol{Z}_{Aeq} + \boldsymbol{Z}_{t3} \cdot m_3\right) \cdot \left[\boldsymbol{Z}_{Af3} + \boldsymbol{Z}_{t3} \cdot (1 - m_3) + \boldsymbol{Z}_{C2}\right] + \boldsymbol{Z}_{Af3} \cdot \left[\boldsymbol{Z}_{t3} \cdot (1 - m_3) + \boldsymbol{Z}_{C2}\right]} \tag{A7}$$

$$\boldsymbol{K}_4 = 3 \cdot \boldsymbol{Z}_{ydS1} + \left(\frac{N3}{N1}\right)^2 \cdot \boldsymbol{K}_1 \cdot \boldsymbol{Z}_{Aeq} + \left(\frac{N3}{N1}\right)^2 \cdot \frac{(\boldsymbol{Z}_{t3} + \boldsymbol{Z}_{C2}) \cdot \boldsymbol{Z}_{Beq}}{\boldsymbol{Z}_{Beq} + \boldsymbol{Z}_{t3} + \boldsymbol{Z}_{C2}} + \left(\frac{N3}{N1}\right)^2 \cdot \frac{(\boldsymbol{Z}_{t3} + \boldsymbol{Z}_{C2}) \cdot \boldsymbol{Z}_{Ceq}}{\boldsymbol{Z}_{Ceq} + \boldsymbol{Z}_{t3} + \boldsymbol{Z}_{C2}} \tag{A8}$$

$$\boldsymbol{K}_5 = \frac{N3}{N1} \cdot \frac{N5}{N1} \cdot \boldsymbol{K}_2 \cdot \boldsymbol{Z}_{Aeq} + \frac{N3}{N1} \cdot \frac{N5}{N1} \cdot \frac{\boldsymbol{Z}_{C2} \cdot \boldsymbol{Z}_{Beq}}{\boldsymbol{Z}_{Beq} + \boldsymbol{Z}_{t3} + \boldsymbol{Z}_{C2}} + \frac{N3}{N1} \cdot \frac{N5}{N1} \cdot \frac{\boldsymbol{Z}_{C2} \cdot \boldsymbol{Z}_{Ceq}}{\boldsymbol{Z}_{Ceq} + \boldsymbol{Z}_{t3} + \boldsymbol{Z}_{C2}} \tag{A9}$$

$$\boldsymbol{K}_6 = \boldsymbol{K}_{10} + \boldsymbol{K}_{11} + \boldsymbol{K}_{12} + \boldsymbol{K}_{13} + \boldsymbol{K}_{14} + \boldsymbol{K}_{15} \tag{A10}$$

$$\boldsymbol{K}_7 = \frac{N5}{N1} \cdot \frac{N3}{N1} \cdot \left(\boldsymbol{Z}_{C2} + \boldsymbol{Z}_{C2} \cdot \frac{\boldsymbol{Z}_{t3} \cdot m_3}{\boldsymbol{Z}_{Af3}} - \boldsymbol{Z}_{C2} \cdot \boldsymbol{K}_1 \cdot \frac{\boldsymbol{Z}_{Aeq} + \boldsymbol{Z}_{t3} \cdot m_3 + \boldsymbol{Z}_{Af3}}{\boldsymbol{Z}_{Af3}}\right) + \frac{N5}{N1} \cdot \frac{N3}{N1} \cdot \frac{\boldsymbol{Z}_{C2} \cdot \boldsymbol{Z}_{Beq}}{\boldsymbol{Z}_{Beq} + \boldsymbol{Z}_{t3} + \boldsymbol{Z}_{C2}} + \frac{N5}{N1} \cdot \frac{N3}{N1} \cdot \frac{\boldsymbol{Z}_{C2} \cdot \boldsymbol{Z}_{Ceq}}{\boldsymbol{Z}_{Ceq} + \boldsymbol{Z}_{t3} + \boldsymbol{Z}_{C2}} \tag{A11}$$

$$\boldsymbol{K}_8 = 3 \cdot \boldsymbol{Z}_{ydS2} + \left(\frac{N5}{N1}\right)^2 \cdot \left(\boldsymbol{Z}_{C2} - \boldsymbol{Z}_{C2} \cdot \boldsymbol{K}_2 \cdot \frac{\boldsymbol{Z}_{Aeq} + \boldsymbol{Z}_{t3} \cdot m_3 + \boldsymbol{Z}_{Af3}}{\boldsymbol{Z}_{Af3}}\right) + \left(\frac{N5}{N1}\right)^2 \cdot \frac{\left(\boldsymbol{Z}_{Beq} + \boldsymbol{Z}_{t3}\right) \cdot \boldsymbol{Z}_{C2}}{\boldsymbol{Z}_{Beq} + \boldsymbol{Z}_{t3} + \boldsymbol{Z}_{C2}} + \left(\frac{N5}{N1}\right)^2 \cdot \frac{\left(\boldsymbol{Z}_{Ceq} + \boldsymbol{Z}_{t3}\right) \cdot \boldsymbol{Z}_{C2}}{\boldsymbol{Z}_{Ceq} + \boldsymbol{Z}_{t3} + \boldsymbol{Z}_{C2}} \tag{A12}$$

$$\boldsymbol{K}_9 = \boldsymbol{K}_{16} + \boldsymbol{K}_{17} + \boldsymbol{K}_{18} + \boldsymbol{K}_{19} + \boldsymbol{K}_{20} + \boldsymbol{K}_{21} \tag{A13}$$

$$\boldsymbol{K}_{10} = \boldsymbol{I}_{ayy1} \cdot \frac{N3}{N1} \cdot \frac{N2}{N1} \cdot \boldsymbol{K}_1 \cdot \boldsymbol{Z}_{Aeq} + \boldsymbol{I}_{ayy2} \cdot \frac{N3}{N1} \cdot \frac{N4}{N1} \cdot \boldsymbol{K}_2 \cdot \boldsymbol{Z}_{Aeq} \tag{A14}$$

$$\boldsymbol{K}_{11} = \boldsymbol{I}_{byy1} \cdot \frac{N3}{N1} \cdot \frac{N2}{N1} \cdot \frac{(\boldsymbol{Z}_{t3} + \boldsymbol{Z}_{C2}) \cdot \boldsymbol{Z}_{Beq}}{\boldsymbol{Z}_{Beq} + \boldsymbol{Z}_{t3} + \boldsymbol{Z}_{C2}} + \boldsymbol{I}_{byy2} \cdot \frac{N3}{N1} \cdot \frac{N4}{N1} \cdot \frac{\boldsymbol{Z}_{C2} \cdot \boldsymbol{Z}_{Beq}}{\boldsymbol{Z}_{Beq} + \boldsymbol{Z}_{t3} + \boldsymbol{Z}_{C2}} \tag{A15}$$

$$\boldsymbol{K}_{12} = \boldsymbol{I}_{cyy1} \cdot \frac{N3}{N1} \cdot \frac{N2}{N1} \cdot \frac{(\boldsymbol{Z}_{t3} + \boldsymbol{Z}_{C2}) \cdot \boldsymbol{Z}_{Ceq}}{\boldsymbol{Z}_{Ceq} + \boldsymbol{Z}_{t3} + \boldsymbol{Z}_{C2}} + \boldsymbol{I}_{cyy2} \cdot \frac{N3}{N1} \cdot \frac{N4}{N1} \cdot \frac{\boldsymbol{Z}_{C2} \cdot \boldsymbol{Z}_{Ceq}}{\boldsymbol{Z}_{Ceq} + \boldsymbol{Z}_{t3} + \boldsymbol{Z}_{C2}} \tag{A16}$$

$$\boldsymbol{K}_{13} = \boldsymbol{I}_{byd1} \cdot \left[\left(\frac{N3}{N1} \right)^2 \cdot \frac{(\boldsymbol{Z}_{t3} + \boldsymbol{Z}_{C2}) \cdot \boldsymbol{Z}_{Beq}}{\boldsymbol{Z}_{Beq} + \boldsymbol{Z}_{t3} + \boldsymbol{Z}_{C2}} + \boldsymbol{Z}_{ydS1} \right] + \boldsymbol{I}_{byd2} \cdot \frac{N3}{N1} \cdot \frac{N5}{N1} \cdot \frac{\boldsymbol{Z}_{C2} \cdot \boldsymbol{Z}_{Beq}}{\boldsymbol{Z}_{Beq} + \boldsymbol{Z}_{t3} + \boldsymbol{Z}_{C2}} \quad \text{(A17)}$$

$$\begin{aligned} \boldsymbol{K}_{14} = {} & \boldsymbol{I}_{ayd1} \cdot \left[- \left(\frac{N3}{N1} \right)^2 \cdot \frac{(\boldsymbol{Z}_{t3} + \boldsymbol{Z}_{C2}) \cdot \boldsymbol{Z}_{Ceq}}{\boldsymbol{Z}_{Ceq} + \boldsymbol{Z}_{t3} + \boldsymbol{Z}_{C2}} - \boldsymbol{Z}_{ydS1} \right] \\ & + \boldsymbol{I}_{ayd2} \cdot \left(- \frac{N3}{N1} \cdot \frac{N5}{N1} \cdot \frac{\boldsymbol{Z}_{C2} \cdot \boldsymbol{Z}_{Ceq}}{\boldsymbol{Z}_{Ceq} + \boldsymbol{Z}_{t3} + \boldsymbol{Z}_{C2}} \right) \end{aligned} \quad \text{(A18)}$$

$$\begin{aligned} \boldsymbol{K}_{15} = {} & \boldsymbol{E}_{Aeq} \cdot \frac{N3}{N1} \cdot (1 - \boldsymbol{K}_3 \cdot \boldsymbol{Z}_{Aeq}) + \boldsymbol{E}_{Beq} \cdot \frac{N3}{N1} \cdot \frac{\boldsymbol{Z}_{t3} + \boldsymbol{Z}_{C2}}{\boldsymbol{Z}_{Beq} + \boldsymbol{Z}_{t3} + \boldsymbol{Z}_{C2}} \\ & + \boldsymbol{E}_{Ceq} \cdot \frac{N3}{N1} \cdot \frac{\boldsymbol{Z}_{t3} + \boldsymbol{Z}_{C2}}{\boldsymbol{Z}_{Ceq} + \boldsymbol{Z}_{t3} + \boldsymbol{Z}_{C2}} \end{aligned} \quad \text{(A19)}$$

$$\begin{aligned} \boldsymbol{K}_{16} = {} & \boldsymbol{I}_{ayy1} \cdot \frac{N5}{N1} \cdot \frac{N2}{N1} \cdot \left(\boldsymbol{Z}_{C2} + \boldsymbol{Z}_{C2} \cdot \frac{\boldsymbol{Z}_{t3} \cdot m_3}{\boldsymbol{Z}_{Af3}} - \boldsymbol{Z}_{C2} \cdot \boldsymbol{K}_1 \cdot \frac{\boldsymbol{Z}_{Aeq} + \boldsymbol{Z}_{t3} \cdot m_3 + \boldsymbol{Z}_{Af3}}{\boldsymbol{Z}_{Af3}} \right) \\ & + \boldsymbol{I}_{ayy2} \cdot \frac{N5}{N1} \cdot \frac{N4}{N1} \cdot \left(\boldsymbol{Z}_{C2} - \boldsymbol{Z}_{C2} \cdot \boldsymbol{K}_2 \cdot \frac{\boldsymbol{Z}_{Aeq} + \boldsymbol{Z}_{t3} \cdot m_3 + \boldsymbol{Z}_{Af3}}{\boldsymbol{Z}_{Af3}} \right) \end{aligned} \quad \text{(A20)}$$

$$\boldsymbol{K}_{17} = \boldsymbol{I}_{byy1} \cdot \frac{N5}{N1} \cdot \frac{N2}{N1} \cdot \frac{\boldsymbol{Z}_{C2} \cdot \boldsymbol{Z}_{Beq}}{\boldsymbol{Z}_{Beq} + \boldsymbol{Z}_{t3} + \boldsymbol{Z}_{C2}} + \boldsymbol{I}_{byy2} \cdot \frac{N5}{N1} \cdot \frac{N4}{N1} \cdot \frac{\boldsymbol{Z}_{C2} \cdot (\boldsymbol{Z}_{Beq} + \boldsymbol{Z}_{t3})}{\boldsymbol{Z}_{Beq} + \boldsymbol{Z}_{t3} + \boldsymbol{Z}_{C2}} \quad \text{(A21)}$$

$$\boldsymbol{K}_{18} = \boldsymbol{I}_{cyy1} \cdot \frac{N5}{N1} \cdot \frac{N2}{N1} \cdot \frac{\boldsymbol{Z}_{C2} \cdot \boldsymbol{Z}_{Ceq}}{\boldsymbol{Z}_{Ceq} + \boldsymbol{Z}_{t3} + \boldsymbol{Z}_{C2}} + \boldsymbol{I}_{cyy2} \cdot \frac{N5}{N1} \cdot \frac{N4}{N1} \cdot \frac{\boldsymbol{Z}_{C2} \cdot (\boldsymbol{Z}_{Ceq} + \boldsymbol{Z}_{t3})}{\boldsymbol{Z}_{Ceq} + \boldsymbol{Z}_{t3} + \boldsymbol{Z}_{C2}} \quad \text{(A22)}$$

$$\boldsymbol{K}_{19} = \boldsymbol{I}_{byd1} \cdot \left[\frac{N5}{N1} \cdot \frac{N3}{N1} \cdot \frac{\boldsymbol{Z}_{C2} \cdot \boldsymbol{Z}_{Beq}}{\boldsymbol{Z}_{Beq} + \boldsymbol{Z}_{t3} + \boldsymbol{Z}_{C2}} \right] + \boldsymbol{I}_{byd2} \cdot \left[\boldsymbol{Z}_{ydS2} + \left(\frac{N5}{N1} \right)^2 \cdot \frac{\boldsymbol{Z}_{C2} \cdot (\boldsymbol{Z}_{Beq} + \boldsymbol{Z}_{t3})}{\boldsymbol{Z}_{Beq} + \boldsymbol{Z}_{t3} + \boldsymbol{Z}_{C2}} \right] \quad \text{(A23)}$$

$$\begin{aligned} \boldsymbol{K}_{20} = {} & \boldsymbol{I}_{ayd1} \cdot \left(- \frac{N5}{N1} \cdot \frac{N3}{N1} \cdot \frac{\boldsymbol{Z}_{C2} \cdot \boldsymbol{Z}_{Ceq}}{\boldsymbol{Z}_{Ceq} + \boldsymbol{Z}_{t3} + \boldsymbol{Z}_{C2}} \right) \\ & + \boldsymbol{I}_{ayd2} \cdot \left[- \boldsymbol{Z}_{ydS2} - \left(\frac{N5}{N1} \right)^2 \cdot \frac{(\boldsymbol{Z}_{Ceq} + \boldsymbol{Z}_{t3}) \cdot \boldsymbol{Z}_{C2}}{\boldsymbol{Z}_{Ceq} + \boldsymbol{Z}_{t3} + \boldsymbol{Z}_{C2}} \right] \end{aligned} \quad \text{(A24)}$$

$$\begin{aligned} \boldsymbol{K}_{21} = {} & \boldsymbol{E}_{Aeq} \cdot \frac{N5}{N1} \cdot \left(- \frac{\boldsymbol{Z}_{C2}}{\boldsymbol{Z}_{Af3}} + \boldsymbol{Z}_{C2} \cdot \boldsymbol{K}_3 \cdot \frac{\boldsymbol{Z}_{Aeq} + \boldsymbol{Z}_{t3} \cdot m_3 + \boldsymbol{Z}_{Af3}}{\boldsymbol{Z}_{Af3}} \right) \\ & + \boldsymbol{E}_{Beq} \cdot \frac{N5}{N1} \cdot \frac{\boldsymbol{Z}_{C2}}{\boldsymbol{Z}_{Beq} + \boldsymbol{Z}_{t3} + \boldsymbol{Z}_{C2}} + \boldsymbol{E}_{Ceq} \cdot \frac{N5}{N1} \cdot \frac{\boldsymbol{Z}_{C2}}{\boldsymbol{Z}_{Ceq} + \boldsymbol{Z}_{t3} + \boldsymbol{Z}_{C2}} \end{aligned} \quad \text{(A25)}$$

$$\boldsymbol{I}_{Bac1} = \left[\frac{N3}{N1}\cdot\left(\boldsymbol{I}_{byd1}+\boldsymbol{I}_{ab1}\right)+\frac{N2}{N1}\cdot\boldsymbol{I}_{byy1}\right]\cdot\frac{\boldsymbol{Z}_{t3}+\boldsymbol{Z}_{C2}}{\boldsymbol{Z}_{Beq}+\boldsymbol{Z}_{t3}+\boldsymbol{Z}_{C2}} + \left[\frac{N5}{N1}\cdot\left(\boldsymbol{I}_{byd2}+\boldsymbol{I}_{ab2}\right)+\frac{N4}{N1}\cdot\boldsymbol{I}_{byy2}\right]\cdot\frac{\boldsymbol{Z}_{C2}}{\boldsymbol{Z}_{Beq}+\boldsymbol{Z}_{t3}+\boldsymbol{Z}_{C2}} - \frac{\boldsymbol{E}_{Beq}}{\boldsymbol{Z}_{Beq}+\boldsymbol{Z}_{t3}+\boldsymbol{Z}_{C2}} \tag{A26}$$

$$\boldsymbol{I}_{Cac1} = \left[\frac{N3}{N1}\cdot\left(\boldsymbol{I}_{ab1}-\boldsymbol{I}_{ayd1}\right)+\frac{N2}{N1}\cdot\boldsymbol{I}_{cyy1}\right]\cdot\frac{\boldsymbol{Z}_{t3}+\boldsymbol{Z}_{C2}}{\boldsymbol{Z}_{Ceq}+\boldsymbol{Z}_{t3}+\boldsymbol{Z}_{C2}} + \left[\frac{N5}{N1}\cdot\left(\boldsymbol{I}_{ab2}-\boldsymbol{I}_{ayd2}\right)+\frac{N4}{N1}\cdot\boldsymbol{I}_{cyy2}\right]\cdot\frac{\boldsymbol{Z}_{C2}}{\boldsymbol{Z}_{Ceq}+\boldsymbol{Z}_{t3}+\boldsymbol{Z}_{C2}} - \frac{\boldsymbol{E}_{Ceq}}{\boldsymbol{Z}_{Ceq}+\boldsymbol{Z}_{t3}+\boldsymbol{Z}_{C2}} \tag{A27}$$

$$\boldsymbol{Z}_{Aeq} = \boldsymbol{Z}_{C1}// \left[\boldsymbol{Z}_{t1}\cdot m_1 + \boldsymbol{Z}_{Af1}//\left(\boldsymbol{Z}_{t1}\cdot(1-m_1)+\boldsymbol{Z}_{eq2}//\left\{\boldsymbol{Z}_{t2}\cdot m_2+\boldsymbol{Z}_{Af2}//\left[\boldsymbol{Z}_{t2}\cdot(1-m_2)+\boldsymbol{Z}_{eq1}\right]\right\}\right)\right] \tag{A28}$$

$$\begin{aligned}\boldsymbol{E}_{Aeq} &= \left[\frac{\boldsymbol{E}_{as2}}{\boldsymbol{Z}_{eq2}}+\frac{\boldsymbol{E}_{as1}}{\boldsymbol{Z}_{t2}\cdot(1-m_2)+\boldsymbol{Z}_{eq1}}\cdot\frac{\boldsymbol{Z}_{Af2}//\left[\boldsymbol{Z}_{t2}\cdot(1-m_2)+\boldsymbol{Z}_{eq1}\right]}{\boldsymbol{Z}_{t2}\cdot m_2+\boldsymbol{Z}_{Af2}//\left[\boldsymbol{Z}_{t2}\cdot(1-m_2)+\boldsymbol{Z}_{eq1}\right]}\right] \\ &\cdot\frac{\boldsymbol{Z}_{eq2}//\left\{\boldsymbol{Z}_{t2}\cdot m_2+\boldsymbol{Z}_{Af2}//\left[\boldsymbol{Z}_{t2}\cdot(1-m_2)+\boldsymbol{Z}_{eq1}\right]\right\}}{\boldsymbol{Z}_{t1}\cdot(1-m_1)+\boldsymbol{Z}_{eq2}//\left\{\boldsymbol{Z}_{t2}\cdot m_2+\boldsymbol{Z}_{Af2}//\left[\boldsymbol{Z}_{t2}\cdot(1-m_2)+\boldsymbol{Z}_{eq1}\right]\right\}} \\ &\cdot\frac{\boldsymbol{Z}_{Af1}//\left(\boldsymbol{Z}_{t1}\cdot(1-m_1)+\boldsymbol{Z}_{eq2}//\left\{\boldsymbol{Z}_{t2}\cdot m_2+\boldsymbol{Z}_{Af2}//\left[\boldsymbol{Z}_{t2}\cdot(1-m_2)+\boldsymbol{Z}_{eq1}\right]\right\}\right)}{\boldsymbol{Z}_{t1}\cdot m_1+\boldsymbol{Z}_{Af1}//\left(\boldsymbol{Z}_{t1}\cdot(1-m_1)+\boldsymbol{Z}_{eq2}//\left\{\boldsymbol{Z}_{t2}\cdot m_2+\boldsymbol{Z}_{Af2}//\left[\boldsymbol{Z}_{t2}\cdot(1-m_2)+\boldsymbol{Z}_{eq1}\right]\right\}\right)} \\ &\cdot\boldsymbol{Z}_{Aeq}\end{aligned} \tag{A29}$$

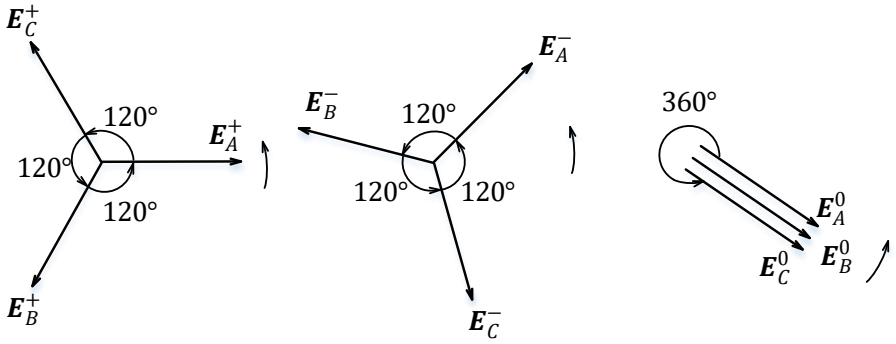
$$\boldsymbol{Z}_{Beq} = \boldsymbol{Z}_{C1}//\left[\boldsymbol{Z}_{t1}+\boldsymbol{Z}_{eq2}//\left(\boldsymbol{Z}_{t2}+\boldsymbol{Z}_{eq1}\right)\right] \tag{A30}$$

$$\boldsymbol{E}_{Beq} = \left(\frac{\boldsymbol{E}_{bs2}}{\boldsymbol{Z}_{eq2}}+\frac{\boldsymbol{E}_{bs1}}{\boldsymbol{Z}_{t2}+\boldsymbol{Z}_{eq1}}\right)\cdot\frac{\boldsymbol{Z}_{eq2}//\left(\boldsymbol{Z}_{t2}+\boldsymbol{Z}_{eq1}\right)}{\boldsymbol{Z}_{t1}+\boldsymbol{Z}_{eq2}//\left(\boldsymbol{Z}_{t2}+\boldsymbol{Z}_{eq1}\right)}\cdot\boldsymbol{Z}_{Beq} \tag{A31}$$

$$\boldsymbol{Z}_{Ceq} = \boldsymbol{Z}_{C1}//\left[\boldsymbol{Z}_{t1}+\boldsymbol{Z}_{eq2}//\left(\boldsymbol{Z}_{t2}+\boldsymbol{Z}_{eq1}\right)\right] \tag{A32}$$

$$\boldsymbol{E}_{Ceq} = \left(\frac{\boldsymbol{E}_{cs2}}{\boldsymbol{Z}_{eq2}}+\frac{\boldsymbol{E}_{cs1}}{\boldsymbol{Z}_{t2}+\boldsymbol{Z}_{eq1}}\right)\cdot\frac{\boldsymbol{Z}_{eq2}//\left(\boldsymbol{Z}_{t2}+\boldsymbol{Z}_{eq1}\right)}{\boldsymbol{Z}_{t1}+\boldsymbol{Z}_{eq2}//\left(\boldsymbol{Z}_{t2}+\boldsymbol{Z}_{eq1}\right)}\cdot\boldsymbol{Z}_{Ceq} \tag{A33}$$

A.3 Symmetrical Components Phasor Diagrams



(a) Positive Sequence (b) Negative Sequence (c) Zero Sequence

Figure A-2 The phasor diagrams of the sequence components of the three phase voltages

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