UNIVERSITY OF BIRMINGHAM

Early failure detection of insulated-gate bipolar transistor semiconductor devices for the power converters of wind turbines

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Abstract

There has been a remarkable increase in the use of wind power generation over the past ten years. However, costly unplanned downtimes caused by reliability issues are a problem. The most common power semiconductor failure mechanisms are bond wire lift off and solder fatigue. Failure detectors should ideally be sensitive enough to detect the early signs of failure and the progress of failure, as well as being applicable during normal operation of a three-phase converter. The junction temperature of an IGBT module has been widely used as a potential failure detector. However, restricting monitoring to purely junction temperature is highly likely to lead to false alarms as the temperature naturally changes with wind conditions. The research in this thesis explores new methods for monitoring the health of IGBTs in an operational wind turbine using a combination of thermal and electrical modelling and a lab-based three-phase converter. The main key findings to the existing knowledge are finding a new method of temperature detection, which is uncoupled with the common failure mechanisms (the bond wire lift-off and solder fatigue) in wind turbines, but also introduce a new temperature estimation method that is uncoupled with progress of the failure.

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مادری دارم بهتر از برگ درخت
به آرامش آب
و به زیبایی یاسی در خواب
می شود وصفش کرد به شکوه یک کوه
به درختی لب رود
مادرم روزگارت پر نور

Notation

ΔT_j	Temperature variations
C_{GC}	Miller capacitance (gate to collector)
C_{GE}	Gate capacitance (gate to emitter)
$\mathrm{I_C}$	Collector current
L_s	Stator inductance
P	Probability
$\mathrm{R_{on}}$	On resistance of IGBT
$R(t)$	Reliability (over period of time t)
$R_{j\_c,th}$	Junction-to-case thermal resistance
R_s	Stator resistance
$t_{d,on}$	Switching on delay time
t_{off}	Switching off time
$t_{d,off}$	Switching off delay time
t_{on}	Switching on time
t_r	Rise time
t_f	Fall time
T_C	Case temperature
T_H	Heatsink temperature
T_j	Junction temperature
T_m	Maximum junction temperature
$T_{j,max}$	Maximum junction temperature
$\mathrm{V_{CE,on}}$	Collector-emitter voltage when IGBT is on
V_{dep}	Depletion layer
V_{GE}	Gate-emitter voltage
V_{GP}	Voltage level of Miller plateau
V_d	Drift region voltage drop

Acronyms

ALC	Aluminium corrosion
BWLO	Bond wire lift off
CM	Condition monitoring
CMS	Condition monitoring system
DCB	Direct copper bonded
DFIG	Direct fed induction motor
ETDS	Electrical train drive system
FOC	Field oriented control
GSc	Grid-side controller
GSC	Grid-side converter
IGBT	Insulated gate bipolar transistor
MPPT	Maximum power point tracking
MTTR	Mean time to repair
MTTF	Mean time to failure
MTBF	Mean time between failures
PI	Proportional-integral
PMSG	Permanent magnet synchronous generator
PMSM	Permanent magnet synchronous machine
PWM	Pulse width modulation
RPM	Revolutions per minute
RSc	Rotor-side controller
RSC	Rotot-side converter
SF	Solder fatigue
SEGR	Single Event Gate Rupture
TDDB	Time-Dependent Dielectric Breakdown
TSR	Tip speed ratio
WT	Wind turbine

Original research articles

1. **R. Moeini**, P. Tricoli, H. Hemida and C. Baniotopoulos, *"Effect of wind speed variations on accuracy of healthy monitoring system used in power electronic converter of wind turbines"*. **In preparation.**
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Chapter 1: Introduction

1.1 Motivation for this research

Wind power is ranked first as a source of power generation amongst renewable power sources [1]. In 2018, wind power generation accounted for 14% out of 362 TWh total generated energy in the EU [2]. Investment in wind power is growing annually as shown in Figure 1.1. A majority (63%) of new power capacity investment is allocated to wind power, with 160 GW onshore wind turbines (WT) and 18.5 GW offshore WT, with investments of, respectively, €16.3 bn and €10.3 bn [2]. The sharing of investment for the new installation capacity is shown in Figure 1.2.

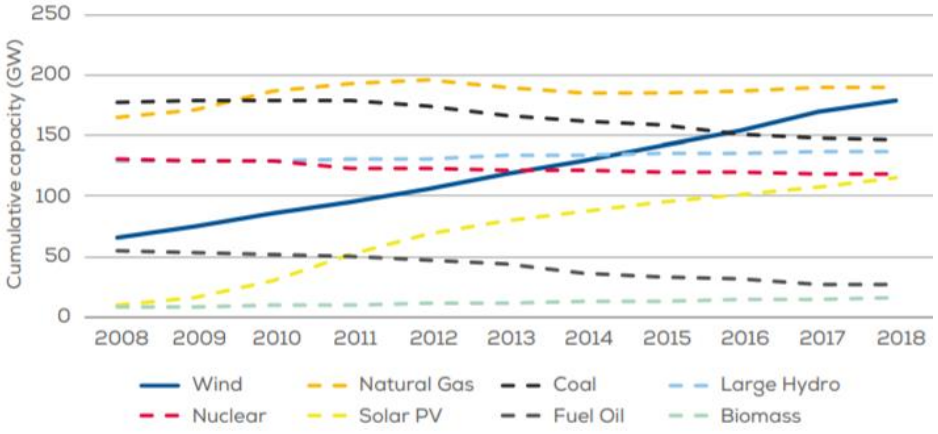


Figure 1.1: The cumulative growth of wind power capacity in Europe [3]

The next highest power capacity investment after wind is photovoltaic (PV) followed by biomass with about 8 GW (39 %) and 1.1 GW (5 %) with respective investments of €10.4 bn and €1.9 bn [3]. Fossil fuel is ranked as the lowest with only a 4 % share [4].

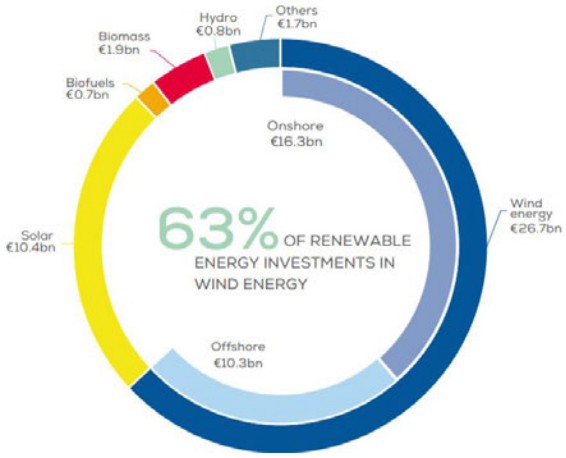


Figure 1.2: Renewable power capacity investments in Europe in 2018 [3]

The generated wind power is highly related to the availability of wind resources. In fact, during peak demand days (winter) up to a third of the energy consumption is serviced by WTs. The wind energy harvesting in urban areas is not straightforward due to lower wind speed resources in comparison with a hilly areas and coastal plains. Being far from urban area increases installation and maintenance costs such as foundations, substations and subsea cables for offshore WTs. In addition, the operation and maintenance (O&M) of WTs contribute a large cost overhead during the wind-farm lifetime. Figure 1.3 shows the capital expenditures associated with an offshore wind farm.

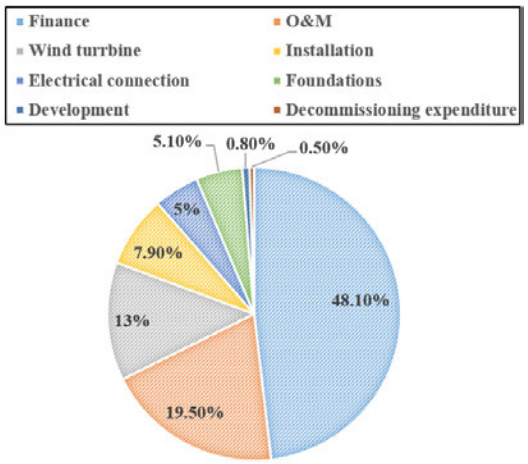
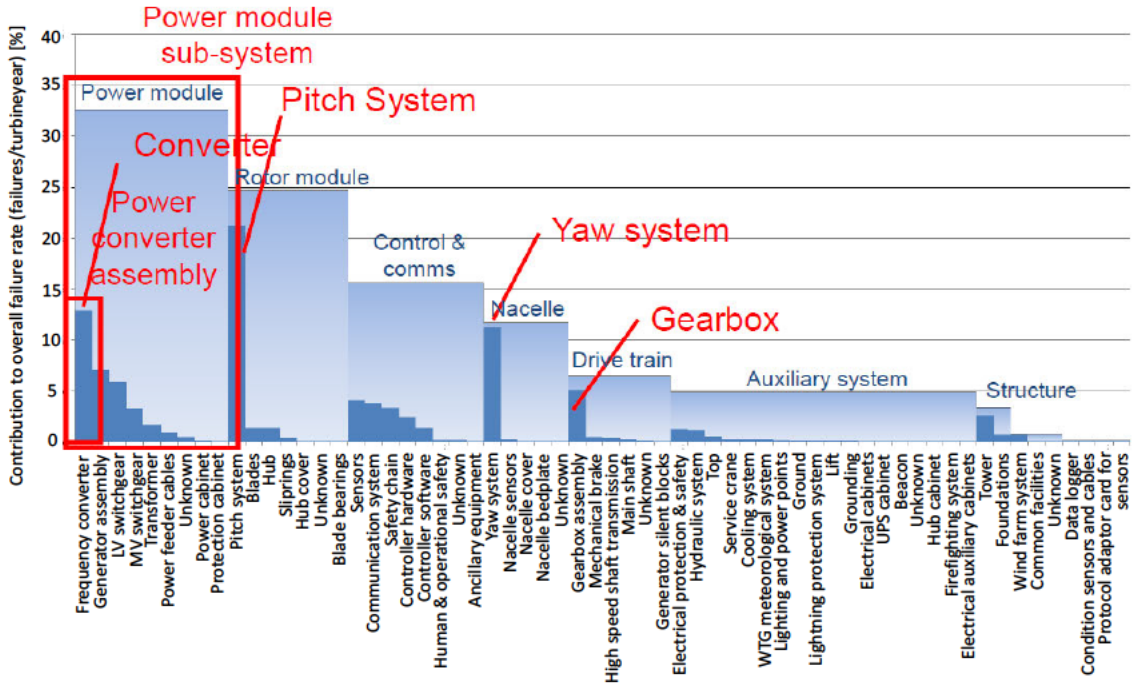


Figure 1.3: Financing costs of an offshore farm in 2015 [5]

'Operation and maintenance' (O&M) is the second largest expenditure (19.5%) with maintenance accounting for 65% of this cost [5]. O&M costs prolong the payback period of WTs [6]. Thus, it is more economically challenging to use a WT as an alternative source of power in remote or difficult locations. Enhancing the reliability of WTs can contribute to a reduction in maintenance costs by reducing the frequency of maintenance visits.

The drivetrain of a WT is a major contributor to the overall maintenance costs. Factors influencing maintenance costs include insurance, design reliability, transport and repair. Among these, design reliability can be improved by the manufacturer. However, it is not possible to achieve a 100% reliable design. Health condition monitoring of critical parts of WTs during operation can increase the chance of observing or detecting precursors to failure and assist in preventing catastrophic failures and reducing operational downtime.

The graph in Figure 1.4 shows the percentage of various failure rates seen in WTs. The highest failure rates in the WT electrical drive train have been experienced in power modules (35%). The pitch system has also experienced relatively high failure rates, 20% [7]. Figure 1.5 shows the overall downtime in different parts of WTs. The power converter contributes the maximum downtime in WTs.



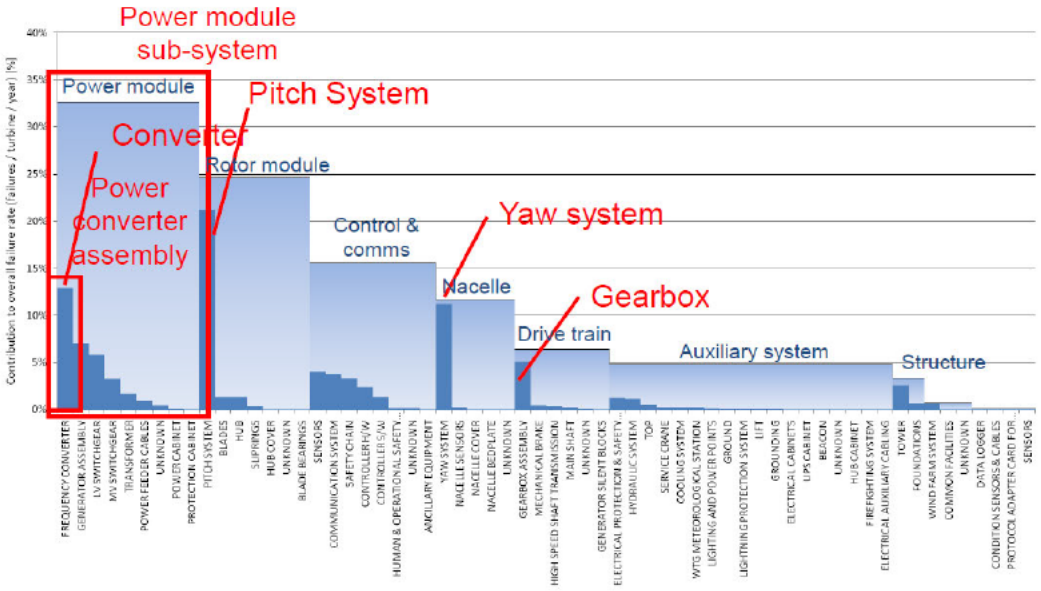


Figure 1.4: Statistical figures for overall failure rates for 350 WTs [8

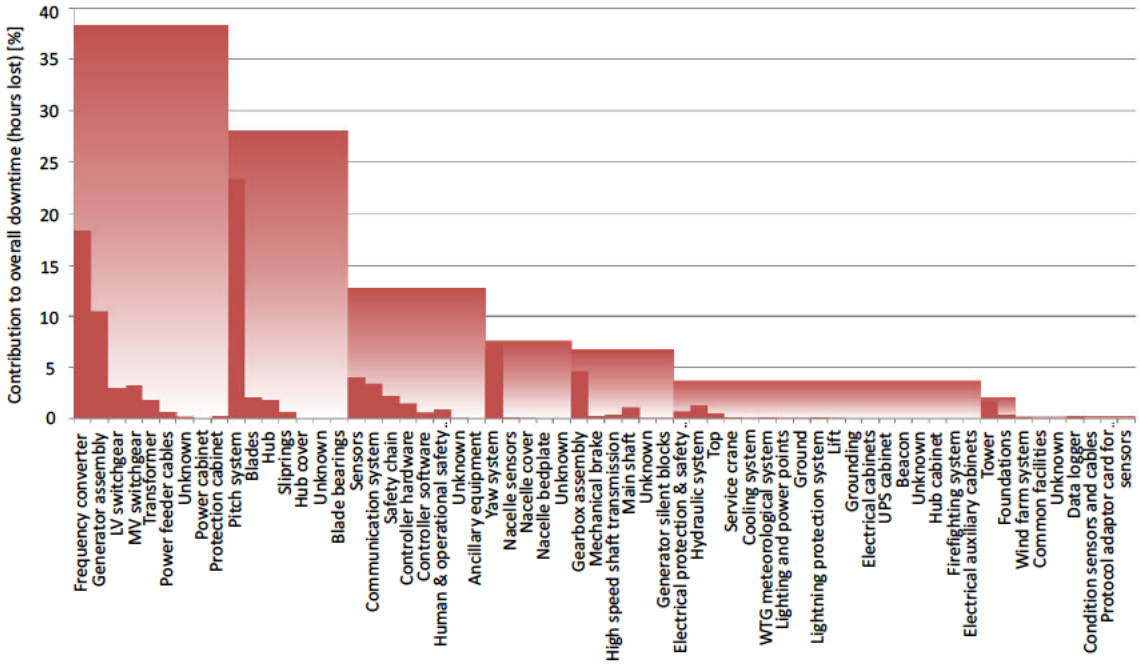


Figure 1.5: Statistical figures of overall downtime for 350 WTs [8]

Statistical figures show that electrical systems contribute the majority of downtime and WT failures [8]. The electrical systems consist of generators, power converters and various control systems (such as yaw controller, pitch controller, speed controller, MPPT, rotor side controller, grid side controller). A power converter consists of various component types: semiconductor devices, gate drivers, direct current (DC), DC-link capacitor, resistive and inductive filters, switchgear and a controller. Figure 1.6 shows the typical downtime rates for these parts. Power semiconductor devices suffer the higher rate of failures

(31%), followed by capacitors (20%), and gate drivers (19%). Together these three components make up over half of all failures. Clearly, improving the reliability of the power electronic converters will lead to higher availability of the electrical drive train and hence to reduced downtime of WTs.

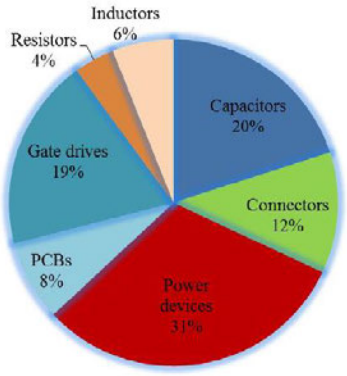


Figure 1.6: Distribution of electrical component failures in a WT electrical drive train system [9]

Insulated gate bipolar transistors (IGBTs) are widely used as the semiconductor devices in the power converters owing to their low power losses while carrying high currents at high voltages in comparison with MOSFETs due to the width of their channel region (although at lower voltages a MOSFET has a lower on resistance as the channel region is narrower). However, semiconductor power electronics components are sensitive to temperature and electrical stresses. IGBTs show the highest failure rate amongst converter components [10].

Thermal and electrical stresses mainly originate from load fluctuations that accelerate the degradation of the IGBTs. Because of the variability of wind speed, such stresses frequently arise in WTs and thus there is an interest in improving the reliability. Reliability here refers to the probability that a system will pass a target performance by yielding correct output over the desired lifetime. In other words, WT reliability refers how well a system can perform. As described, the reliability of the IGBT plays a significant role in reducing the downtime of the power electronic converters and hence increasing the converter availability and in turn the WTs. Availability refers to the percentage of time that a system remains operational under normal circumstances. Especially for critical applications where there are unpredictable load conditions. Unpredicted failure causes loss of energy generation and requires unplanned maintenance with consequent downtime. Unplanned maintenance in wind farms results in a high cost penalty [11]. Failure causes unplanned interruption to the power generation and generates unexpected costs.

Maintenance costs of WTs are often significant because of their remote locations. For example, the UK offshore WTs have a reported capacity factor of 50%. Based on this, the turbine expected power for a 5 MW offshore WT per day is 60 MWh. Considering the average base level energy generation price is about £140 per MWh, that equates to £8400 per day [12-13]. Conversely, this figure can be seen as the

daily lost revenue for each non-working 5 MW WT. Maintenance cost is at least £5k for a vessel and one expert human resource. The reported average downtime associated with an offshore WT is 5 days per fault [14]. This is due to remote location of WT, providing the components and organising the trip 5 days×£8400=£42k and plus the maintenance cost (£5k) can be £47k in total.

The typical cost of a WT controller and the health condition monitoring system (from Bachmann and Mita Teknik) is £70k per WT [15]. Considering that a wind farm with 20×5 MW turbines can experience a power converter failure every 2 years (the wind measurement & evaluation programme (WMEP) database specifics to 1.5 electrical failures per WT annually). The licensing of the monitoring system is £4k and sensor replacement costs £1k per WT. From these figures it can be concluded that a health condition monitoring system adds to the complexity and cost of running a WT. However, considering the average WT downtime and relatively low cost of a monitoring system, even if the system prevents one unplanned shutdown the additional system cost will be paid back [16].

Some efforts at the design stage can improve IGBT availability, such as improving the system architecture by including a fault tolerant design. In order to grow the popularity of WTs compared with fossil fuels, it is essential to minimise downtime costs and predict the requirement to replace the parts and hence optimise the maintenance schedule. Health condition monitoring of electrical, mechanical and structural components of a WT has the potential to address this issue [16]. To apply and develop an effective health condition monitoring system, a better understanding of the mechanisms underpinning the progress of damage is essential. A health condition monitoring system refers to the normal set of activities that contribute to the observation of instantaneous state of health of the system/device under study. By the addition on condition monitoring, the maintenance schedule and repair time will be improved. It is important to note that a condition monitoring system does not influence the lifetime or reliability of a component but rather indicates a requirement for the replacement of a degraded component before total failure occurs.

1.2 Overview of research methodology

- Calibration of $V_{CE,on}$ against variations in T_j and i_c has been carried out in healthy mode by applying one short pulse in a controlled junction temperature condition.
- Thermo-electrical modelling of the IGBT is done to determine temperature rise in each layer. The IGBT transient thermal model has been tuned based on the experimental results. The same amount of heat flow has been applied to the IGBT model. The case temperature (T_c) and substrate temperature ($T_{substrate}$) predicted by the thermo-electrical model are compared with the measured T_c and $T_{substrate}$ values.

- To detect the progress of SF, the thermal resistance of the junction to case has been estimated by using Joule heating rules. Power losses are calculated by using a 2D look up tables for conduction power losses and a 3D look up table for switching power losses.
- A 15% increase in R_{th} compared to $R_{th,cal}$ can represent the presence of SF.
- $V_{CE,on}$ is measured with a voltage differential amplifier. The $V_{CE,on-measured}$ is also compared with $V_{CE,cal}$. Deviations can represent the presence of bond wire lift-off.
- T_j is estimated from the switching off time (t_{off}). Time t_{off} is defined as the interval from V_{GE} at 90% to when i_c reaches 10%. To provide the measurement of 90% of V_{GE} and 10% of i_c, a state machine process has been developed.
- A wind profile has been applied to the rotor side converter – numerically modelled in Simulink to investigate the effect of the fundamental frequency and load amplitude on the IGBT.

1.3 Problem statement

- Proposing effective failure detectors that are sensitive to the progress of the failures and feasibly employable to measure within the operation of three-phase converter.
- Processing the data corresponding to the switching times and developing an accurate state machine to find out 90% and 10% points in i_c and V_{GE}.
- Proposing a temperature estimator to be independent of the progress of BWLO.
- Finding the effect of wind speed variations on the failure detectors and junction temperature.

1.4 Aim of this research and objectives

The main aim of this Ph.D is to investigate the fault detection of an IGBT used in a WT, bearing in mind the wind speed variations. A list of objectives is given below:

O1. To find out what are the issues for the existing approach.

O2. To propose effective electrical failure detectors that are sensitive to the progress of the failures and can be feasibly calibrated in healthy and unhealthy states of the IGBT.

O3. To find an appropriate method of processing the measured data corresponding to the electrical failure detectors and also to validate the measured data.

O4. To develop a thermal model of an IGBT in order to find its thermal resistance and thermal behaviour.

O5. To generate a temperature estimator that is independent of the progress of BWLO in order to independently measure temperature variations from failure.

O6. To measure and detect early failure mechanisms within the operation of a three-phase converter by the proposed electrical failure detectors.

O7. To numerically model the WT in order to understand the effect of wind speed variations on IGBT.

1.5 Original research contributions

With respect to failure detection for an IGBT module used in the power electronic converters, the main research contributions to existing knowledge are listed below:

1. Developed a state machine to process switching times within operation of a three-phase-converter.
2. Developed an 'in-situ' measurement technique to detect premature failures; with an accuracy of detection of one wire lift-off. The technique is practically applicable to WT applications.
3. Developed a temperature estimator that is independent of the progress of failure.
4. Developed an algorithm that can detect common early failure mechanisms.

1.6 Thesis outline

The thesis is structured to show in detail how the objectives in section 1.4 and the research contributions given in subsection 1.5 have been achieved and how. Chapter 2 provides a brief background on WT electrical drive train systems, power converters and most specifically the IGBT structure and various associated failure modes. Chapter 3 reviews previous research on failure detectors and health condition monitoring technologies to identify gaps in the research knowledge, allowing identification of the specific research to be undertaken for this thesis. Chapter 4 presents the design of the laboratory prototype of a power electronic converter controller.

Chapters 5 and 6 contain the experiment results from detection of a failure mechanism in an IGBT and the corresponding setup. The sensitivity of the proposed failure detectors to the two different failure mechanisms, namely BWLO (Chapter 5) and SF (Chapter 6), are studied and discussed for the calibration setups and in an operating three-phase converter. Chapter 7 presents the WT numerical model, in accordance with the experimental setup presented in the next chapter. Chapter 7 also contains an electrical model of the WT power train using a real wind profile to assess the effects of wind speed variations on IGBT performance. Chapter 8 is a detailed discussion of the outcomes of the research, together with specification of the key contributions to knowledge (novelty) of the work. Chapter 9 concludes the thesis and proposes possible future studies to allow exploitation of this research.

1.7 References

[1] M. Bhattacharya, S.R. Paramati, I. Ozturk and S.Bhattacharya "The effect of renewable energy consumption on economic growth: Evidence from top 38 countries", Applied energy. Springer Inter Publishing, pp. 733-741, Vol.162, 15th Jan 2016.

[2] C. Walsh, and I. Pineda, Wind energy in Europe in 2018. Trends and statistics, in 2019 available at https://windeurope.org/wp-content/uploads/files/about-wind/statistics/WindEurope-Annual-Statistics-2018.pdf

[3] G. Resch, et al. "Assessment of Policy Pathways for Reaching the EU Target of (At Least) 27% Renewable Energies by 2030", The European Dimension of Germany's Energy Trans. Cham: Springer Inter Publishing, pp. 45–65, 2019, doi: 10.1007/978-3-030-03374-3_4.

[4] M. Aly, E. Ahmed, and M. Shoyama, "Thermal and Reliability Assessment for Wind Energy Systems With DSTATCOM Functionality in Resilient Microgrids," IEEE Transon Sustainable Energy, vol. 8, no. 3, pp. 953 - 965, Dec, 2016.

[5] Shipurkar, "Improving the availability of WT generator systems", 2019.

[6] WindEurope Report, 201, in 2018. available at https://windeurope.org/wp-content/uploads/files/about-wind/statistics/WindEurope-Annual-Statistics-2018.pdf [7] EREC, 'Renewable energy technology roadmap 20% by 2020'.

[8] M. Wilkinson and B. Hendricks, "Reliawind Deliverable D.1.3 Reliability Profiles Results," 2007.

[9] P. Tavner, B. Hahn, S. Faulstich, "Eliability & availability of WT electrical & electronic components', Jan 2011.

[10] Y.Avenas, L.Dupont and Z.Khatir "Temperature Measurement of Power Semiconductor Devices by Thermo-Sensitive Electrical Parameters-a review", IEEE Trans on Power Electro, Vol.27, (6), Jun 2012, pp. 3081-3092.

[11] GL Garrad Hassan, "A guide to UK offshore wind operations and maintenance," Scottish Enterp. Crown Estate, p. 42, 2013.

[12] S. Konaklieva "Power Module Condition Monitoring for Offshore Wind Applications with Focus on the Die Attach Degradation" PhD thesis, University of Warwick, 2017.

[13] L. Ran, S. Konaklieva, P. McKeever and P. Mawby, "Condition Monitoring of Power Electronics for Offshore Wind" DOI: 10.1049/etr.2014.0004, IET journal in Engineering & Technology, 2014.

[14] L. Ran, S. Konaklieva, P. Mawby, and P. McKeever, "Condition Monitoring of Power Electronics for Offshore Wind", IEEE Trans, Jun 2014, pp 1–10.

[15] The Crown Estate, "A Guide to an Offshore Wind Farm," 2010.

[16] S. Sheng, “NREL/PR-5000-59111,” NREL, Jun 2013, available at https://www.nrel.gov/docs/fy13osti/59111.pdf.

[17] R. Moeini, P. Tricoli, H. Hemida and C. Baniotopoulos, “Increasing the reliability of WTs using condition monitoring of semiconductor devices: a review”, IET, RPG conf, Sept 2016.

Chapter 2: Review of condition monitoring of power converters for wind turbines

2.1 Introduction

WTs convert a proportion of the kinetic energy of wind into electrical energy using electrical generators [1]. The electrical systems and control algorithms used to convert the wind energy to electricity are discussed in this chapter. Due to wind speed variations, WT electrical systems will encounter diverse load swing variations. These load swings will reduce in the expected lifetime of the semiconductor 'power-switch' component (IGBT), used in the power converters. The ability of the lifetime can result in an unplanned halting of the system. Health condition monitoring can help to identify premature failure of the IGBT and predict the time remaining to failure. To design and implement an effective condition monitoring system it is essential to understand failure mechanisms and their root causes. The structure of IGBTs and different failure modes are discussed in this chapter.

2.2 Electric drive train system of a wind turbine

Wind energy passing a WT causes the blades to produce torque on a main shaft that is then converted into electrical power. The main WT shaft rotates the rotor of an electrical generator either directly, or indirectly by means of a gearbox. The foundations, the design of the blades and the mechanical structure of the WTs are not of concern in this thesis. The main electrical drive system mainly comprises the generator, power electronic converters and their controller systems, an electric breaker, pitch angle controller, yaw motor and its driver and actuator. The focus of this thesis is on the electrical drive train system and most specifically on the power electronic converters and their control system. This is because the control system defines the operation strategy of the power converter. For example, the pitch angle controller can keep the generated power constant, so constant thermal stresses are applied to the IGBTs of the power converter despite changes in wind speed; this will discussed further in chapter 7. This subsection describes the electrical parts of the electrical drive train of WT in terms of efficiency

and potential maintenance costs. The drive train system of the WT is located in a nacelle that houses all of the generating components in a WT. The nacelle is connected to the hub where the blades are attached. The drive train can be divided into two sections: the mechanical and electrical drive system [2], shown in Figure 2.1.

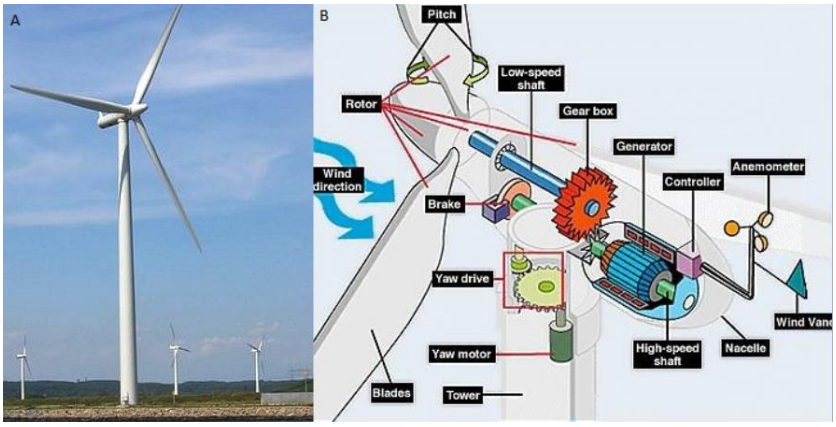


Figure 2.1: A horizontal axis WT (left) and schematic of the turbine's blade assembly and nacelle (right) [3]

2.3 Electrical drive system of wind turbines

Three types of electrical power generator are typically found in WTs:; squirrel-cage induction generators (SCIGs); doubly-fed induction generators (DFIGs); and permanent magnet synchronous generators (PMSGs). They are classified in Figure 2.2.

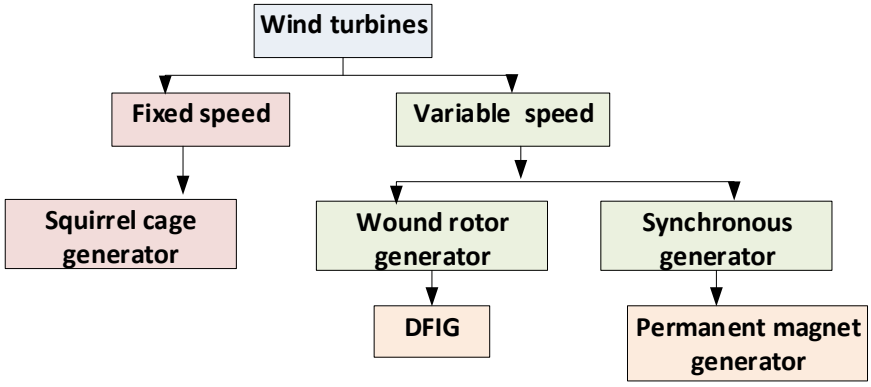


Figure 2.2: Most common classification of WT according to their generator types

2.3.1 Fixed-speed wind turbines

SCIGs without power electronic converters are used for fixed-speed WTs directly connected to the grid [4]. A block diagram of this type of WT is shown in Figure 2.3. The SCIG speed can change by only a few percent because the torque-speed characteristic of SCIGs is steep around the synchronous speed, so the pull-out torque (that guarantees stability) is close to the synchronous speed.

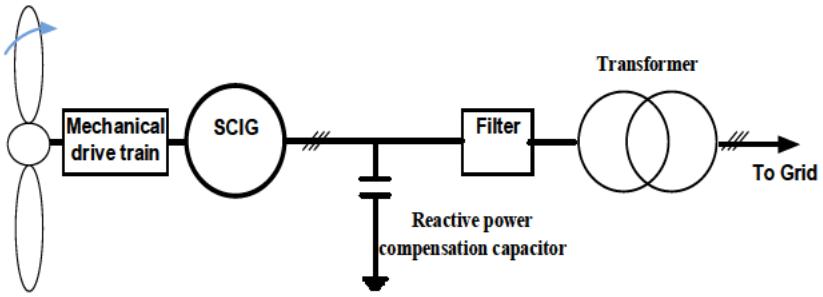


Figure 2.3: Diagram of fixed-speed WTs, using SCIG

The drivetrain consists of a mechanical section (a variable-ratio gearbox and a mechanical breaker) and an electrical section (electrical generator, reactive power compensator and transformer). The generator requires a higher shaft speed than the WT rotor produces so a gearbox is required. The gearbox is essential because wind speed variations lead to mechanical rotational speed fluctuations and thus to variations in electrical power output. These variations yield voltage fluctuations at the point of connection to the grid. Fixed-speed WTs draw varying amounts of reactive power from the grid. Therefore, in these types of WT, a capacitor bank is used to compensate reactive power.

The fixed-speed type of WT is cost-effective, especially for small and medium systems. However, its best efficiency (optimum tip speed ratio) occurs over a rather limited range of wind speeds [5]. The tip-speed ratio 'λ' for a WT is the ratio between the tangential speed of the tip of WT blade and the actual speed of the wind speed (v). The tip-speed ratio is related to efficiency, with the optimal value varying with blade design in equation (2.5). Furthermore, a fixed-speed WT requires an electrically stable grid as a load and the mechanical drive train needs to withstand the high mechanical stresses caused by wind gusts and turbulent flow.

$$\lambda = \frac{\omega.R}{v} \tag{2.5}$$

where v is the wind speed, R is the rotor radius and ω is the rotational speed.

2.3.2 Variable-speed wind turbines

Variable-speed WTs can operate at peak electrical efficiency over a wide range of wind speeds. Both asynchronous and synchronous generators can be used for these types of WT in combination with back-to-back power converters (AC to DC and DC to AC converters). The use of a back-to-back converter enables a WT to maximise the generated electrical power by implementing maximum power point tracking (MPPT) strategies [6]. To extract maximum power from the wind (between cut-in and rated speed) the WT shaft speed is varied so that the optimum tip-speed ratio is achieved. MPPT is a control strategy that is applied when the wind speed is equal or below the rated speed of the WT by generating appropriate reference voltage for DC power bus voltage before the DC to AC converter associated with

the wind speed. WTs have to be designed to withstand extreme wind speeds that will naturally occur from time to time.

A WT can survive in a storm, but the blades do not turn and no electricity is generated. Indeed, if the wind speed exceeds the cut-out speed for the WT, brakes are applied to bring the WT blade rotation to a halt. Wind speed is measured with the anemometer located at the top of the WT nacelle. At wind speeds between the rated and cut-out speeds, two methods can be used to control the power. One is the active 'pitch controller' method and the other is the passive stall/'soft stall' method, also known as active stall. Figure 2.4 illustrates the power output for the two types of pitch control. The purple dashed line links the maximum power points for each speed.

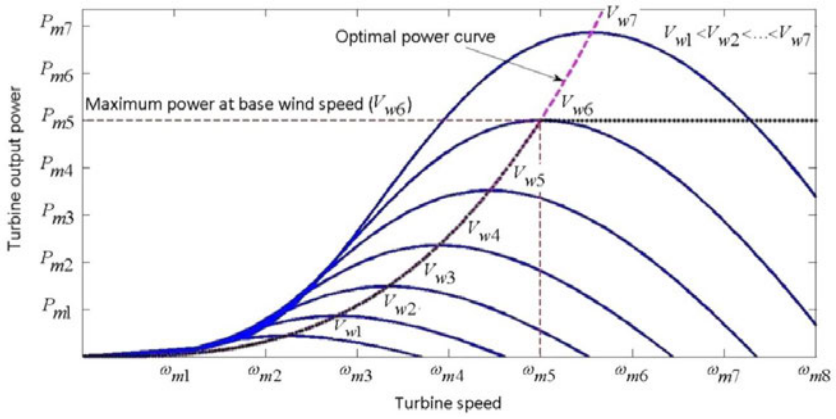


Figure 2.4: Power control in different range of wind speed [7]

The presence of a pitch controller means that there is a control system that can vary the pitch angle of turbine blades so as to decrease the torque produced by the blades in a fixed-speed turbine or to decrease the rotational speed in variable-speed turbines. Power output can be kept at the rated power by adjusting the pitch angle of the blades [8]. When the wind speeds are above the rated speed (but below the cut-out speed), the blades will rotate so that there is less lift and more drag due to increasing flow separation along the blade length. This will slow down the rotational speed or the torque transferred to the shaft so that the rotational speed or the torque is kept constant below a set threshold. A WT with a pitch controller increases its power output with increasing wind speed, up to the rated wind speed, then as the wind speed increases to the cut-out speed, the pitch is controlled and the power remains constant. The pitch controller communicates with the converter controller to monitor the generator speed and power output. A reference pitch angle is determined based on the generator speed and average wind speed. The output of the pitch angle controller is fed to a mechanical drive system to adjust the blade pitch angle through actuators.

A passive stall system is a control system where the blades are designed so that when wind speed is too high, the rotational torque is automatically reduced by aerodynamic effects. The power decreases with

increasing wind speeds due to aerodynamic effects on the turbine blades (regions of the blade are stalled, transmitting from the hub and outwards with increasing wind speeds). Blades are designed so that they will perform with inferior quality (in terms of energy extraction) in higher wind speeds to protect the WT without requiring active controls [9]. Active stall/soft stall refers to when the rotor speed is actively regulated to ensure a reduction of the torque. Power electronic converters are used (where required) to connect power generated by the WT generator to the grid supply via a transformer. Power electronic converters have two stages with an intermediate DC-link [10]. A block diagram in Figure 2.5 shows a typical variable-speed WT. The two converters communicate with each other and with the grid to keep the DC-link voltage constant.

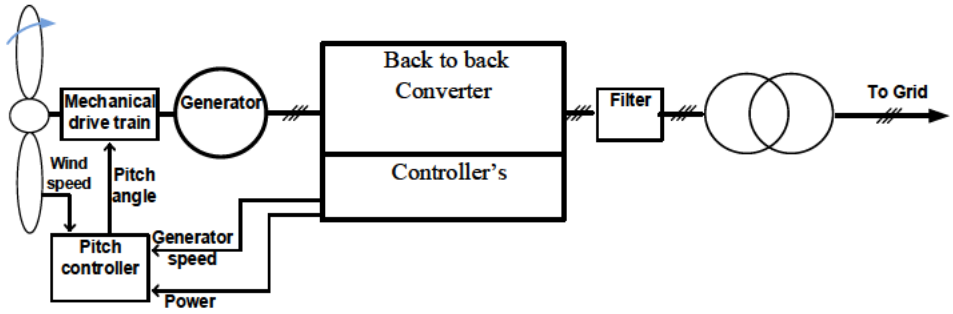


Figure 2.5: Simplified block diagram of variable speed WTs including back-back converter

Two important control functions are carried out by the AC to DC converter, and two others by the DC to AC converter. The DC to AC converter, the grid side converter, controls the DC-link voltage and the reactive power exchanged with the grid. The AC to DC converter, the rotor side converter, controls the torque and flux of the generator. DFIGs and PMSGs are used for variable-speed WTs [11]. Both DFIG and PMSG types are combined with power electronic converters to generate electrical power with a larger range of wind speeds than a fixed-speed WT. Power electronic converters also help to satisfy grid regulations (synchronous frequency and voltage regulation requirements) when integrating with the grid. DFIGs are more efficient for high, steady wind conditions, but have lower efficiency at low speeds as more current must be injected into the rotor [12]. A brief explanation of different types of WTs are given in the following subsections, including a discussion of their advantages and limitations.

2.4 DFIG type of wind turbine

DFIG is commonly found in variable speed WTs produced since the late 1990's. Currently, 57.5% of the variable WTs are equipped with DFIG [13]. Vesta V90, Gamesa G80 and GE1.5 models are examples of this type of WT [14]. DFIG is also extremely popular to use in medium power WTs, rated below 2 MW. The electric drive train of a WT with a DFIG is shown in Figure 2.6. A DFIG has a stator winding that is directly connected to the grid, while the rotor windings are supplied by a power converter. For this reason, this type of generator is called 'doubly-fed' because both stator and rotor

windings are energised. The "opti-slip" feature allows the generator to have a variable slip and to choose the optimum slip, reducing fluctuations of the torque and power output [15].

The rated power of the power electronic converter is smaller for this type of WT than that found in a PMSG or SCIG with similar power. The reason is that the converter is connected to the rotor which typically only sees 30% of the generator rated power [16]. When the stator excitation is applied, a voltage will be generated at the output terminals of the rotor circuit. The rotor-side converter (RSC) provides the excitation for the induction machine. With this converter it is possible to control the torque and hence the speed of the DFIG and also the power factor at the stator terminals. The rotor-side converter provides a varying excitation frequency depending on the wind speed. In a DFIG designed for high-speed, a slow-turning shaft from the rotor (10-20 rpm) drives a gearbox with its output shaft rotating up to 2000 rpm, and this drives the generator. This type of WT is equipped with a gearbox [17].

The gearbox is used to convert low speed rotations from the rotor shaft to the higher speed rotation that is required to generate initial torque for the induction generator. Generally, the DFIG requires a gearbox to adjust the generator speed so that tip speed ratio is kept constant at MPPT. Using a gearbox adds to the maintenance costs of the SCIG and DFIG WTs. These requirements and limitations mean turbine manufacturers have been recently looking to PMSG technology as the most promising type for medium and low power WTs [18].

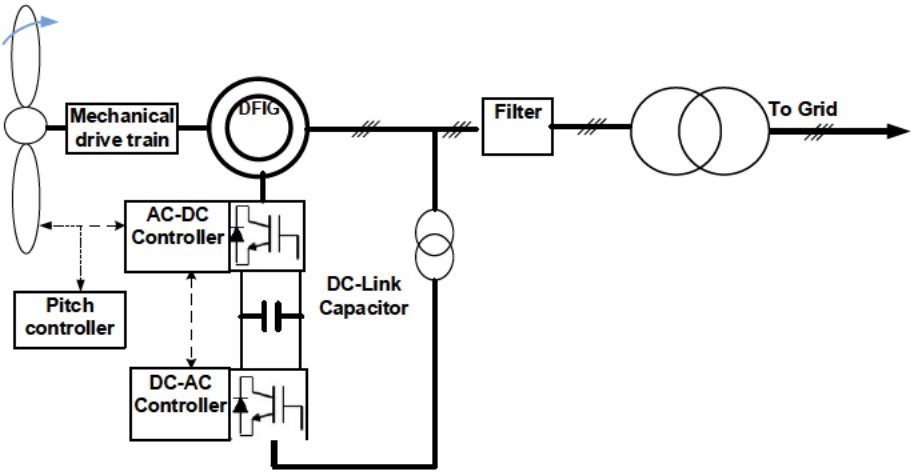


Figure 2.6: Diagram of a variable speed WT with a DFIG

2.5 PMSG type of wind turbine

PMSGs are becoming increasingly popular amongst manufacturers as they are looking to enhance the reliability and serviceability of WTs by avoiding the need for a gearbox. Currently almost 40% of WTs are equipped with PMSGs [19]. The largest manufacturer of this type of electrical drive train system are Enercon and Gold Wind [20]. For medium power WTs, (2-3 MW) direct drive using PMSGs is

extremely popular. However, they are less popular for larger WTs because of their requirements for large and expensive rare earth NdFeB magnets.

It should also be noted that the power efficiency and density of PMSGs are remarkably higher than those of SCIGs and DFIGs as there is no need for an excitation current. An electrical drive train system of this type is shown in Figure 2.7. The power electronic converter is connected to the stator winding and the electrical machine is excited by its rotor magnets.

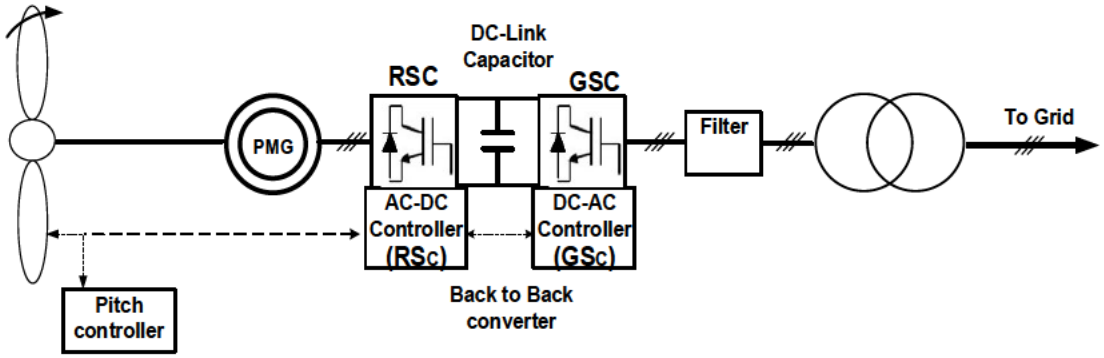


Figure 2.7: Diagram of a variable speed WT with a PMSG

For a PMSG there is no need for any excitation current since the magnetic field is generated by rotor magnets. Comparing the DFIG type to a PMSG, the DFIG is more economical because of the smaller rated power of power electronic converters and the absence of permanent magnet materials. However, PMSGs can be controlled more easily to cope with a wide range of wind speeds while controlling reactive power. In fact, for a PMSG reactive power can be fully adjusted for all speeds, whereas the reactive power in a DFIG is determined by wind speed.

2.6 IGBT module

All embedded controllers in the converters and pitch angle controllers are integrated through controlling pulse signals sent to active semiconductor devices, such as insulated gate bipolar transistors (IGBTs). These switches can be switched 'on' and 'off' to set the electric drive train systems output to the desired voltage and frequency. This section gives some details of the power semiconductors typically found in WT power converters. IGBTs are the semiconductor devices of choice for high voltage applications due to their low on-state losses [21]. For a gate voltage below the threshold value, (typically in a range of 8-10 V), IGBTs do not conduct any significant current and, hence, they are off. Above the threshold value, the control current varies based on the gate voltage. Rated current is conducted when the gate voltage reaches approximately 12-15 V. It takes some time for IGBTs to transition from off-to-on and on-to-off. Internal capacitances of IGBTs affect the 'turn-on' and 'off' times of the IGBTs. These transition times, called the turn-on and turn-off times, are important for power losses (see chapters 5

and 6). IGBTs have three terminals: the ‘gate’, ‘collector’ and ‘emitter’. The equivalent circuit of an IGBT is shown in Figure 2.8 [22].

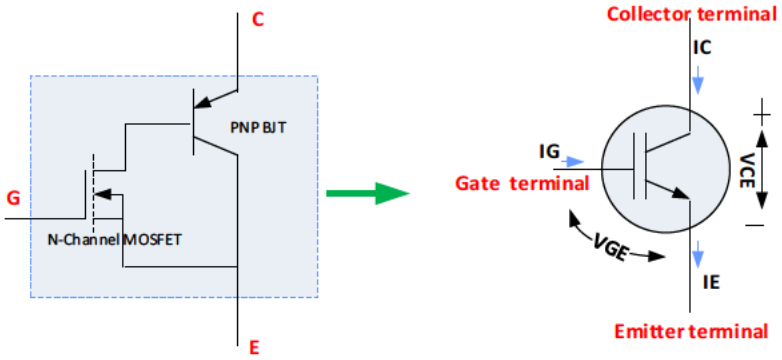


Figure 2.8: An N-channel IGBT equivalent circuit

2.7 IGBT structure

IGBTs are broadly used because of their efficient switching performance combined with relatively low conduction losses. IGBTs are made in different sizes, shapes and functionalities. IGBTs are becoming more compact, cost effective and reliable. The popularity of IGBTs in WTs as switching devices is due to higher efficiency and the capability for handling higher currents. Their multi-layer structure with several materials offers a higher mechanical stability, electrical insulation and adequate thermal conductivity [23]. Figure 2.9 shows 3D views of an IGBT module and its structure.

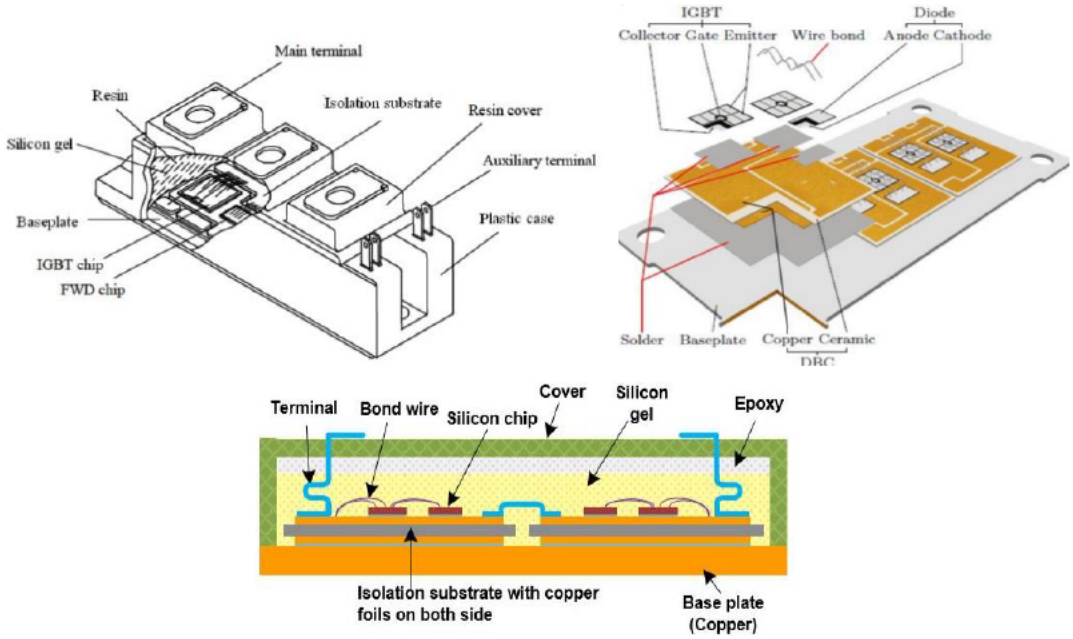


Figure 2.9: A 3-D view (top-left), cross section of a typical IGBT module (bottom-left) and IGBT layers (top-right) [24]

The structure consists of a plastic case connected to a baseplate. A direct copper bonded (DCB) ceramic substrate is soldered to the baseplate of the IGBT module and the IGBTs and diodes (fabricated on silicon chips) are soldered to the DCB. Aluminum bond wires are commonly used to connect the upper side of the silicon chips to the substrates as well connecting the substrates to the terminals. Table 2.1 lists the IGBT parts with their thermal expansion coefficients [25]. A description of three main different layers, i.e metallization and bond wires, DCB substrate, die-attached and solder joint are described below.

Bond wires are short aluminum wires used to connect pads on the silicon die to the emitter and gate terminals of the IGBT. In this thesis, the bond wires will always refer to the ones carrying the load current. The ones for the gate are not subjected to much stress in comparison. The bond wire diameter varies from 200 µm to over 500 µm, depending on the rated current of the IGBT. Multiple parallel bond wires can be present to allow high currents to be carried.
The DCB substrate consist of three layers: copper; ceramic; and copper. Copper layers are metallized on the top and bottom of the central ceramic layer. Common ceramics are alumina (AL_2O_3) or aluminum nitride (AlN). The lower copper layer is soldered to the baseplate. The copper-ceramic-copper 'sandwich' combines considerable thermal conductivity with electrical insulation. The DCB enables internal electrical interconnection between multiple silicon devices using copper tracks. It also ensures high insulation between the chips and baseplate, conducting waste heat away from the devices towards the cooling system at the rear of the device.

There are two layers of solder: one attaches the chips (or die) to the substrate and the other attaches the bottom layer of the DCB to the baseplate.

The baseplate provides a sound mechanical base for the housing. It also provides some thermal capacity and facilitates heat transfer to the attached heatsink. It also provides mechanical fixing holes or slots. The gap between heatsink and baseplate is filled with a thermal interface material such as thermal grease, the typical thickness being about 100 µm.

A module is mounted into a plastic case filled with a silicone gel, which provides better thermal insulation than air and better mechanical rigidity and protection against contamination. Terminal pins provide the electrical connections to the internal semiconductors, held in place by the molded plastic case. An IGBT module should operate reliably and efficiently over a large range of load and environmental conditions, so different packaging techniques have been developed for different applications.

2.8 Failure modes

Failures of IGBTs occur when one or more components fail to perform their intended function. Failure mechanisms are mainly a process whereby a specific stress, or a combination of different stresses, lead to failure. Failure mode mechanisms effect analysis (FMMEA) is a methodology to determine potential failure mechanisms and to assess the root causes of failures. FMMEA also captures the consequences of failures for a component or system [25]. Failure modes can be caused by one, or more failure mechanisms such as humidity, mechanical stresses, over current, over voltage, or temperature [26]. One approach that can be applied to reduce average failure rates, is to enhance device performance by optimising device design, thereby reducing the thermal and electrical stresses. Another approach, the one taken in this thesis, is to use a prognostic approach and monitor gradual failures. Failures are also categorised based on the failure site. i.e. chip related failures and package related failures. Chip-related failures are related to IGBT physics and silicon die intrinsic failures that can eventually destroy the IGBT. Chip-related failure mechanisms are further categorised into the following failure types:

- Time dependent dielectric breakdown (TDDB) [27]
- Electro-migration [28]
- Transient electrical stresses [29]
- Cosmic rays [30]

These failures are not the focus of this thesis. Packaging-related failures could adversely affect operating performance of a device by degrading the device safe operating area (SOA) [31]. These types of failure could promote increased operating temperature, which results in deterioration of SOA and thus the functionality of device. The maximum operating temperature of an off-the-shelf module plays an important role in defining the maximum electrical ratings. The temperature profile determines the reliability and lifetime of an IGBT under different load conditions.

The multi-layer structure of IGBTs can be affected by thermal stresses, as cyclic expansions and contractions during the power cycling of the IGBT can cause cracks between the layers. Various package related failure mechanisms can be categorised according to Figure 2.10. Among these faults, - BWLO [32], solder fatigue (SF) [33] and aluminium corrosion (ALC) [34] are found in WT applications [35]. Statistical analysis identifies BWLO and SF (for both die attach solder and DCB substrate solder) as critical failure mechanisms of IGBTs [36].

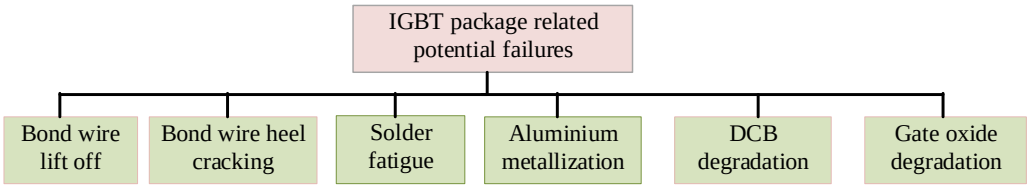


Figure 2.10: Common failure mechanisms of the IGBT

Results from field tests reveal that the most common site of 'wear-out' is the chip front side connection (bond wire to silicon), the chip to substrate connection (chip-solder joints) and the substrate to baseplate connection (DCB substrate-solder joints). The locations of these common failures are shown in Figure 2.11.

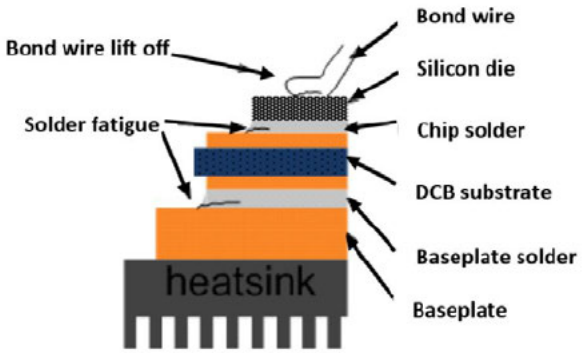


Figure 2.11: Three major regions facing thermo-mechanical failures

Amongst these, the first solder layer (silicon die to DCB) shows the lowest mismatch in thermal expansion coefficients. This failure is, therefore, not as common as the other two failures [37]. For this reason, the main focus of this work is on BWLO and DCB base plate failures.

Each layer of the IGBT is made from materials with different thermal expansion coefficients, which causes thermal stresses during relative expansions and contractions during power cycling [38]. Table 2.1 lists the IGBT parts with their thermal expansion coefficients [39]. Thermal stresses are one cause of failure. The next section describes this and other failure mechanism in more detail.

Table 2.1: Thermal expansion coefficients for materials commonly found in IGBTs [36]

Parts	Material	CTE (ppm/°C)
Silicone gel	Silicon resins	30-300
Epoxy resins	Epoxy	15-100
Terminal	Copper	16.5
Ni plating	Nickel	13.4
Bond wire	Aluminium	24
Chip	Silicon	3.2
Isolation substrate	Aluminium	6.8
	Aluminium Nitride	4.7
Baseplate	Copper	16.5
	ALSiC	8

2.8.1 DCB degradation

DCB ceramic cracks and DCB metallization can be observed under high temperature cycling [40-41]. Mismatch between the thermal expansion coefficients of the copper metallization and ceramic materials cause mechanical stresses during temperature cycles.

2.8.2 Gate oxide degradation

The gate oxide forms the dielectric layer found at the gate of an IGBT, separating the gate terminal from the drain terminal and from the conduction channel. The conduction channel connects the source and drain during the on-time of the transistor. Gate oxide degradation is the development of a conducting path through the gate oxide to the substrate because of a changing distribution of electrons in the oxide boundary. This situation typically occurs when the IGBT is operating beyond its gate-emitter voltage limit. This failure can also be as a result of ageing, being divided into two main types based on the root causes: time dependant dielectric breakdown (TDDB); and, single event gate rupture (SEGR). TDDB is the most common type of gate oxide degradation. TDDB is caused by gate voltage bias stress over time. This will lead to accumulations of defects in the gate oxide with an increase in the defect density conduction channel in the gate oxide layer, and hence gate oxide degradation will occur. A SEGR failure occurs when the IGBT operates in a radioactive environment due to the entrance of heavy ions into the device through the gate regions. This generates significant electron-hole pairs in the gate oxide over time, leading to gate oxide failure of the IGBT [43].

2.8.3 Bond wires lift-off degradation

Wire bonding is a process of electrically connecting a semiconductor to another place, such as a terminal pin or another die in a module. Bonding is carried out using an ultrasonic welding process that melts the wire and attaches a flattened end onto the target area. The bonded area is where the bond wire feet are connected to the chip metallisation. The most fragile part of the bond wire is its heel, due to a shear stress between the wire and chip pads. Heel-cracks can lead to peeling of the wire bonds and when there is an extension of a crack, to a full BWLO. Heel cracking of bond wires can occur if the module is poorly constructed [44-45]. BWLO occurs when the cracks from two opposite edges finally meet. An example of an initial crack is shown in Figure 2.12 [46].

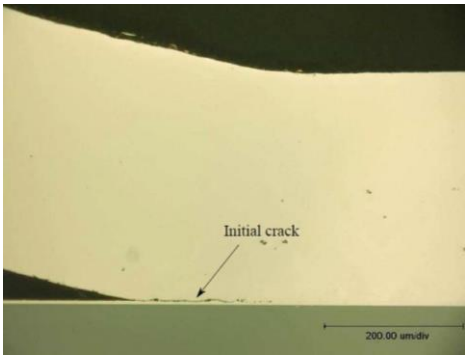


Figure 2.12: Initial crack at the heel of bond wires [46]

Due to low strength of aluminum bond wire and wire bond joints, initial cracks begin close to the wire to chip interface and propagate alongside the grain boundaries [47]. BWLO originates from exceeding the maximum junction temperature(T_{max}) and temperature fluctuations (ΔT_j). Examples of BWLO failure are illustrated in Figure 2.13.

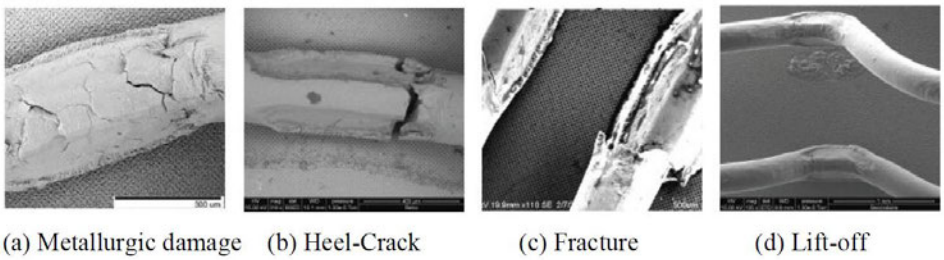


Figure 2.13: Examples of bond wire damage [48]

IGBTs are nowadays often made with a multiplicity of parallel bond wires. Failure mechanisms initially affect those wires located closer to the chip centre, where the temperature is higher. When one wire lifts off, the remaining wires carry the full load current with increased current density. This increases the stress on the remaining bond wires, increasing the likelihood of additional bond wire failures. This process continues until localised overcurrent and burnout failures occur [49, 50].

There have been attempts to estimate the lifetime of bond wires by numerical modelling [51, 52]. However, there is uncertainty in the initial stresses induced by deformation during the bonding process. Currently, the estimation of BWLO is based on experiments (accelerated ageing tests). This method is beneficial for emulating the ageing process, however there are many assumptions in this accelerating test in contrast to what happens in the real ageing process. BWLO will be considered in further details in chapter 5.

2.8.4 Solder fatigue

Chip solder and substrate solder joint are prone to the degradation in an IGBT. Degradation of the solder layers increases the thermal impedance from the junction to the case, eventually leading to overheating of the silicon chip. SF is mainly reported as initiating from either the edge or center of the chip, due to mismatch in the thermal expansion coefficients in combination with cyclic temperature variations [53, 54]. Deterioration in these solder layers occurs in the forms of voids, cracks and solder delamination. Cracks in the solder joint results in voids in the solder which leads to a rise in thermal resistance. The number of the voids and length of cracks increase due to power cycling and hence lead to SF. Crack propagation in the solder joints can also disturb the thermal path and hence can adversely affect the lifetime of bond wires.

There are three methods to estimate SF: the energy-based method [55]; the damage-based method [57]; and the strain-based method [56]. The energy-based method estimates the lifetime of solder by calculating the overall stress-strain hysteresis energy of the solder joint. The damage-based method carries out the same task by calculating the accumulated damage caused by crack propagation. These first two methods require a FEA tool to obtain the stress-strain hysteresis loop, so they are time consuming. The best-known strain-based method predicts failure from calculated or experimentally determined shear strain (ratio of the damage in deformation to its original length). The Coffin-Manson model is one of the best-known strain-based models [58]. SF will be considered in detail in chapter 6.

2.9 Reliability definition

Reliability is the probability that system or a component will perform a specified function under identified operational and environmental conditions for a given period of time, equation (2.3) [59, 60].

$$R(t) = P[t > T] \tag{2.3}$$

where reliability (over period of time t) is $R(t)$, the probability is P, the time to failure is T.

Failure against time is typically divided into three sections. The first section is the early failure period, where the hazard failure decreases with the passing of time. In the second section, random failures occur and the probability of failure remains roughly constant. The third period is the fatigue phase, where the failure rate increases over time and the product exceeds its design lifetime. The combined failure rate against time is shown in Figure 2.14 [60]. The graph is called the ‘bathtub’ curve because its shape resembles that of the longitudinal cross-section of a bathtub [61].

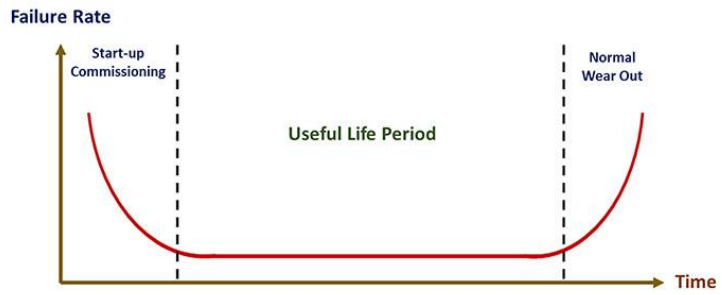


Figure 2.14: Bathtub curve

Failures are categorised into sudden and gradual failures. Sudden failure is considered as catastrophic failure and gradual failure is considered as a degradation failure [62]. SF and BWLO are categorised as gradual failures.

Mean time between failure (MTBF) is the average time between two successive failures. MTBF is one of the most important quantitative parameters that can help to achieve preventative maintenance as well as reliability, since an effective maintenance schedule can be carried out with knowing remaining time to the next failure. MTBF can be combination of mean time to repair (MTTR) and mean time to failure (MTTF) in equation (2.4). MTTF is the average time before the first failure of a component or device after starting to operate. MTTR is the average time to spend on repair of a failed device and its value is dependent on maintenance conditions [63].

$$MTBF = MTTF + MTTR \tag{2.4}$$

Availability is one of the important indicators of reliability and shows the probability of the system being functional as it becomes older. Average availability is the probability of functionality of requested components under given conditions during a period of time. Average availability can be obtained by equation (2.5), [64].

$$A_{ave} = MTTF/(MTTF + MTTR) \tag{2.5}$$

The average availability is improved by reducing the MTTR and increasing the MTTF [65]. Increasing the MTTF does not increase the average availability if the MTTR is much less than the MTTF. Average availability can be increased by reducing MTTR. To reduce MTTR, repair and maintenance time should be reduced by predicting the failure of the components. The minimisation of MTTR is realised at the design stage by eliminating or improving components that fail, for example by increasing the strength of components or materials so that they can withstand larger stresses, or by reducing the stress on failure-prone components. For the specific case of IGBTs, manufacturers aim to produce efficient cooling systems as a cooler IGBT lasts longer [66-68]. Even with changes in the component design, still there is a chance of a failure in the system.

An alternative solution to increase the reliability of IGBTs, or other power converter components, is to introduce fault-tolerant devices. Incorporating fault tolerance is one way to allow a system to continue operating in the presence of a fault until maintenance and repair can be effected. This is used so that a healthy device can take over while the faulty device is replaced. The time needed to service the faulty device should be short to reduce the probability of failure of the back-up module causing complete failure. This solution significantly increases the cost, size and weight of power converters, which is not desirable for the WT industry [69]. There is also a need to incorporate switching devices to disconnect the faulty device from the circuit and connect the replacement automatically, further adding to the cost of implementing this solution.

2.10 Summary

In summary, the electrical drive train of WTs are categorised into fixed-speed and variable speed WTs. The fixed-speed WT always rotates at the same speed of generator within operation of WT. As such the tip speed ratio (TSR) varies with wind speed and the dynamic performance of the rotor is optimum at this speed. In fact, the generated torque of fixed speed WT is accomplished by the induction generator (only small speed changes are expected due to the slip of the induction generator). A variable-speed WT operates over a wider range of wind speeds. As such, the generator speed is proportional to the wind speed variations so that between cut-in and rated speed it tries to maintain a constant TSR and optimal aerodynamic performance by using maximum power point tracking controller. Above the rated wind speed, the generator speed is held constant. The torque is actively controlled by the power electronic converters. PMSG and DFIG are the most common generator found in variable speed WTs.

The multi-layer structure of an IGBT is prone to premature failures due to expansion and contraction of the different materials. Detecting early degradation of the IGBT by applying a health condition monitoring system can help to predict the time required to replace the degraded IGBT and hence increase its reliability. To apply and develop an effective health condition monitoring system, IGBT's failure mechanisms are studied and discussed in this chapter. In addition, to understand the definition of the reliability and how the time remaining to failure can help increase the reliability and availability of the system the bathtub curve has been introduced. In the next chapter, chapter 3, different methods that have been applied to monitor IGBTs will be described. In addition, the pros and cons of these methods in terms of their limitations and complexity are discussed. A health condition monitoring method is suggested according to the outcomes at the end of chapter 3. In order to apply and investigate the proposed method, a physical model of the converter is designed as described in chapter 4.

2.11 References

[1] "EWEA: 'Wind energy – the FACTS', Earthscan, London", pp. 212–220, 2009.

[2] R. Moeini, M. Entezami, M. Ratkovac, P. Tricoli, H. Hemida, R. Hoeffer and C. Baniotopoulos, “Perspectives on Condition Monitoring Techniques of wind turbines”, wind energy journal, 2018.

[3] M. RabiulIslam, Y. Guo and J. Zhu, ‘A review of offshore wind turbine nacelle: Technical challenges, and research and developmental trends’, Renewable and Sustainable Energy Reviews, vol. 33, May 2014, p.p.161-176.

[4] Z. Chen, M. Guerrero and F. Blaabjerg, “A Review of the State of the Art of Power Electronics for Wind Turbines”, IEEE Trans on Power Electro, vol. 24, (8), Aug 2009.

[5] C. Chompoo-Inwai, C. Yingvivatanapong, K. Methaprayoon and W. J. Le, “Reactive compensation techniques to improve the ride-through capability of wind turbine during disturbance,” IEEE Trans, vol. 41, (3), pp. 666–672, 2005.

[6] W-M. Lin, C-M. Hong “Intelligent approach to maximum power point tracking control strategy for variable-speed wind turbine generation system”, Energy Elsevier, vol. 35, (6), Jun 2010, pp. 2440-2447.

[7] D. Kumar, K.Chatterjee, “A review of conventional and advanced MPPT algorithms for wind energy systems”, Renewable and Sustainable Energy Reviews, vol.55, Mar 2016, pp. 957-970.

[8] E. Muljadi, C.P. Butterfield , “Pitch-controlled variable-speed wind turbine generation”, IEEE Trans on Industry Appl, vol. 37 , (1) , pp. 240-246, 2001.

[9] E. Muljadi, K. Pierce and P. Migliore, “Control strategy for variable-speed, stall-regulated wind turbines”, American Control Conf, Jun 1998.

[10] F. Blaabjerg, Z.Chen, “Power Electronics for Modern Wind Turbine”, Synthesis Lectures on Power Electronics, DOI: 10.2200/S00014ED1V01Y200602PEL001, 2006.

[11] B. Dehong Xu, F. Blaabjerg, W. Chen and N.Zhu, “Advanced Control of Doubly Fed Induction Generator for Wind Power Systems”, The Institute of Electrical and Electronic Engineers, DOI. 10.1002/9781119172093, 2018.

[12] X. Jing “Modelling and Control of a Doubly-Fed Induction Generator for Wind Turbine-Generator Systems”, Dec 2012.

[13] S.Arnaltes, J. L.Rodriguez-Amenedo and Miguel E. Montilla-DJesus, “Control of Variable Speed Wind Turbines with Doubly Fed Asynchronous Generators for Stand-Alone Applications” Energy journals, 2017.

[14] B. Almutairi, “Investigating the feasibility and soil structure integrity of onshore wind turbine systems in Kuwait”, PhD Thesis, Loughborough University, 2017.

[15] T. Sandhya and K. Sri Chandan (2011), “Control and operation of Opti-slip induction generator in wind farms”, Int Conf on Computer, Communication and Electrical Technology (ICCCET), Tamilnadu, India, Mar 2011. DOI: 10.1109/ICCCET.2011.5762517.

[16] E. N. Sanchez, R. Ruiz-Cruz (2016), “Doubly Fed Induction Generators: Control for Wind Energy”, CRC Press, 2016. ISBN 9781498745840.

[17] Q. Han, J. Wei, Q. Han, (2017), “Dynamics and Vibration Analyses of Gearbox in Wind Turbine”, Springer Singapore, 2016. DOI 10.1007/978-981-10-2747-5.

[18] N. Goudarzi, W. D. Zhu (2013), “A review on the development of wind turbine generators across the world”, Int. Journal of Dynamics and Control, Vol 1, pp. 192–202, 2013.

[19] R. S. Semken, M. Polikarpova, P. Roytta, “Direct-drive permanent magnet generators for high-power wind turbines: benefits and limiting factors”, IET Renewable Power Generation, Vol. 6 , pp.1-8, Jan 2012.

[20] A. Lebsir, A. Bentounsi, M. Benbouzid and H. Mangel, “Electric Generators Fitted to Wind Turbine Systems: An Up-to-Date Comparative Study”, 2015.

[21] P. Sharma, T. S. Bhatti, K. S. S. Ramakrishnan, Permanent-Magnet Induction Generators: an overview, Journal of Engineering Science and Technology, Vol. 6, No. 3 332 – 338, 2011.

[22] S. Fu, Y. Mei, X. Li, et al. ‘Reliability evaluation of multichip phase-leg IGBT modules using pressure-less sintering of nanosilver paste by power cycling tests’, IEEE Trans. Power electro, 2017, 32, (8), pp. 6049–6058.

[23] V. Kumar Khanna, Insulated gate bipolar transistor theory and design, 2014.

[24] Blicher, Thyristor Physics, 2013.

[25] M. Ohring, L. Kasprzak, ‘Reliability and failure of electronic materials and devices’, 2014.

[26] L. Kongjing, T. Gui Yun, C. Liang , ‘State detection of bond wires in IGBT modules using eddy current pulsed thermography’, IEEE Trans on Power Electro, Vol. 29 , PP. 5000 – 5009, 2014.

[27] Choi, U.-M., Jørgensen, S., Blaabjerg, F, ‘Advanced accelerated power cycling test for’, IEEE Trans. Power Electron, 31, (12), pp. 8371–8386, 2016.

[28] N.Patil, “Diganta Das, Kai Goebel and Michael Pecht, Failure Precursors for Insulated Gate Bipolar Transistors (IGBTs)”, 2008.

[29] H. Abbad, “A first approach on the failure mechanisms of IGBT inverters for aeronautical applications: effect of humidity-pressure combination”, 2011.

[30] H. Wang, P.P. Rimmen, J. B. Jacobsen, T.Kvisgaard, and J. Landkildehus “Transitioning to Physics-of-Failure”, Reliability Driver in Power Electronics, 2014.

[31] Re. Bayerer, T. Herrmann, T. Licht, Jo. Lutz, M. Feller, “Model for power cycling lifetime of IGBT modules-various factors influencing lifetime”, 2008.

[32] M. Trivedi, K. Shenai, “Failure mechanisms of IGBTs under short-circuit and clamped inductive switching stress”, IEEE on power electronics, Vol.14, PP.118-116, Jan 1999.

[33] S. Nishida, T.Shoji, T.Ohnishi, et al, ‘Cosmic ray ruggedness of IGBTs for hybrid vehicles’, Power Semiconductor Devices & IC's (ISPSD), 2012.

[34] C. Zorn, N. Kaminski, 'Temperature–humidity–bias testing on insulated-gate bipolartransistor modules – failure modes and acceleration due to high voltage', IET Power Electronics, Vol. 8, PP. 2329 – 2335, 2015.

[35] H. Li, S.Liu, Y. Li, et al, 'Power cycling capabilities assessment of IGBT modules in wind power converter considering the wind turbulence effects', Int Conf on Power Electronics, PP. 30 – 34, 2014.

[36] L. Zhou, S.Zhou, M.Xu, 'Investigation of gate voltage oscillations in an IGBT module after partial bond wires lift-off', Microelectron. Reliab. Vol. 53, (2), pp. 282–287, 2013.

[37] B. Ji, X. Song, W. Cao, et al, "In Situ diagnostics and prognostics of solder fatigue in IGBT modules for electric vehicle drives", IEEE on power electro, Vol. 30, Mar 2015.

[38] U.-M. Choi, S.Jørgensen, F.Blaabjerg, "Advanced accelerated power cycling test", IEEE Trans. Power Electron., 31, (12), pp. 8371–8386, 2016.

[39] V. K. Khanna, "Insulated gate bipolar transistor theory and design", 2014.

[40] L. Dupont, Z. Khatir, S. Lefebvre, and S. Bontemps, "Effects of metallization thickness of ceramic substrates on the reliability of power assemblies under high temperature cycling", Microelectronics Reliability, Vol. 46, pp. 1766-1771.

[41] G. Mitic and G. Lefranc, "Localization of electrical-insulation and partial discharge failures of IGBT modules", IEEE Trans on Industry Appl, Vol. 38, pp. 175-180, 2002.

[42] L. Dupont, Z. Khatir, S. Lefebvre, R. Meuret, B. Parmentier, and S. Bontemps, "Electrical characterizations and evaluation of thermo-mechanical stresses of a power module dedicated to high temperature applications", European Conf Power Electro and Appl, pp. 11, 2015.

[43] G. Mitic and G. Lefranc, "Localization of electrical-insulation and partial discharge failures of IGBT modules", IEEE Trans Ind Appl, vol. 38, pp. 175-180, 2002.

[44] M. Pecht, "Integrated Circuit Hybrid, and Multichip Module Package Design Guidelines", Power Engineering Review, IEEE, vol. 15, 1995.

[45] M. Pecht and G. Jie, "Physics-of-failure-based prognostics for electronic products", Trans of the Institute of Measurement and Control, vol. 31, pp. 309-322, Jun/Aug 2009.

[46] C. Mauro, "Selected failure mechanisms of modern power modules", Microelectronics Reliability, vol. 42, pp. 653-667.

[47] M. Ciappa and W. Fichtner, "Lifetime prediction of IGBT modules for traction applications", Rel Physics Symposium, Proceedings, pp. 210-216, 2000.

[48] J. Onuki and M. Koizumi, "Reliability of thick Al wire bonds in IGBT modules for traction motor drives", Power Semiconductor Devices and ICs, ISPSD '95. Proceedings of the 7th Int Symposium on, 1995, pp. 428-433.

[49] V. Smet, F. Forest, J.-J. Huselstein, F. Richardeau, Z. Khatir, S. Lefebvre, and M. Berkani, “Ageing and failure modes of IGBT modules in high-temperature power cycling”, IEEE Trans on Industrial Electro, vol. 58, pp. 4931-4941, 2011.

[50] T. Herrmann, M. Feller, J. Lutz, R. Bayerer, and T. Licht, “Power cycling induced failure mechanisms in solder layers”, European Confe on Power Electro and Appls, 2007, pp. 1-7.

[51] F. Kovačević, Drofenik, and J. W. Kolar, “New physical model for lifetime estimation of power modules”, Power Electro Conf (IPEC), Int, 2010, pp. 2106-2114.

[52] J. Lutz, “IGBT-Modules: Design for reliability”, Power Electro and Appli, EPE '09. 13th European Conf, 2009, pp. 1-3.

[53] H. Ye, M. Lin, and C. Basaran, “Failure modes and FEM analysis of power electronic packaging”, Finite Elements in Analysis and Design, vol. 38, pp. 601-612, 2002.

[54] Z. Khatir and S. Lefebvre, “Boundary element analysis of thermal fatigue effects on high power IGBT modules”, Microelectronics Reliability, vol. 44, pp. 929-938, 2004.

[55] R. Amro, J. Lutz, J. Rudzki, M. Thoben, and A. Lindemann, “Double-sided low temperature joining technique for power cycling capability at high temperature”, Power Electro and Appl Conf, 2005.

[56] H. Wang, K. Ma, F. Blaabjerg, “Design for reliability of power electronic systems”, Conf on IEEE Industrial Electro Society, Oct 2012; pp. 33–44.

[57] R.Giuntini, “Mathematical characterization of human reliability for multi-task system operations”, IEEE Inter Conf on Sys, Oct 2000, pp. 1325–1329.

[58] G. Klutke, P.Kiessler, M.Wortman, “A critical look at the bathtub curve”, IEEE Trans on Rel, 2003, (52), pp.125–129.

[59] A. T. Bryant, P. A. Mawby, P. R. Palmer, E. Santi, and J. L. Hudgins, “Exploration of Power Device Reliability Using Compact Device Models and Fast Electro thermal Simulation,", IEEE Trans Industry Appl, Vol. 44, pp. 894-903, 2008.

[60] M. Ciappa and A. Castellazzi, “Reliability of High-Power IGBT Modules for Traction Applications”, Reliability physics symposium, 2007, pp. 480-485.

[61] “Semiconductor Reliability Handbook”, Renesas Electro Corporation, Nov 2008.

[62] X. Perpiñà, L. Navarro, X. Jordà, M. Vellvehi, J.-F. Serviere and M. Mermet-Guyennet, “Reliability and Lifetime Prediction for IGBT Modules in Railway Traction Chains”, reliability and safety in railway, in 2013, available at http://cdn.intechopen.com/pdfs/34436/InTech-Reliability_and_lifetime_prediction_for_igbt_modules_in_railway_traction_chains.pdf.

[63] P. A. Kullstam, “Availability, MTBF and MTTR for Repairable M out of N System” IEEE Trans on Rel, Vol. R-30, (4), pp. 393 – 394, Oct 1981.

[64] S. J. Rhee, K. Ishii “Using cost based FMEA to enhance reliability and serviceability”, Vol.17, (3–4), Elsevier at advanced engineering and affirmative, 2004, pp.179-188.

[65] L.Wei, A. L. Richard, A. L. Thomas, “Analysis of Power Cycling Capability of IGBT Modules in a Conventional Matrix Converter”, (5-9), DOI: 10.1109/08IAS.2008.265, Oct. 2008.

[66] C. Gillot, C. Schaeffer, C. Massit, and L. Meysenc, “Double-sided cooling for high power IGBT modules using flip chip technology”, IEEE Trans on Components and Packaging Techno, Vol. 24, pp. 698-704, 2001.

[67] J. B. Campbell, L. M. Tolbert, C. W. Ayers, B. Ozpineci, and K. T. Lowe, “Two-Phase Cooling Method Using the R134a Refrigerant to Cool Power Electronic Devices”, IEEE Trans on Industry Appl, Vol. 43, pp. 648-656, 2007.

[68] G. Mulcahy and J. Santini, “Next Generation Military Vehicle Power Conversion Modules”, TDI Power, Apr 2008.

[69] B. Lu, Y. Li, X.Wu and Z. Yang “A review of recent advances in wind turbine condition monitoring and fault diagnosis” IEEE Power Electro and Machines in Wind Appl, 2009.

Chapter 3: Review of failure modes of IGBT modules – mechanisms and effects

3.1 Introduction

Some parts of this chapter are taken from the proceedings of the Wind Engineering Journal (Moeini, Pietro, Hemida and Baniotopoulos) with appropriate referencing. IGBTs have been used as power electronics switching components for several decades. Methods for detecting incipient failures have being developed to improve the maintenance processes for IGBT modules and to predict the residual lifetime. This chapter reviews the state-of-the-art of IGBT (module) health condition monitoring methods in the technical literature in combination with various failure modes and gives directions on the future steps that require to be addressed by research in this area.

3.2 Faults and failures

The engineering definition of the term 'fault' is an unpermitted abnormality or deviation of any system parameters from an acceptable condition. When a fault within a system prevents normal operation (a malfunction), this stops the system functioning, thus causing a failure. A failure to operate is a breakdown [1, 2]. Detecting the fault type, magnitude, time of occurrence and location in a system are the main factors involved in fault detection and diagnosis systems. In a fault, detection and diagnosis system the following tasks are carried out [1]:

- Fault detection: indicates that a fault has occurred in the system.
- Fault diagnosis: determines the type of fault. This could lead to finding the possible location (component) of the failure.
- Fault identification: Extracts the characteristics of the fault out of the health condition monitoring system, such as seriousness of health damage and significance. It also determines the exact location of the failure.

3.3 Health condition monitoring of IGBT

Some failures in an IGBT module cause the system to stop functioning completely. For example, if an IGBT becomes a short circuit and there is no way to electronically disconnect the IGBT from the circuit. Other failures might degrade the performance of the system without rendering the system inoperative. An example might be an open-circuit failure of one of two parallel IGBTs in a module. The two failure modes described are example of sudden faults; the fault is either present or not present. Yet other failure modes can be in the form of continuous degradation of some property of the module, such as weakening of the solder joint between an IGBT and the substrate material. This type of failure mode is continuous in nature and the definition of when it becomes a serious problem depends on the application. A fault such as an open circuit IGBT could be linked to several different failure mechanisms, for example, either the emitter or the collector connection might have been damaged.

If the gate connection fails, this might give the appearance that the IGBT has failed in an open circuit way but be defined as a different failure mechanism. Thus, a named fault may be caused by more than one failure, acting independently or together. Fault detection means identifying that a certain fault has occurred. Fault diagnosis means determining the root cause of the failure. Knowing the root cause means that maintenance can be carried out on the right component rather than arriving on site and having to figure out what the problem is. Being able to detect a failure, or to estimate the extent of some degradation, can be useful to providing information to advise maintenance scheduling that is critical for predictive maintenance.

Intuitively, a health condition monitoring targets common failure modes, but optimally it should target failure modes that cause the greatest cost if undetected. An unreliable health condition monitoring scheme can also introduce additional failure modes and false alarms are a particular problem as these prompt unnecessary maintenance actions. Fault diagnosis involves understanding and interpreting the current state of the system, generally using historical knowledge of the system state. Providing early diagnosis of changing system state while the system is still functioning acceptably can help to avoid progression of the failure to the point where complete failure occurs. Health condition monitoring of IGBTs enables assessment of degradation in the context of the application. Furthermore, this offers the possibility of predicting the health state and the residual lifetime of the IGBT modules.

Three steps are required to implement a health condition monitoring system [3]:

1. Evaluation of the ‘current health state’ of the IGBT
2. Definition of the factors and assessment of their degradation effects on the IGBT performance, or the system in which the IGBT is used
3. Anticipation of the future health state of the IGBT

A health condition monitoring system helps to predict the impact of failures associated with ageing. Implementation of an accurate health condition monitoring for IGBT modules generally relies on on-line tracking of the temperature variations of the components due to the changes in the thermal path of the module. The heat source of the IGBT is silicon die and hence, it is the hottest point with temperature T_j. It is not easy to measure T_j directly . Additional challenge of direct measurement is to track high speed dynamic temperature variations given the slower response of most thermal sensors due to sensor thermal mass.

Therefore, several methods have been presented in the technical literature to estimate T_j by monitoring the electrical parameters. Each method has some advantageous and disadvantages in terms of accuracy and complexity, since failure mechanisms have their own effects on the variations of T_j and some, or all, of the electrical parameters. Detection algorithms have to determine whether the temperature variations are estimated using the variation of electrical parameters originated from a failure or it is caused by normal operation such as varying device current or voltage.

Various methods can be applied to assess the current health state of an IGBT module and to understand the state of degradation. This can be done through tracking parameters, also called 'failure detectors', that are affected by failure mechanisms. A failure detector is specified to detect premature failure in the IGBT module. Each failure detector can be used for diagnosis of a specific failure. Given an understanding the type of failure and stage of degradation, the future state of the IGBT could be estimated [4]. To date, two main approaches have been used to monitor the state of health in the IGBT modules and predict imminent failures. These methods are either based on secondary devices, or are data driven. The data driven method can be divided into direct measurement and estimation methods, as shown in Figure 3.1 and explained in detail in the following subsections [5, 11].

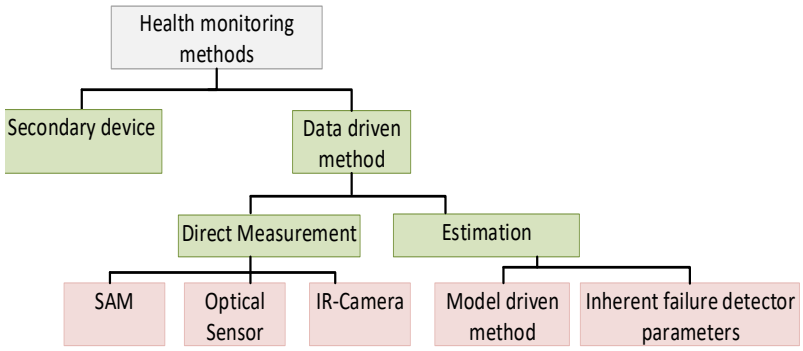


Figure 3.1: Health condition monitoring techniques for IGBT

3.3.1 Diagnostic techniques based on secondary devices

Techniques based on secondary devices use an expendable component, called the 'secondary device', that is embedded into the monitored component and emulates the same failure mechanisms. The secondary device is designed with a shorter lifetime than the monitored component, so that failure of this device flags that the monitored component is likely to fail in the near future. To achieve the desired reduced lifetime, the secondary device is either subjected to accelerated degradation before commissioning, or it is weakened in some other way (for example, making a current carrying component thinner) [12]. Figure 3.2 shows the 'bath tub' curves of the secondary device and the main component. As shown in the figure, the secondary device is designed to fail ahead of the main component to be able to detect the problem and take action before a fault occurs[6]. This approach has been developed by [6-7]. In the context of a semiconductor device, a prognostic cell is included inside the silicon chip [12], located on the same silicon chip as the IGBT. Therefore, any parameter that affects the reliability of the main device will also similarly affect the secondary device.

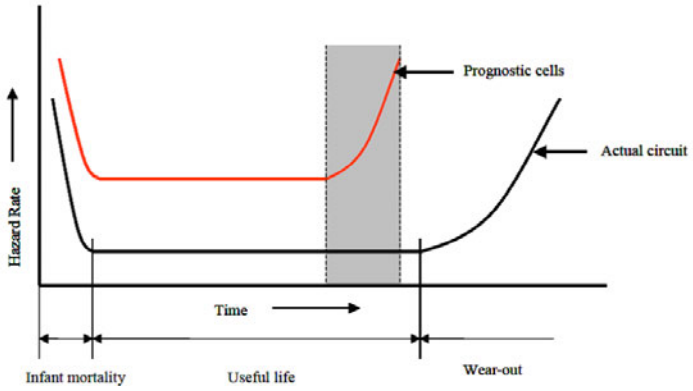


Figure 3.2: The idealized 'bathtub' reliability curves for a test circuit and prognostic cell [12]

3.3.2 Data driven methods

Data driven methods are based on tracking T_j or temperature related electrical parameters. This tracking can be done in two ways: direct measurement and estimation techniques. Direct approaches evaluate the trends of the parameters that are directly measured by sensors. Estimation approaches evaluate historical data collected by an in-situ monitoring system, also called a historical profile of the temperature or electrical parameters. Any changes of the parameters when compared to their historical healthy values may indicate an impending failure [13]. Initially the IGBT should be calibrated in a known healthy state at different temperatures and under controlled load conditions to characterise the electrical parameters of the IGBT in healthy status. The existing degradation is estimated, and then an extrapolation of the measured parameters is performed to find a relationship between the extrapolated degradation rate and failure. This relationship can help to understand any variation of failure detector parameters within the progress of the failure.

3.1.3.2 Direct measurement methods

Almost all failure mechanisms, as explained chapter 2, affect the temperature profile of the IGBT. The direct method refers to direct measurement of T_j using a temperature sensor or an IR camera [14-15]. In addition, the failure itself can be directly identified by integrating a temperature sensor into the IGBT structure. The direct method is mainly considered as an invasive way of monitoring T_j due to required modification to the module structure by adding integrated sensors. The direct methods with integrated sensors are mainly used to detect early BWLO. As an example of this approach is using a sensor resistor connected in parallel with the bond wires of the IGBT as a temperature sensor, as shown in Figure 3.3 [16, 17]. The left-hand side shows a healthy IGBT and the right-hand side is a schematic with two bond wires out of six lifted off. In the presence of BWLO, all i_c will pass through the remaining wires with the current sensor so that the rise in the sensed current can indicate BWLO. When BWLO occurs, the combined impedance of the embedded current sensor and remaining bond wires becomes comparable with that of the non-lifted bond wires, since the current passing through the remaining bond wires increases. The disadvantages are the requirement of additional sensors integrated into the architecture of the module and the restriction to the detection of only a very specific failure. Another schematic of the IGBT is shown in

Figure 3.4. The voltage across the bond wire is measured by a sensor and fed to a comparator that compare this value with a set voltage value that is called V_0. Any derivation from these two measurements can be detected through the logic block (output of the comparator).

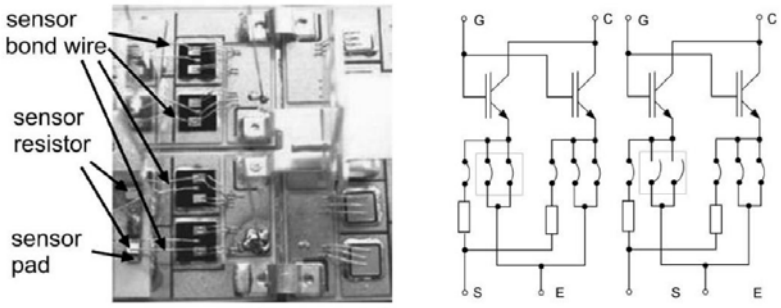


Figure 3.3: Emitter bond wire lift-off [18]

(a) modified the IGBT module, (b) equivalent circuit for pre-failure (left -side); equivalent circuit for post failure (right-side) [12]

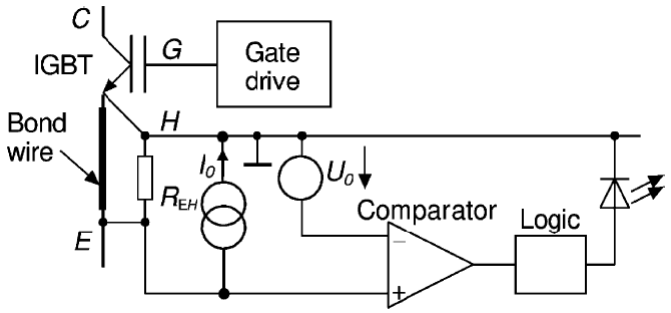


Figure 3.4: The example of embedded sensor for monitoring of bond wire lift-off [19]

Some other methods have been used to observe and analyse the temperature profile of the junction terminal to detect BWLO by using an optical fibre [21], infrared (IR) camera [22, 23] or infrared sensors can be used [24]. Through these devices, temperature variations of the bond wires can be observed. These approaches avoid significant modifications of the monitored device, since they can be applied by looking into the module. However, using IR cameras are not sufficiently accurate, as the camera only scans the surface of the IGBTs and not the inner layers and hence, does not give details for the inner layers of the IGBT. In addition, the IGBT modules tends to be filled by silicone gel which acts as a barrier to sensing the temperature of the substrate and bond wires. Chen, *et al*. [25] demonstrated that the accuracy of temperature measurement could be improved by using an IR camera together with laser scanning, as the laser provides an internal view of the module. However, the synchronisation between the IR camera and laser scanning requires a large data set (the temperature of each pixel at each sample time), which makes this method unsuitable for on-line measurements. Scanning acoustic microscopy (SAM) imaging is another direct method of examining failure degradation. They are used to evaluate direct copper bond (DCB) solder layer conditions and detect SF in terms of voids, cracks and delamination [17, 18].

Scanning acoustic microscopy (SAM) is also used as direct approach of detecting failure. SAM can image voids and cracks relative to the intact solder [26]. This is due to the increase in thermal resistance at the locations of degradation. This approach is, however, only applicable as an off-line method for health condition monitoring. To achieve an on-line assessment of the thermal path condition, thermal impedance can be employed as a failure detector parameter [27]. The condition of the thermal path between heatsink to junction terminal can be adversely affected by degradation of the DCB substrate and solder layers. The thermal impedance can be estimated from measurement of power losses and temperature in combination with a thermal model of the IGBT [26].

In general, direct methods are not very popular as they incur high implementation cost and often require access inside the module or removing the module from the system [20]. For these reasons, the direct

detection of failure mechanisms is mainly adopted only for the experimental verification of other techniques and is not generally useful for field applications [25].

3.2.3.2 Estimation methods

Estimation methods are based on interpolations of the thermo-sensitive parameters to extract temperature. The estimation methods are divided into two approaches: using inherent failure detector parameters; and developing numerical models of the IGBTs in combination with power losses measurement. Inherent electrical parameters of the IGBT can be used to estimate T_j or used to estimate premature failure. The second approach is based on thermo-mechanical modelling of an IGBT and its heatsink to calculate the thermal path of the IGBT layer. Any variations in thermal behaviour of the IGBT (outside of normal limits) can represent the possibility of failure.

3.2.3.2.1 Methods based on inherent failure detector parameters

The 'thermo-sensitive electrical parameters' (TSEPs)/ inherent electrical parameters of the IGBT are those electrical parameters that have sensitivity to variations of temperature. These parameters can be used as failure detectors or means of estimating T_j. Using these parameters is a challenge for dynamic applications (such as WTs and electrical transport drives), owing to difficulties in the measurement and processing of the data within the operation of the system [28]. There has been some success reported using such parameters in an on-line monitoring system for application to electric vehicles for monitoring of BWLO and SF [29]. Measurements are made when vehicles are stopped, for example at traffic lights or refuelling stations for electric road vehicles or at station stops for rail vehicles, and the data analysed at leisure such as while in a depot or when vehicles are stationary.

Health condition monitoring of IGBTs in continuous dynamic applications such as WTs is more challenging, as operation ideally does not come to a stop. In such cases, it is essential to use failure detectors that can be monitored during normal operation. Some research concerning the use of failure detecting parameters are described in the following paragraphs. These methods have some advantages and disadvantages in terms of sensitivity to the failure, complexity of implementation, but some of them can be used in normal operations. The above failure detection methods can be applied to detect several failure mechanisms in the IGBT however the accuracy and sensitivity of each described method to the progress of failure varies from one failure type to another as described in following sections.

3.2.3.2.2 Detection of gate oxide degradation

Gate oxide degradation can be detected by measuring several electrical parameters, such as $V_{GE,th}$ [30], switching times [30, 31] and leakage current [32]. Gate oxide degradation causes an increase of $V_{GE,th}$, (up to 11 V). Patil, et al. (2018) [33] studied the effect of gate oxide degradation on switching-on time.

They measured $V_{GE,th}$ during 'turn on time' and showed that the duration of the Miller plateau decreases. The Miller plateau voltage increases as the gate trapped charge increases with advancing gate oxide degradation. However, this approach is not suggested to be feasible in real time applications. To measure $V_{GE,th}$ it is necessary to interrupt the operation of the converter and inject an external signal. It is well-known that positive bias temperature (PBT), high electric field (HEF) and irradiation stress adversely affect the gate oxide [33] but each of them affects the gate oxide in a different way. The Miller platform voltage level could be used to identify gate oxide degradation originating from both BPT and HEF stresses. The voltage level of Miller plateau (V_{GP}) shows higher sensitivity to the gate degradations compared to $V_{GE,th}$. Karki, *et al*. (2018) [34] and Karli *et al*. (2009) [35] have proposed using the duration of the Miller plateau (t_{GP}) as a detector of gate oxide deterioration.

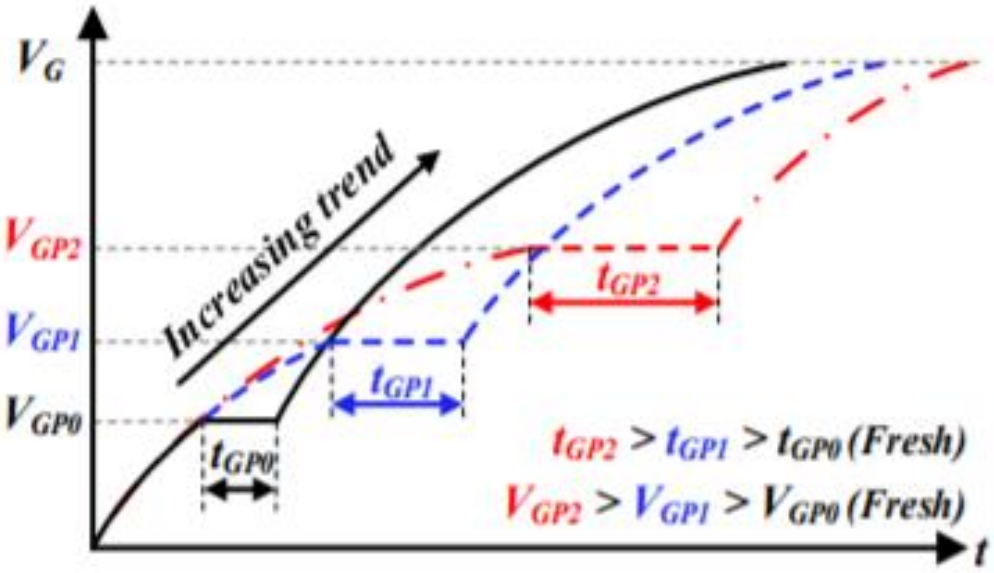


Figure 3.5: Increase in Miller plateau voltage (V_{GP}) within the progress of gate oxide degradation [35]

Time t_{GP} has been found by considering the time difference between rising edges of two pulses (during the turning on time of the IGBT). t_{GP} is shown to be more sensitive to gate oxide degradation compared to V_{GP}, so t_{GP}increases from 0.72% to 124% and V_{GP} increases from 0.35% to 56% for voltages between 54 V and 66 V for their setup [36]. Temperature t_{GP} measurement is examined for low switching frequency such as DC circuit breaker. However, the measurement uncertainly and complexity of measurement circuit integration to the gate driver in a high switching frequency application is not clearly outlined.

Lue, *et al*. (2016) [37] used switching time parameters to estimate T_j, which is subsequently used as a failure detector of gate oxide degradation. T_j is estimated using linear relations previously established between T_j, t_{on} and t_{off} using calibration experiments. A rise in T_j represents gate oxide degradation.

The negative aspect of this research is that increases in $t_{on}$and t_{off} can originate not only from IGBT degradation but also from degradation of the gate driver that causes V_{GE}, and therefore t_{on} and t_{off}, to change [38]. Kuhn, et al. (2009) [39] used $t_{d,on}$ and its first derivative with respect to T_j as failure detector of the gate oxide degradation. Quantity $t_{d,on}$ was estimated from measurements of the V_{CE}, V_{GE} and i_c waveforms. They estimate T_j from $t_{d,on}$, in combination with prior calibration between them. In this research gate oxide degradation is the failure being diagnosed by monitoring variations of T_j.

Another parameter that has been studied as failure detector for gate oxide degradation is the emitter capacitance which changes due to electrons trap in the presence of this failure mode [40]. Kuhn, *et al*. (2008) [39] have shown that gate oxide degradation increases $V_{GE,th}$ and decrease $V_{CE,on}$. In this research $V_{GE,th}$ and $V_{CE,on}$ are used as gate oxide degradation detector while T_j is estimated from $t_{d,on}$. Kuhn has improved the reliability of the failure detection process by monitoring T_j and the failure detectors using a different approach for monitoring of healthy status of the IGBT, i.e using $t_{d,on}$ to estimate T_j and $V_{GE,th}$ and $V_{CE,on}$ to detect the failure mechanisms.

3.2.3.2.3 Detection of bond wire lift-off degradation

The $V_{CE,on}$, V_F, R_{on} and i_c are four electrical failure detectors that are widely used to detect BWLO [40-44]. $V_{CE,on}$, V_F, i_c, and R_{on} all increase when BWLO occurs. Chip metallisation causes a reduction in the effective cross-sectional area of metallisation layers, leading to an increase in the electrical resistance [45]. Relative variations of the above electrical parameters are not studied when a converter is in operation. Imire *et al.* (2014) [46] and Bęczkowski *et al.* (2013) [47] demonstrated that $V_{CE,on}$ increases linearly with T_j. They used variations of $V_{CE,on}$ to detect early BWLO. However, an increase of $V_{CE,on}$ does not necessarily imply an increase in T_j. For example, in the presence of gate oxide degradation, T_j increases while $V_{CE,on}$ decreases [48]. Therefore, $V_{CE,on}$ can only accurately predict early BWLO if the T_j is estimated with a parameter that is independent from BWLO. An alternative method of measurement of $V_{CE,on}$is based on an in-situ circuit connected to the power converter that measures both i_c and $V_{CE,on}$ in real time [48-50], however this requires modification to the structure of the IGBT, which is not desirable. A bipolar amplifier circuit is used so that the circuit can operate for both positive and negative $V_{CE,on}$ and the voltage drop on a freewheeling diode V_{FD} can also be measured. V_{FD} is used to detect BWLO of diode. T_j is estimated by calibration between $V_{CE,on}$ and T_j as a function of i_c. This looks like a promising approach as BWLO does not significantly affect the temperature distribution within an IGBT in its early stages. Zhou, *et al*, [25] have studied dynamic changes of i_G in the presence of BWLO. They argue that parasitic elements (L and R are representing bond wires in Figure 3.5) within the chip are affected by BWLO.

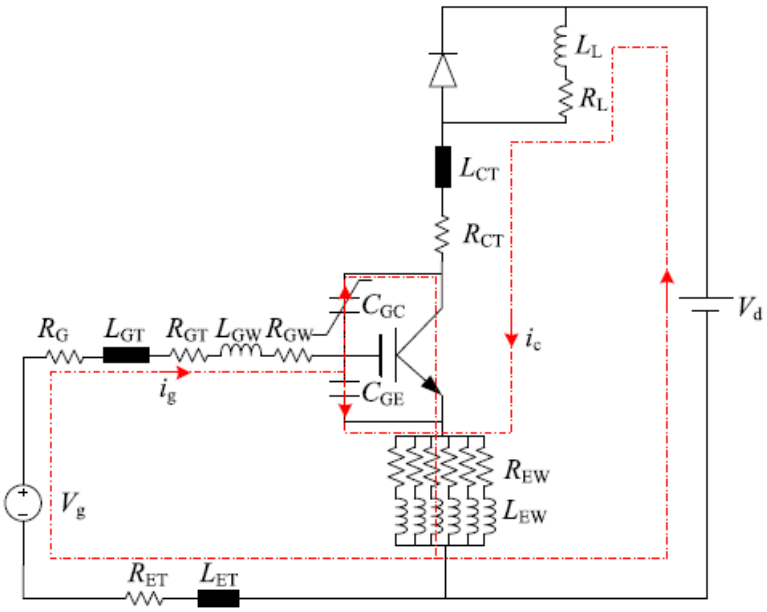


Figure 3.5: Equivalent gate circuit during turning on of the IGBT [25]

The authors extracted the parasitic parameters by a 3-D model of the IGBT [42]. They applied the achieved parameters in a 2-D equivalent gate circuit and showed that variations of inductance and resistance are mainly due to the packaging terminal leads and not BWLO. Thus, i_G does not significantly change until full degradation of the bond wires has occurred, shown in Figure 3.5.

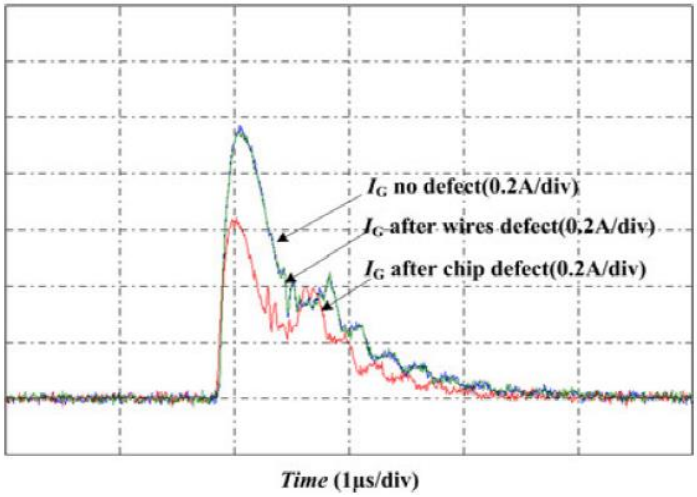


Figure 3.5: Variations of I_G during the progress of bond wire lift off [40]

Zhou, *et al.* [25] has found that V_{GE} cannot be a good detector of BWLO during its initial stages until three out of seven bond wires has lifted off. They electrically modelled the gate circuit of the IGBT considering its parasitic elements to evaluate the variations of the V_{GE} during the turn on of the IGBT according to equation (2.5). The analytical study based on the model and experiment results show that there is no significant change inV_{GE} when early and partial BWLO occurs. The change in V_{GE} with the progress of BWLO is shown in Figure 3.6.

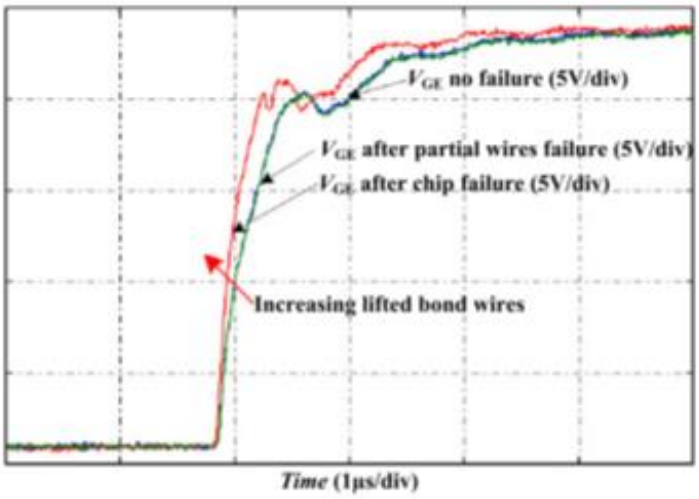


Figure 3.6: Variations of V_{GE} in the presence of BWLO [46]

Wang *et al*.[51] used $V_{CE,on}$ as an indicator of BWLO. They showed that a 10%-20% variation of $V_{CE,on}$ is a symptom of early BWLO. Baker *et al.* [52] suggested both i_G and $V_{CE,on}$ as the early failure detectors. They showed that these electrical parameters can be individually used to detect BWLO. In their paper, an external gate resistor, which is already present in most gate drive designs, is used as a gate current sensor. The results showed that the BWLO causes an increase in i_G and a decrease in $V_{CE,on}$ [46]. However, the effects of other failures such as gate oxide degradation on the variation of i_G are ignored. This is important as i_G decreases in the presence of gate oxide degradation whereas it increases in the presence of BWLO. Barlini, *et al.* [52] and Xue, *et al*, [53] used both the static (i_c) and switching (V_{GE}) parameters of IGBTs to detect BWLO.

Derivative di_C/d_t and V_{GE} have been calculated during a double pulse test in order to increase the accuracy of calibration between the electrical parameters to the BWLO in healthy mode [49]. However, variations of V_{CE} should be evaluated in the proposed method, as it directly affects the level of i_c. In fact, the relationship between i_c and T_j cannot be explained with a 2D model, since there is a direct relation between V_{CE} and i_c. Considering V_{CE} is also affected by temperature variations, to estimate T_j, both V_{CE} and i_c should be continuously measured. In order to uncouple the variation of T_j with the occurrence of the BWLO, an independent failure detector should be found [54].

3.2.3.2.4 Solder fatigue degradation

Barlini. *et al*, [52] and Lehmann. *et al*, [55] employed an in-situ circuit to evaluate the variation of $V_{GE,th}$ as a SF failure detector. They showed that an increase in $V_{GE,th}$ can be caused by additional thermal stresses within an IGBT. These variations are caused by an increase in the capacitance between the gate and the emitter terminals, which traps electrons in the gate oxide. This work did not been take place in an operational converter where$V_{GE,th}$ depends on additional parameters T_j, i_c and V_{CE} [56].

Therefore, it would be necessary to monitor T_j, i_c and V_{CE} in order to use $V_{GE,th}$ as the failure detector. In addition, it is not clear if $V_{GE,th}$ can be considered as an independent failure detector since the variations of $V_{GE,th}$ can originate from T_j rather than from the progress of the failure.

Fratelli, *et al.* [47] and Sankaran, *et al.* [57] proposed a technique to detect SF by means of the calculation of the junction-to-case thermal resistance ($R_{j\_c,th}$). They showed that the resistance can increase up to 20% in the presence of SF. As SF worsens, the thermal resistance between the solder and DCB layers increases because there is a progressive reduction of the effective surface area of the solder leading to increasing $R_{j\_c,th}$ according to equation (3.6).

$$R_{th} = \frac{L}{A \times k_{th}} \tag{3.6}$$

where L is layer thickness in mm, A is effective surface area (mm^2) and v is effective volume in m^3, k_{th} is thermal conductivity (W.m^{-1}.K^{-1}). The challenge for this method is that to obtain $R_{j\_c,th}$, the power losses and T_j should be calculated in order to use equation (3.7).

$$T_C - T_j = R_{th,j-C} \times P_{loss} \tag{3.7}$$

Xiang, *et al.* [60] proposed case temperature (T_C) as a SF detector. They have proposed monitoring the variation of T_C by inserting a thermocouple between the case and the heat sink. As R_{th} increases with the progress of failure, T_j increases and consequently T_C increases. However, a rise in temperature can be due to the load variations. That is why it is necessary to calibrate the T_C with different load variations in a healthy state to predict the expected temperature rise for a certain load. Any deviation from the expected value can indicate SF degradation but could also be caused by another failure mode. In fact, considering temperature rise of the IGBT (T_C or T_j) cannot be suggested to diagnose a particular degradation as almost all failure modes can affect the temperature of an IGBT [61]. Katsis *et al* [48] revealed that a 10% increase of $R_{j\_c,th}$ can be a symptom of the presence of a crack, as temperature distribution over the case-base plate becomes unbalanced. A longer crack also leads to faster expansion and the contraction between stress cycling and $R_{j\_c,th}$ is exponentially increasing with progress of the failure. However, the method did not consider the effect of other failures and the health condition monitoring of thermal grease on the variation of $R_{j\_c,th}$.

3.3.3 Model driven methods

Another method of health condition monitoring is based on electro-thermal and thermo-mechanical modelling of the IGBT module, since the variation of the temperature is caused by either mechanical or electrical stresses within the IGBT module structure. Electro-thermal modelling mainly refers to the definition of a thermally equivalent electrical RC circuit of the IGBT layers and an understanding of

the temperature variations of each layer for a certain applied heat power (from electrical losses). Thermo-mechanical modelling refers to modelling of the IGBT as a multi-layer structure and applying mechanical stresses (Von-Mises mechanical stress) [64] that cause mechanical failures such as lifting of the bond wires and SF.

3.3.3.1 Detection of the bond wire lift-off degradation

Estimation-based methods based on electro-thermal modelling cannot be applied to the detection of BWLO as they do not detect the occurrence failure at an early stage [65]. However, electro-thermal modelling can be used to estimate T_j by applying (3.7) [66]. In fact, BWLO only affects the current distribution from the die to the bond wires. The bond wires contribute little to the losses and, hence, heat within a device. With a small cross-sectional area, they do not contribute significantly to the heat transfer model, as such BWLO does not materially change temperature distribution. As a result, the only effective way to detect the BWLO is to monitor electrical parameters.

3.3.3.2 Detection of the solder fatigue degradation

Yun, *et al*. [67] and Kojima, *et al.* [68] used experimental data and infrared thermography techniques to calibrate a static 3-D finite element model of both a converter and its heatsink, with improved accuracy compared to 2-D, RC electrical models based only on heat transfer theory (further details of RC model appear in chapter 6). Yun, et al. [67] used a 3-D model to determine the temperature distribution across the layers of an IGBT. Based on the numerical results, the positional temperatures of the 3-D FEM result are used to generate a set of 2-D RC components for a thermal network model. A 2-D electro thermal model of the IGBT layer is used to extract an equivalent RC model according the obtained thermal constants and impedances. This model is developed so when applying a certain electric power T_j is estimated from the RC model of the IGBT. SF affects the thermal coupling between the die and contact pad. If there are voids between the layers, the effectiveness of heat transfer from die to the heatsink reduces, increasing the thermal impedance. Changing thermal impedance during a power cycle can indicate the presence of SF. Variation of thermal impedance has been considered as a SF detector. The time response of an RC thermal network is fast enough to show the thermal variation of the IGBT layers simultaneously. In addition, using an RC model reduces the computation time required to solve the IGBT thermal model, in comparison with using the 3-D finite-element models for the thermal network. However, the method still depends on the development of computational 3-D models for finding the thermal model RC component values (thermal resistances and time constants of the IGBT layers).

3.4 Residual lifetime prediction for IGBTs

The actual residual lifetime of IGBT modules can be significantly different from the manufacturer predictions as the actual temperature fluctuations (ΔT_j) and power cycles are application dependent. Understanding the residual lifetime of the IGBT in their working environment is a promising approach to reduce unplanned converter stoppages. Ageing causes the electrical characteristics of the IGBT to change and, hence, real-time IGBT health condition monitoring is necessary to allow reliable lifetime prediction. Defining the remaining lifetime of an IGBT is an important contribution to minimising the likelihood of premature failure.

Initially, temperature-cycling tests are used to correlate residual lifetime to temperature stresses which necessitate the estimation of T_j . Temperature cycling tests refer to the laboratory power cycling of IGBT modules at high and low temperatures when the modules are in their on- and off-states respectively. During these tests, both ΔT_j and the mean value of T_j need to be collected. The model includes not only ΔT_j, but also other parameters that can influence power losses, such as $T_{j,max}$ and the thermal duty cycle. The temperature fluctuations (ΔT_j) and maximum junction temperature, ($T_{j,max}$) are measured in real-time to find out the number of cycles, N_f. Figure 3.7 shows ΔT_j used for the comparative analysis of the lifetime algorithms, since the ΔT_j has the greatest impact on the IGBT reliability because of the thermal stresses between the IGBT layers with differing thermal expansion coefficients.

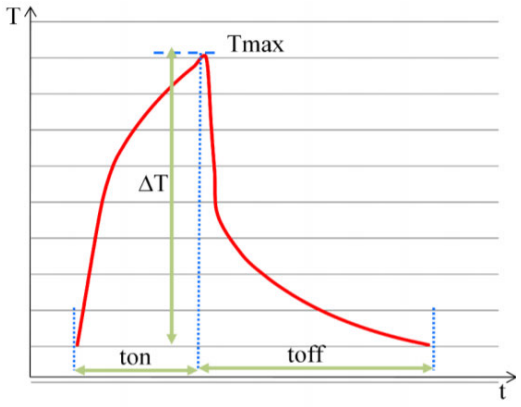


Figure 3.7: ΔT_j during a power cycle [68]

Direct measurement of T_j is difficult because of accessing the junction inside a module [68]. Data-driven methods provide an alternative approach to estimate T_j. When the converter is running, the temperature history is collected and use to compute N_f by using a cycle counting algorithms [69].

Using dedicated algorithms and (3.6), residual lifetime can be estimated from the measured data. However, the lifetime of an IGBT is so long in normal operating conditions that accelerated life testing is used to reduce the time taken for experiments. Accelerated life testing on the IGBT is applied by thermal and power cycling [50, 69].

These algorithms are based on accelerated life tests, where overstress conditions (high temperature, high temperature cycling, high power cycling, humidity, and so on) are applied to the module to understand the effects of these stresses on the external characteristics and the electrical parameters of IGBTs over a relatively short time. A health condition monitoring system will then monitor the stresses in normal conditions and calculate the residual lifetime over the correct time scale using the acceleration factor used for the test.

A residual lifetime model is typically obtained using the Palmgren-Miner rule [70]. The Palmgren-Miner's rule is one of the most widely used cumulative damage models for fatigue failures and it is probably the simplest cumulative damage model. This indicates that if there are k different stress levels and the average number of cycles to failure at the i_{th} stress, (S_i) is N_f, then the damage fraction, C, is calculated by (3.6). This equation can be assessed as the proportion of life consumed at each stress level and then adding the proportions for all the levels together. In general, failure occurs when the damage fraction reaches 1.

$$\sum_{i=1}^{k} \frac{n_i}{N_f} = C \tag{3.6}$$

- n_i is the number of cycles accumulated at stress S_i.
- C is the fraction of life consumed by exposure to the cycles at the different stress levels.

In this model, the lifetime consumption is calculated from the ratio between the total temperature cycle number and the number of cycles to failure. The former is obtained from a cycle counting algorithm, like the 'Rainflow algorithm' [71], the latter is calculated from one of the mathematical models listed in Table 3.2, for example the Coffin-Manson law [72]. The Rainflow algorithm extracts ΔT_j and the number of cycles from a load-time history containing peaks and valleys. Using the Miner rule, physical models are made for each fault. The residual lifetime is then estimated from the time history (time duration until the fault occurs) over the lifetime of the device. The drawback of using the model-based technique (Table 3.1) for residual lifetime estimation is that it can only be applied to predict the remaining time for certain degradation modes. In addition, developing a model to estimate residual lifetime for all possible combinations of degradation is unrealistic. Thus, the weakest part of an IGBT module, specifically bond wires and solder joints, are considered as the most important degradation modes for a model-based method. Models are available that represent increasingly complicated lifetime

models, introducing more and more parameters. The most common plastic-strain-based fatigue model is called the Coffin-Manson model, based on (3.1) [73].

The number of cycles to failure, N_f, is given by equation (3.1).

$$N_f = \alpha(\Delta T_j)^{-n} \tag{3.1}$$

where parameters α and n are constants determined by empirical curve fitting.

Variation ΔT_j is the junction temperature variation during IGBT operation. The exponent n generally lies between 1 to 3 for SF and between 3 and 5 for metal alloy fatigue [74]. In this method, only ΔT_j is taken into account, which may be a limiting factor for the model. The modified Coffin-Manson method introduces a factor relating to the mean temperature of junction temperature, $T_{j,mean}$, leading to (3.2)

$$N_f = \alpha(\Delta T_j)^{-n} \times e^{E_a/(K_B.T_{mean})} \tag{3.2}$$

where K_B is Boltzmann's constant, E_a is active energy of the deformation process, exponent n and α are derived from experimental fitting results [50].

The Norris-Landzberg model is derived from the modified Coffin-Manson model equation (3.3) [75].

$$N_f = \alpha f^{-n_2}(\Delta T_j)^{-n_1}.e^{E_a/(K_B.T_{mean})} \tag{3.3}$$

where K_B is Boltzmann's constant, f is frequency of the thermal cycle, E_a, exponent n and α can be derived by experiment.

The Bayerer model is a more comprehensive model that combines a power cycling test and IGBT module properties, given in (3.4). The physics-based models can be applied in three different stages to understand the health status as well as the residual lifetime of an IGBT [76].

$$N_f = k(\Delta T_j)^{\beta 1} \times e^{\beta_2/(T_{j,max}+273k)} \times t_{on}^{\beta_3} \times I^{\beta_4} \times V^{\beta_5} \times D^{\beta_6} \tag{3.4}$$

In (3.4), D is the bond wire diameter, V is blocking voltage of the IGBT, I is the DC current, K, β_1,…β_6 are extracted from experimental fitting data, and t_{on} is the heating time. ΔT_j is the temperature fluctuation and $T_{j,max}$ is the maximum T_j.

A summary description of different lifetime models is given in Table 3.1.

Table 3.1: Comparison of different lifetime models

Analytical lifetime model	Model parameters	Model variables
Coffin-Manson model [75]	a, n	ΔT_j
Modified Coffin-Manson model [75]	a, n, E_a	ΔT, $T_{j,max}$
Norris-Landzberg model [76]	A, n_1, n_2, E_a	ΔT_j, $T_{j,max}$, f
Bayerer model [76]	K, β_1, β_2, β_3, β_4, β_5, β_6	ΔT, $T_{j,max}$, t_{on}, I, V, D

Various residual lifetime algorithms for different applications and module characteristics have been developed, listed in Table 3.2. Quantity V is voltage, T_j is temperature, J is current density and ΔH is humidity. These data are provided by measurement of the inherent electrical parameters as discussed in section 3.3.2.2.1. On-line data from an IGBT module is used to parameterise a lifetime model.

Table 3.2: Comparison of failure mechanisms in IGBTs [9]

Failure mechanisms	**Failures**	**Input of cycle counting algorithm**	**Lifetime models**
Bond wire fatigue	Bond pads and bond wires	T_j, ΔH, $T_{j,max}$, dT_j/dt	Coffin-Manson [75] Norris-Landzberg [75] Bayere [76]
Solder joint fatigue	Die-attach solder and DCB solder		
Ceramic cracks	DCB substrate		
Time dependent dielectric breakdown	Dielectric layers	T_j and V	Arrhenius [9]
Electro-migration	Metallization	J and T_j	Eyring [65]

Yang, et al [78] and Kovacevic, *et al*., [79] suggest that none of these models is truly compatible with experimental results. The wear out process is complex and can involve combinations of failure mechanisms. It is difficult to create a universal model applicable to all possible failure modes [80]. Alternatives to the Rainflow cycle counting algorithm are studied and compared in terms of accuracy and complexity in [82-83]. There is no commercially available health condition monitoring system for IGBT-based converters applicable during the normal operation of a WT converter. Many lab-based research experiments have been conducted to monitor the health of IGBTs through monitoring temperature and/or other failure detection parameters or based on numerical modelling analysis.

Since almost all failure mechanisms affect the temperature profile of an IGBT, T_j is not an adequate failure detector to distinguish the root causes of a failure. Therefore, it is necessary to estimate T_j through an independent temperature estimation approach. Detecting premature failures through failure detector parameters without considering T_j is not a reliable approach, since the variation of failure detector parameters changes T_j and variations in operating condition can change, based on analysis of Table 3.3 and Table 3.4. Determination of the exact root cause of failure mechanisms is still the main

issue for health condition monitoring systems. This is because fault mechanisms can occur at the same time and mutually interfere, resulting in misleading information being transferred to the monitoring system. Additionally, there is no comprehensive approach applicable to different IGBT types and new calibration is required whenever a different IGBT module type is used, significantly increasing the cost of a health condition monitoring system.

Apart from temperature, many external factors can contribute to false alarms and thus render a health condition monitoring system unreliable. Examples of such factors are: IGBT gate driver failures; cooling system failure; and load (wind speed) variations. The complexity comes from the non-linear relationships between the failure detectors and the ageing of the IGBT. This makes it difficult to find a relationship between failure detectors and the different parameters that can cause the failures.

A clear area of development would be to overcome this problem by monitoring a combination of different variables in conjunction with a suitable algorithm. Analysis of the simultaneous variation of and cross-correlations between a multiplicity of monitored variables would be used to identify the most probable root cause of failure. For example, if the monitored variables are $V_{GE,th}$, R_{CE} and T_C, an increase of R_{CE} while T_C and $V_{GE,th}$ remain near constant is a likely symptom of early BWLO, as discussed previously. Alternatively, an increase of T_C and $V_{GE,th}$ without significant variation in R_{CE} would be a symptom of SF. For the successful implementation of the above methods it is essential that a pre-calibration is performed to understand the sensitivity of each variable to the chosen fault mechanism, and their level of correlation, as well as a characterisation of these sensitivities for different load conditions. It is anticipated that these algorithms will require a significant computational effort due to the complex relationships between the failure detectors and actual ageing of the IGBT. Algorithms based on artificial intelligence could be used to tackle the problem associated with the non-linearity. These algorithms are particularly useful when the mathematical relationships between causes and effects are not well-known or are expressed in a complex way. However, almost all failure mechanisms can increase the temperature of an IGBT. In this case, T_j changes due to the occurrence of other failures and not only gate oxide degradation. In addition, there is a lack of research on switching time variations for three-phase converters feeding inductive loads.

3.5 Discussion and Summary

Table 3.3 summarises the main characteristics of the health condition monitoring methods and gives indications of their main field of application, their advantages, implementation difficulties.

Table 3.3: Comparison of health condition monitoring methods in an IGBT

Techniques	Failure mechanism	Requirements	Perceived advantages	Perceived limitations	Identification or Indicator	Ref
Model driven method	-Thermal fatigue	-FEM software	-Accurate prediction of temperature	Computational cost and time	-Thermal model	[7],[46]
	-Thermal model -Gate driver	- Additional sensor	-Easy measurement	-Accuracy of thermal model -Distinguish of fault's type -Accuracy of temperature sensor	-Heatsink modelling	[31], [52], [8]
Direct based	-BWLO, - SF	-Additional sensor	-Reliable and accurate	-Required modification in IGBT module	-T_j (+10%)	[25], [27]
Inherent failure detector parameters	-BWLO	-Embedded measurement circuit - Additional sensor -fast sampling time	-Distinguish of fully lift-off -Applicable within operation of system	-Influence by both IGBT and driver -Sampling time	-Gate current (decrease)	[12], [17]
	-SF -Short circuit -latch up -Wire bond degradation -Die attach degradation	-Embedded measurement circuit -sensors	-Applicable within operation of system	-Distinguish of fault's type and unhealthy part -Capture of small variation in fast switching	-$V_{CE,on}$ (+5% -10%-20%)	[16], [17], [18], [19]
	-Gate degradation -Short circuit - Latch up - Wire bond degradation	-Embedded measurement circuit -Sensors -External signal to gate	-Indicator of gate oxide degradation	-Applicable in off line mode of system -Required modification in IGBT module	$V_{GE,th}$ (+11%)	[67]
	-SF and cracking	-Electro thermal and thermo electrical modelling		-Expensive -Time consuming	$R_{th,j-c}$ (+20%)	[33]
Model driven method	-Thermal fatigue	-FEM software	-Accurate prediction of temperature	-Computational cost and time	-Thermal model	[35], [7],
	-Thermal model-Gate driver	- Additional sensor	-Easy measurement	-Accuracy of thermal model -Distinguish of fault's type -Accuracy of temperature sensor	-Heatsink modelling	[31], [52], [8]
Others	-SF	-Embedded measurement circuit to amplify harmonic	-No additional sensor	-Distinguish of fault's type -Complicated algorithm	-Current harmonics amplitude	[50], [56]
	-Thermal increase -Power losses of converters	-Embedded measurement circuit	-No additional sensor -Estimation of T_j	-Accuracy of power loss estimation -Distinguish of fault's type	-Control of converter efficiency	[36]

The different failure mechanisms can be detected by looking at specific parameters, but often research papers have shown that the variation of a specific parameter can be the symptom of multiple causes. Therefore, it is quite difficult to classify the methods of failure detection. An attempt has been made to group together different methods used for failure detection and compare them on the basis of specific performance criteria in Table 3.4. The table presents a comparison of different failure detectors in terms of accuracy, linearity and sensitivity. For each column the detector has been scored with a value from 1 (worst) to 6 (best). A positive sign (+) shows positive sensitivity of failure detector to the progress of failure and negative sign (-) shows negative sensitivity of the failure detector to the progress of failure.

Table 3.4: Failure mechanisms of IGBTs and their failure indicator parameters

	Failure Indicators	Accuracy	Linearity	On-line	Sensitivity	Symptom	Ref
BWLO	$V_{CE,on}$	3	3	4	6	+10%, +20%	[38], [32]
	i_C	5	3	4	6	increase	[65], [66]
	T_C	2	4	5	4	+10%	[48], [67]
	5th current harmonic	6	1	6	5	increase	[49]
	$I_{leakage,GE}$	1	2	1	1	increase	[68]
	$V_{GE,th}$	3	3	2	2	+11%	[69]
	V_{GE}	2	3	3	2	decrease	[46], [70]
	i_G	4	3	2	2	increase	[71], [45]
	i_{sc}	7	4	5	6	-4.5%	[34], [72], [73]
	R_{CE}	7	3	4	6	+15%	[58]
	$R_{j-c,th}$	3	3	5	3	+10%	[57], [74]
SF	$R_{j-c,th}$	3	2	3	4	+20%	[58]
	5th current harmonic	2	1	3	1	-3% to -5.5%	[64]
	$V_{GE,th}$	1	2	1	2	+11%	[46]
	T_C	4	3	4	4	+1.57° C	[62]
	$V_{CE,on}$	1	2	2	3	-17%	[44]
Gate oxide	$V_{GE,th}$	2	2	2	2	+11%	[69]
	$i_{GE,leakage}$	3	1	1	2	+sharp increase	[75], [71]
	$V_{CE,on}$	1	2	3	1	-13%	[76]
Corrosion	$V_{CE,on}$	1	2	1	2	+10%	[63], [75]
	$i_{GE,leakage}$	2	1	2	1	+sharp increase	[9], [27]

Electrical failure detectors are often used to estimate the temperature.. However, to use them as temperature detectors, a calibration process and fitting between temperature and measured failure detectors (TSEPs) should be done beforehand. Methods using an estimate of T_j are preferred to those requiring direct measurement of T_j, as they do not require modifications to the internal structure of an IGBT. The improvement of models and algorithms for the analysis of indirect measurements have meant that indirect methods are achieving the same level of accuracy as their direct method counterparts, even when detection of a rapid change in T_j is required [62].

On the other hand, TSEP-based methods have drawbacks in terms of practical implementation and reliability. This is because, particularly for wind power generation, the IGBTs operate with variable mechanical vibrations, ambient temperatures, loads, switching frequencies and duty cycles. Since these conditions are not easily predictable, conflicting information is collected and this may result in the health condition monitoring system issuing false alarms. The efficiency of TSEPs methods can be improved by aggregating test results to improve the signal to noise ratio. TSEPs methods invariably require specialised on-line sensors that are generally expensive. The methods based on finite-element thermal modelling require specialised software, which is expensive. The commissioning phase of finite element modelling is also time-consuming due to requirement for defining and applying accurate meshing of the system and the initialization of variables. Additionally, the pre-calculation of power losses, achieved by the finite element thermal analysis, is required for a large number of IGBT operating conditions. With regard to implementation, these methods require the measurement of converter power losses, which may require additional dedicated sensors. The methods based on converter output quantities such as odd harmonic content [69] and RC modelling of the different layers of the IGBT require numerical modelling of thermal resistance and knowing the time constants for the IGBT layers.

Sensor-based methods require expensive temperature sensors, such as IR cameras, which require an accurate initial calibration. Additionally, they are difficult to implement as the sensors should be placed inside the IGBT modules. The benefit is the absence of pre-calculations and a reduction in the requirement for computational capabilities. TSEP-based methods require additional sensors, but they are cheaper than IR cameras as they measure only electrical quantities. Additionally, fast signal processors are required as electrical quantities need to be sampled faster than the switching frequency of the converter. The commissioning phase requires a pre-calibration of the relationship between inherent failure detectors and T_j.

3.6 References

[1] S. Fu, Y. Mei, X. Li and G.-Q. Lu, "Reliability Evaluation of Multichip Phase-Leg IGBT Modules Using Pressureless Sintering of Nanosilver Paste by Power Cycling Tests," *IEEE Trans on Power Electro*, Vol. 32, no. 8, pp. 6049 - 6058, Aug 2017.

[2] U.-M. Choi, S. Jørgensen and F. Blaabjerg, "Advanced Accelerated Power Cycling Test for," *IEEE Trans on power electro*, Vol. 31, (12), pp. 8371-8386, Dec 2016.

[3] H. Luo, Y. Chen, P. Sun, W. Li and X. He, "Junction Temperature Extraction Approach With Turn-Off Delay Time for High-Voltage High-Power IGBT Modules," *IEEE Trans on Power Electro*, Vol. 31, (7), pp. 5122 - 5132, Jul 2016.

[4] K. Fischer, F. Besnard and L. Bertling, "Reliability-Centered Maintenance for Wind Turbines Based on Statistical Analysis and Practical Experience," *IEEE Trans on Energy Conversion*, Vol. 27, (1), pp. 184 - 195, Mar 2012.

[5] D. Astigarraga, F. Martin Ibanez, A. Galarza, J. M. Echeverria, I. Unanue, P. Baraldi and E. Zio, "Analysis of the Results of Accelerated Aging Tests in Insulated Gate Bipolar Transistors I," EEE Transactions on Power Electronics, vol. 31, no. 11, pp. 7953 - 7962, 2016.

[6] K. Takashi, Y. Yamada, M. Ciappa, M. Chiavarini and W. Fichtner, "A novel electro-thermal simulation approach of power IGBT modules for automotive traction applications," *in PCIM Europe*, 2017.

[7] P. Ghimire, A. Ruiz de Vega, S. Be¸czkowski, B. Rannestad, S. Munk-Nielsen, and P. Thøgersen, "Improving Power Converter Reliability: Online Monitoring of High-Power IGBT Modules," *IEEE Industrial Electro Magazine*, Vol. 8, (3), pp. 40 - 50, Sept 2014.

[8] L. Condra, S. O'Rear, T. Freedman, L. Flancia, M. Pecht and D. Barker "Comparison of plastic and hermetic microcircuits under temperature cycling and temperature humidity bias," *IEEE Trans on Components, Hybrids, and Manufacturing Technology*, Vol. 15, (5), pp. 640 - 650, Oct 1992.

[9] H. WANG, M. LISERRE and F. BLAABJERG, "Toward Reliable Power Electronics: Challenges, Design Tools, and Opportunities," *IEEE Industrial Electronics Magazine*, vol. 7, no. 2, pp. 1932-4529, 2013

[10] S. Zhou, L. Zhou b, S. Liu, Q. Luo, P. Sun and J. Wu, "Monitoring chip fatigue in an IGBT module based on grey relational analysis," *Microelectronics Reliability, ELSEVIER*, vol. 56, pp. 49-52, Jan 2016.

[11] H. T. Jadhav and R. Roy, "Gbest guided artificial bee colony algorithm for environmental/economic dispatch considering wind power", Vol. 40, no. 16, p. 6385–6399, Nov. 2013.

[12] W. S. Loh, P. A. Agyakwa, C. M. Johnson, T. K. Loh, C. Luechinger and K. Oftebro, “Thick Al ribbon interconnects: A feasible solution for power devices packaging,” Symp. Micro, Providence, RI, pp. 1056–1063, 2008.

[13] V. Khanna, Insulated gate bipolar transistor IGBT theory and design, John Wiley & Sons, 2004.

[14] A. S. Bahman, F. Iannuzzo, C. Uhrenfeldt, F. Blaabjerg and S. Munk-Nielsen, “Modeling of Short-Circuit-Related Thermal Stress in Aged IGBT Modules,” *IEEE Trans on Industry Appls,* vol. 53, no. 5, pp. 4788 - 4795, Sept-Oct 2017.

[15] M. A. Eleffendi and C. M. Johnson, “Application of Kalman Filter to Estimate Junction Temperature in IGBT Power Modules,” *IEEE Trans on Power Electro,* vol. 31, no. 2, pp. 1576 - 1587, Feb. 2016.

[16] N. Chen, F. Chimento, M. Nawaz and L. Wang, “Dynamic Characterization of Parallel-Connected High-Power IGBT Modules,” IEEE Trans on Industry Appl, vol. 51, no. 1, pp. 539 - 546, Jan Feb 2015.

[17] L. Kongjing, Y. T. Gui, L. Cheng, A. Yin, C. Wenping and S. Crichton, “State Detection of Bond Wires in IGBT Modules Using Eddy Current Pulsed Thermography,” *IEEE Trans on Power Electro,* vol. 29, no. 9, pp. 5000 - 5009, Sept 2014.

[18] C. G and R. Lallemand, “Failure criteria for long term accelerated power cycling test linked to electrical turn off SOA on IGBT module’. A4000 h test on 1200 A-3300 V module with AlSiC base plate,” Micro. Rel Elsevier, vol. 40, no. 8-10, pp. 1665-1670, 2002.

[19] U.-M. Choi, F. Blaabjerg and S. Jørgensen, “Study on Effect of Junction Temperature Swing Duration on Lifetime of Transfer Molded Power IGBT Modules,” IEEE Trans on Power Electronics, Vol. 32, no. 8, pp. 6434 - 6443, Aug 2017.

[20] R. Bayerer, T. Herrmann, T. L. J. Licht, Feller and M. M., “Model for power cycling lifetime of IGBT modules-various factors influencing lifetime,” *Integrated Power Systems (CIPS*), pp. 1-6, 2008.

[21] L. Dupont and Y. Avenas, “Preliminary Evaluation of Thermo-Sensitive Electrical Parameters Based on the Forward Voltage for Online Chip Temperature Measurements of IGBT Devices,” *IEEE Trans on Industry Applications,* vol. 51, no. 6, pp. 4688 - 4698, 2015.

[22] L. Chen and H. Jiang, “Synchronous laser scanning IR imaging for chip bonding defect inspection“, *In Electronic Packaging Technology (ICEPT),* in *Int Confon IEEE,* 2016 .

[23] E. Baygildina, L. Smirnova, R. Juntunen, K. Murashko, A. Mityakov, M. Kuisma, O. Pyrhönen, P. Peltoniemi, K. Hynynen, V. Mityakov and . S. Sapozhnikov, “Condition Monitoring of Wind Power Converters Using Heat Flux Sensor,” in *IEEE Energy Conversion Congress and Exposition (ECCE),* 2015.

[24] G. Breglio, A. Irace, E. Napoli, M. Riccio and P. Spirito, "Experimental detection and numerical validation of different failure mechanisms in IGBTs during unclamped inductive switching," *IEEE Trans Electron Devices,* vol. 60, no. 2, pp. 563 - 570, Feb 2013.

[25] L. Zhou, S. Zhou and M. Xu, "Investigation of gate voltage oscillations in an IGBT module after partial bond wires lift-off," *Microelectronics Reliability, Elsevier,* vol. 53, no. 2, p. 282–287, Feb 2013.

[26] H. Deng, F. Xiao, Y.Luoa, Y. Jia, Y. Duan, "Simulation Research on IGBT Thermal Impact of Solder Voids Based on Fractal Theory", *IEEE Int Power Electro and Appl Conf and Exposition,* 2018.

[27] E. Herr, T. Frey, R. Schlegel, A. Stuck and R. Zehringer, "Substrate-to-base solder joint reliability in high power IGBT modules", Vol. 37, (10–11), *Micro Rel in Elsevier journal,* Oct–Nov 1997, pp. 1719-1722.

[28] E. Kostandyan, J. D. Sørensen, "Reliability of Wind Turbine components - Solder elements fatigue failure", Proceedings Annual Reland Maintainability 2012.

[29] J-P. Sommer, T. Licht, H. Berg, K. Appelhoff and B. Michel, "Solder fatigue at high-power IGBT modules", 4th Int Conf on Integrated Power Systems, Jun 2011.

[30] A. Alghassi, S. Perinpanayagam and . M. Samie;, "Stochastic RUL Calculation Enhanced With," *IEEE Trans on rel,* vol. 65, no. 2, pp. 558 - 573, Jun 2016.

[31] H. Luo, Y. Chen, P. Sun, W. Li and X. He, "Junction Temperature Extraction Approach With Turn-Off Delay Time for High-Voltage High-Power IGBT Modules," IEEE Trans on Power Electro, vol. 31, no. 7, pp. 5122 - 5132, Jul 2016.

[32] C. Zorn and N. Kaminski, "Acceleration of temperature humidity bias (THB) testing on IGBT modules by high bias levels," in Power Semiconductor Devices & IC's (ISPSD), May 2015.

[33] N. Patil, J. Celaya, D. Das, K. Goebel and M. Pecht, "Precursor parameter identification for insulated gate bipolar transistor (IGBT) prognostics", IEEE Trans on Rel, Vol. 58, (2) , pp 271 - 276, Jun 2009.

[34] U. Karki, and F Zheng Peng , "Effect of Gate-Oxide Degradation on Electrical Parameters of Power MOSFETs", IEEE trans on power electronics, Vol. 33, (12), Dec 2018.

[35] J. Liu, G. Zhang, Q. Chen, L. Qi, Z. Qin, J. Wang, Y. Geng "Online Junction Temperature Extraction and Aging Detection of IGBT via Miller Plateau Width" IEEE Applied Power Electro Conf and Exposition (APEC), Mar, 2018.

[36] J. Liu, G.Zhang, Q. Chen, L. Qi , Y.Geng and J. Wang "In situ Condition Monitoring of IGBTs Based on the Miller Plateau Duration", IEEE Trans on Power Electro, Vol. 34, (1), Jan. 2019.

[37] P. Tu, P. Wang, X. Hu, . C. Qi and S. Yin, "Analytical evaluation of IGBT turn-on loss with double pulse testing," in *Industrial Electronics and Applications (ICIEA),* Jun. 2016.

[38] D. C. Katsis and J. D. van Wyk, “Thermal, mechanical, and electrical study of voiding in the solder die-attach of power MOSFETs,” *IEEE Trans. Compon. Packag. Technol,* vol. 29, no. 1, p. 127–136 , Mar 2006.

[39] J. Lehmann, M. Netzel, R. Herzer and S. Pawel, “Method for electrical detection of bond wire lift-off for power semiconductor,” in Int Symp. Power Semicond, Devices IC’s, 2003.

[40] H. Wang, M. Liserre, F. Blaabjerg, P. de Place Rimmen, J. B. Jacobsen, T. Kvisgaard and . J. Landkildehus, “Transitioning to Physics-of-Failure as a Reliability Driver in Power Electronics,” IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 2, no. 1, pp. 97 - 114, 2014.

[41] L. Dupont, Y. Avenas and P. Jeannin, “Comparison of junction temperature evaluations in a power IGBT module using an IR camera and three thermos sensitive electrical parameters,” *IEEE Trans on Industry Appl*, vol. 49, no. 4, pp. 1599-1608, 2013.

[42] Y. Chen, H. Luo, W. Li, F. Iannuzzo and F. Blaabjerg, “Analytical and Experimental Investigation on A Dynamic Thermo-Sensitive Electrical Parameter With Maximum dIC/dt During Turn-OFF for High Power Trench Gate/Field-Stop IGBT Modules,” *IEEE Trans on Power Electro,* vol. 32, no. 8, pp. 6394 - 6404, 2017.

[43] B. Gao, F. Yang, M. Chen, . L. Ran, I. Ullah, S. Xu and. P. Mawby, “A Temperature Gradient-Based Potential Defects Identification Method for IGBT Module,” *IEEE Trans on Power Electro,* vol. 32, no. 3, pp. 2227 - 2242, 2017.

[44] K. B. Pedersen and K. Pedersen, “Dynamic Modelling Method of Electro-Thermo-Mechanical Degradation in IGBT Modules,” IEEE Trans on Power Electro, vol. 31, no. 2, pp. 975 - 986, 2016.

[45] D. Barlini, M. Ciappa and M. Mermet-Guyennet, “Measurement of the transient junction temperature in MOSFET devices under operating conditions,” *Microelectronics Reliability, Elsevier,* vol. 47, no. 9-11, p. 1707–1712, 2007.

[46] A. S. Bahman, K. Ma, P. Ghimire, F. Iannuzzo and F. Blaabjerg, “A 3-D-Lumped Thermal Network Model for Long-Term Load Profiles Analysis in High-Power IGBT Modules,” *IEEE journal of emerging and selected topics in power electronics,* Vol. 4, no. 3, pp. 1050 - 1063, Sep 2016.

[47] L. Fratelli, G. Giannini, B. Cascone and G. Busatto, “Reliability test of power IGBT’s for railway traction,” *Conf. Power Electro*. Appl, 1999.

[48] C. Busca, R. Teodorescu, F. Blaabjerg, Munk-Nielsen, S, L. Helle and T. Abeyasekera, “An overview of the reliability prediction related aspects of high power IGBTs in wind power applications,” *Microelectronics reliability,* vol. 51, no. 9, pp. 1408 - 1413, 2011.

[49] U.-M. Choi, F. Blaabjerg, S. Jørgensen, S. Munk-Nielsen and B. Rannestad, "Reliability Improvement of Power Converters by Means of Condition Monitoring of IGBT Modules," *IEEE Trans on Power Electro*, vol. 32, no. 10, pp. 7990 - 7997, 2017.

[50] Z. Sarkany, W. He and M. Rencz, "Temperature change induced degradation of SiC MOSFET devices," *15th IEEE Intersociety Conf*, May 2016.

[51] Z. Wang, B. Tian, W. Qiao and L. Qu, "Real-Time Aging Monitoring for IGBT Modules Using Case Temperature," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 2, pp. 1168-1178, 2016.

[52] N. Baker, L. Dupont, S. Munk-Nielsen, F. Iannuzzo and M. Liserre, "IR Camera Validation of IGBT Junction Temperature Measurement via Peak Gate Current," *IEEE Transactions on Power Electronics*, vol. 32, no. 4, pp. 3099-3111, 2017.

[53] D. Barlini, M. Ciappa and M. Mermet-Guyennet, "Measurement of the transient junction temperature in MOSFET devices under operating conditions," *Microelectronics Reliability, Elsevier*, vol. 47, no. 9-11, p. 1707–1712, 2007.

[54] P. Xue, G. Fu and D. Zhang, "Modeling Inductive Switching Characteristics of High-Speed Buffer Layer IGBT," *IEEE Trans on Power Electronics*, vol. 32, no. 4, pp. 3075 - 3087, Apr 2017.

[55] M. Lotfi and D. Zohir, "Modelling Inductive Switching Characteristics of High-Speed Buffer Layer IGBT Measurement of the transient junction temperature in MOSFET devices under operating conditions", *Int Journal of Hybrid Information Techno,* Vol.9, No.1 (2016), pp. 141-152.

[56] J. Lehmann, M. Netzel, R. Herzer and S. Pawel, "Method for electrical detection of bond wire lift-off for power semiconductor," *in Int Symp. Power Semicond*, Devices IC's, 2003.

[57] L. Fratelli, G. Giannini, B. Cascone and G. Busatto, "Reliability test of power IGBT's for railway traction," in Conf. Power Electron. Appl., 1999.

[58] V. Sankaran and X. Xu, "Integrated power module diagnostic unit". U.S. Patent 5528446, 1996.

[59] D. Xiang, L. Ran, P. Tavner, S. Yang, A. Bryant and P. and Mawby, "Condition monitoring power module solder fatigue using inverter harmonic identification," IEEE Trans Power Electron, vol. 27, no. 1, p. 235–247, Jan 2012.

[60] D. C. Katsis and J. D. van Wyk, "Thermal, mechanical, and electrical study of voiding in the solder die-attach of power MOSFETs," IEEE Trans. Compon. Packag. Technol., vol. 29, no. 1, p. 127–136 , Mar 2006.

[61] A. E. Ginart, D. Brown, P. W. Kalgren and M. J. R, "Online ringing characterization as a diagnostic technique for IGBTs in power devices," IEEE Trans. Instrum. Meas, vol. 58, no. 7, p. 2290–2299, Jul 2009.

[62] D. Mingxing, W. Kexin, L. Jian and X. and Linlin, “Condition monitoring IGBT module bond wire lift-off using measurable signals,” in *Power Electronics and Motion Control Conf. (IPEMC)*, 2012.

[63] A. Hamidi, N. Beck, K. Thomas and E. Herr, “Reliability and lifetime evaluation of different wire bonding technologies for high power IGBT modules,” Microelectronics reliability , vol. 39, no. 6-7, pp. 1153-1158, 1999.

[64] C. Yun, P. Malberti, M. Ciappa and W. Fichtner, “Thermal component model for electro-thermal analysis of IGBT module systems’. Advanced Packaging,” *Transactions on IEEE,* vol. 24, no. 3, pp. 401-406, 2001.

[65] M. Riccio, G. D. Falco, P. Mirone, L. Maresca, M. Tedesco, G. Breglio and A. Irace, “Accurate SPICE Modeling of Reverse-Conducting IGBTs Including Self-Heating Effects,” *IEEE Trans on Power Electronics*, vol. 32, no. 4, pp. 3088 - 3098, Apri 2017.

[66] U-M. Choi, F. Blaabjerg and S. Jørgensen, “Study on Effect of Junction Temperature Swing Duration on Lifetime of Transfer Molded Power IGBT Modules*,” IEEE Trans on Power Electronics*, vol. 32, no. 8, pp. 6434 - 6443, Aug 2017.

[67] S. Daliento, A. Chouder, P. Guerriero, A. Massi Pavan, A. Mellit, R. Moeini, and P. Tricoli, “Monitoring, Diagnosis, and Power Forecasting for Photovoltaic Fields: A Review”. Inter Journal of Photoenergy, Jan 2017.

[68] C. Yun, P. Malberti, M. Ciappa and W. Fichtner, “Thermal component model for electro-thermal analysis of IGBT module systems’. Advanced Packaging,” Transactions on IEEE, vol. 24, no. 3, pp. 401-406, 2001.

[69] T. Kojima, Y. Yamada, M. Ciappa, M. Chiavarini and W. Fichtner, “A novel electro-thermal simulation approach of power IGBT modules for automotive traction applications,” R&D Review of Toyota CRDL, vol. 39, no. 4, pp. 27-32, 2016.

[70] Z. Sarkany, W. He and M. Rencz, “Temperature change induced degradation of SiC MOSFET devices,” in 15th IEEE Intersociety Conf, May 2016.

[71] M. Pecht and R. Jaai, "A prognostics and health management roadmap for information and electronics-rich systems," Microelectronics Reliability, vol. 50, pp. 317-323, 2010.

[72] R. Mancini. “Op Amps for Everyone Design Reference (Rev. B) - Texas Instruments”. in 2002, available at https://web.mit.edu/6.101/www/reference/op_amps_everyone.pdf

[73] M.Musallam , C. M. Johnson, C. Yin , C. Bailey and M. Mermet-Guyennet Real-time life consumption power modules prognosis using on-line rainflow algorithm in metro applications”, IEEE Energy Conversion Congress and Exposition, 2010.

[74] B. Baker, “Techniques that Reduce System Noise in ADC Circuits”, 2010.

[75] Low Level Measurements Handbook: Precision DC Current, Voltage, and Resistance Measurements, 6th edition ed.: Keithley, 2004.

[76] R. C. Blish Ii, "Temperature cycling and thermal shock failure rate modeling," Proceedings of the 35th Annual IEEE International Reliability Physics Symposium,1997, pp. 110-117.

[77] IET Digital Library, "Author Guide - IET Research Journals," in Nov 2014, available at http://digital-library.theiet.org/journals/author-guide.

[78] F. Kovačević, Drofenik, and J. W. Kolar, "New physical model for lifetime estimation of power modules," in Power Electronics Conference (IPEC), 2010, pp. 2106-2114.

[79] S. Yang, D. Xiang, A. Bryant, P. Mawby, L. Ran and P. Tavner, "Condition Monitoring for Device Reliability in Power Electronic Converters: A Review," IEEE Transactions on Power Electronics, vol. 25, no. 11, pp. 2734 - 2752, Nov. 2010.

[80] Q. Jin and J. B. Bernstein, "Non-arrhenius temperature acceleration and stress dependent voltage acceleration for semiconductor device involving multiple failure mechanisms," IEEE International Integrated Reliability Workshop Final Report, IIRW, 2006, pp. 93-97.

[81] G. Vachtsevanos, *et al*, "Intelligent fault diagnosis and prognosis for engineering systems", *Hoboken (NJ): John Wiley & Sons*, Inc., 2006.

[82] A. T. Bryant, P. A. Mawby, P. R. Palmer, E. Santi, and J. L. Hudgins, "Exploration of power device reliability using compact device models and fast electro-thermal simulation", *IEEE Industry Appl Conf- Forty-First IAS Annual Meeting*, 2006, pp. 1465-1472.

Chapter 4: Experimental set up

4.1 Introduction

Significant parts this chapter appear in the proceedings of the IET renewable power generation journal (Moeini, Pietro, Hemida and Baniotopoulos) and WINERCOST'16 Conference (Moeini, Pietro, Hemida and Baniotopoulos, 2016), with appropriate referencing .

A three-phase converter was designed and constructed to carry out experimental tests on health condition monitoring techniques for IGBTs. This chapter describes the procedure followed for building the converter and validating its controller. The chapter is divided into two sections: the power board and controller board. The power part of the converter includes the IGBT's specification, the heatsinks and the DC-link. The controller board part summarises the design of the gate driver for the IGBTs, the microcontroller that includes firmware and controller signals, the encoder that measures the rotor position and the serial communication system (UART). The converter is used in the following chapter for calibration of the IGBT electrical parameters in healthy and unhealthy states. The feasibility of monitoring the parameters within operation of three-phase converter is practically studied in chapters 5 and 6.

4.2 Design of a conventional three-phase converter for use in the laboratory

A three-phase converter has been designed and constructed to drive a small WT as a generator or motor.. The design of the converter is divided into two main sections: the power part and the controller part. The power part is divided into two sub-sections. The first sub-section is the design of hardware components (4.2.1). The second sub-section describes the implementation of the power part (4.2.2). The controller part of the converter is explained in section 4.2.5.

4.2 Design of the hardware

This section introduces the hardware components used in the converter such as the IGBTs, the gate drivers and heatsinks [1].

4.2.1 IGBT under test

An N-channel half bridge IGBT module (VS-50MT060WHTAPbF), Appendix A [2] was selected for the converter, and its main data are shown in Table 4.1. This particular IGBT module provides easy access inside the module, enabling the bond wires to be cut to simulate BWLO. The IGBT module is filled with silicone gel to protect the IGBT module from dust and humidity.

Table 4.1: Selected IGBT specifications

$V_{CE,off}$	$V_{CE,on}$ at 15 V V_{GE}	I_C at 100ºC
600 V	2.3 V	50 A

Silicone gel is also used to avoid short circuits of bond wires. Having half bridge IGBT modules allows each leg of the converter to be studied independently. The electrical diagram of internal components of on half bridge module is shown in Figure 4.1. Two chips are placed in parallel for the high side and low side devices to increase the output current. A freewheeling diode is placed in parallel with the high and low sides of the IGBT and there are internal 10 Ω resistors in series with the gates of all IGBTs. Figure 4.1 also shows the physical dimension of the IGBT module under test in this work.

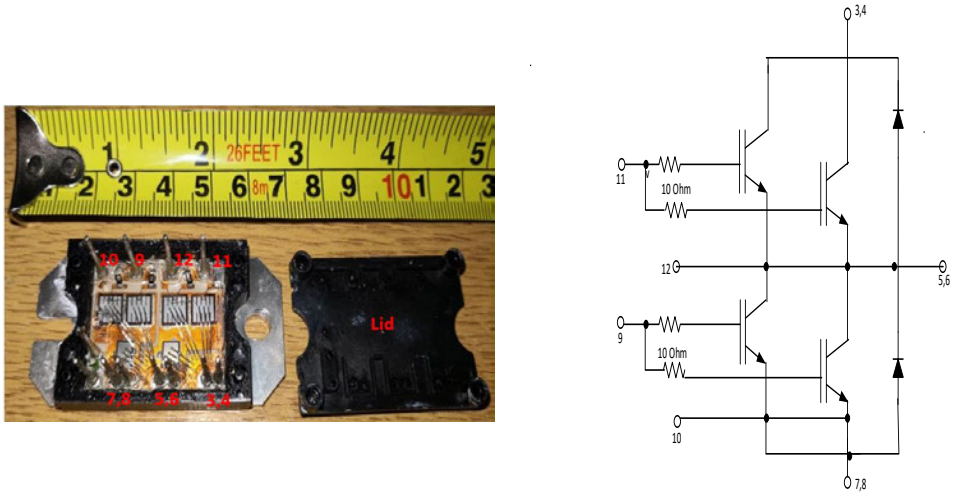


Figure 4.1: (a) The physical half bridge IGBT module; (b) Electrical diagram of the IGBT module

4.2.1.1 Gate drivers

The high side IGBT requires its gate voltage to be referenced to a higher voltage than the low side IGBT. A gate driver is a power amplifier that accepts a low input voltage and current from a

microcontroller and produces a high current and sufficient voltage to drive the gates of the IGBTs. A driver for high side IGBTs also offsets the high side gate voltage to a higher voltage, e.g. using the bootstrap principle [2]. The gate driver circuit is designed to drive the IGBTs according to their required switching times [3]. Most importantly, gate driver supplies or sinks the significant peak currents to charge or discharge the IGBT input capacitances [4]. A gate driver (part number IRS21867S) is used to drive each half bridge IGBT module. A schematic of the gate drive for one leg of the three-phase converter is shown in Figure 4.2.

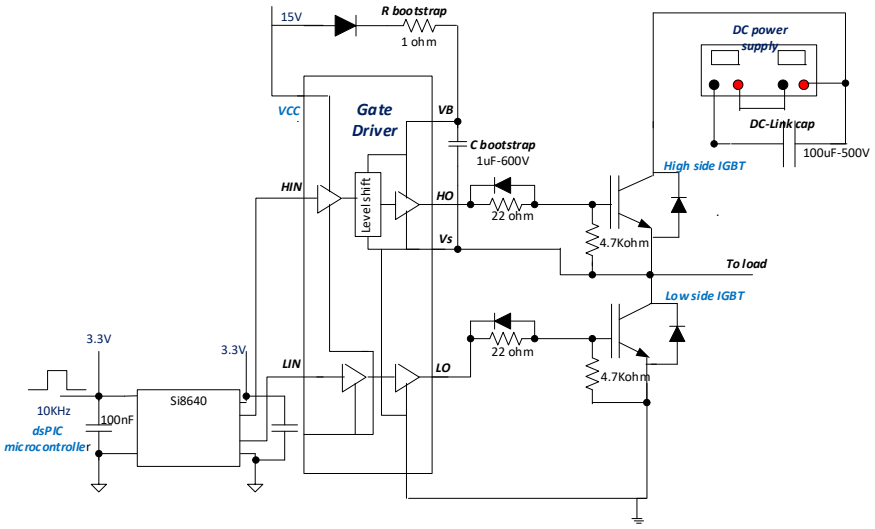


Figure 4.2: Schematic of the designed gate driver

4.2.1.2 Design of support circuitry of gate driver

A few components are added between each gate drive output and the IGBT gate terminal to control the maximum charge and discharge currents. In addition, a capacitor and resistor are required for the integrated bootstrap circuit of the gate driver circuit that generates the high side gate voltage. Design of gate resistor and bootstrap circuit is explained in sections 4.2.1.4 and 4.2.1.5.

4.2.1.3 Gate resistor design

A gate resistor (R_G) with a parallel Schottky diode is placed in series with the IGBT gate terminal. This resistor controls the current spikes during the IGBT gate charge and discharge events. In addition, R_G helps to damp oscillations caused by the inductance of the PCB track from the gate driver to the gate terminal interacting with the gate capacitance. R_G is designed based on specification limitations of the gate driver output current. Assuming an ideal voltage from the gate driver, V_O, the gate resistor must satisfy the following inequality:

$$R_G \geq \frac{V_O}{I_G} \tag{4.1}$$

where i_G is the maximum allowed gate driver output current. From the datasheet, V_O is 15 V and I_{out} is 4 A, leading to a minimum external gate resistance of 3.75 Ω:

$$R_G \geq \frac{15}{4} = 3.75\ \Omega \tag{4.2}$$

If the gate resistor is too high, the result is a reduced gate drive current and an increase in the time taken to charge the gate to emitter capacitance and an increased switching time. If the gate resistance is too low, the gate current may ring. Thus, a trade-off between these two effects needs to be made [4]. Here, 7 times the minimum gate resistor has been found to be a suitable value. As shown in Figure 4.1, there are internal gate resistors inside the module, which are series-connected to the external resistor. Figure 4.3 shows the charge and discharge paths used to find the total gate resistance during charge (blue colour) and discharge (red colour) of the gate.

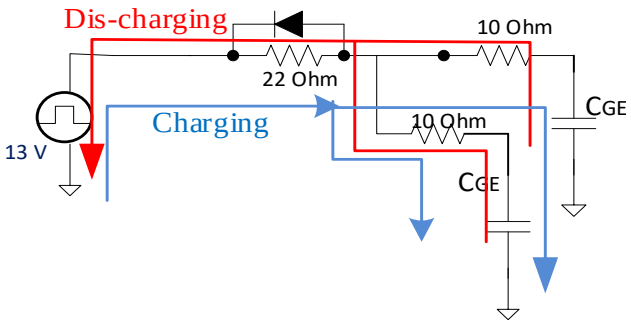


Figure 4.3: Equivalent circuit of total resistors through the gate terminal

The additional resistors lead to a total gate resistance of 27 Ω for charging and 5.7 Ω for discharging. The gate current is calculated through (4.3) and (4.4) for gate charging and discharging , respectively. A Schottky diode (part number PMEG2020AEA) is placed in parallel with gate resistor. The diode provides a path for discharging the gate capacitance of the IGBT. There is no problem with ringing during turn off, hence there is no need for a series resistor [5]. The gate-emitter voltage at the IGBT was about 13 rather than 15 V, which is important in the calibration section of the next chapter.

$$I_G = \frac{13}{22+5+1} = 0.46\ \text{A} \tag{4.3}$$

$$I_G = \frac{13}{5+0.2} = 2.5\ \text{A} \tag{4.4}$$

An additional 4.7 kΩ resistor is placed between the gate and emitter terminals to prevent the gate voltage V_{GE} from charging up randomly and switching on the IGBT if the gate driver is not powered but the DC-link voltage is present.

4.2.1.4 Bootstrap circuit design

The bootstrap gate-drive technique is used for the high-side N-channel IGBT. The emitter terminal voltage of the top device switches from 0 to V_{dc} during inverter operation. The bootstrap circuit consists of a capacitor (C_{BS}), a diode (D_{BS}), and an optional surge limiting resistor (R_{BS}), as shown in Fig. 4.4. The operation of this circuit can be divided into two phases: when the capacitor is charging and when it is discharging. The charging part is when the high-side IGBT is turned off and the low-side IGBT is turned on. The current path is shown in red in Figure 4.4. V_s charges C_{BS} through R_{BS} and D_{BS}. The capacitor is charged at VCC in order to supply the higher chip. For the discharging sequence, the capacitor acts as an auxiliary power supply to keep the gate terminal voltage at a constant value above the emitter terminal voltage. This happens when the low-side switch is turned off and the high-side switch is turned on. The capacitor acts as a power source to drive the high-side IGBT via the discharge current path, highlighted in blue. This is provided by V_{BS} when V_s is pulled to a higher voltage by high-side switch. The voltage V_B floats and the bootstrap diode is reversed biased and blocks any current to the power supply.

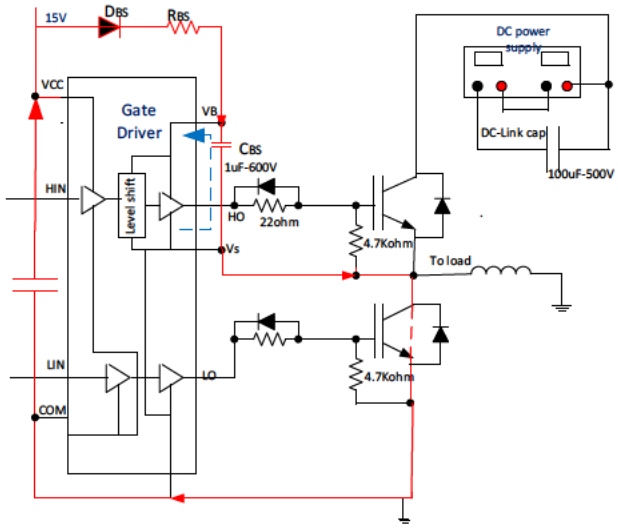


Figure 4.4: Charge and discharge of bootstrap capacitor (C_{BS})

The bootstrap method is simple and low cost to implement – it is built into the gate driver. However, this method is limited by the charge stored by the bootstrap capacitor. One of the challenges is when negative voltage appears at the switching device during turn off causing load current to flow in the low-side freewheeling diode. Much research has been carried out to optimize the bootstrap circuit and the charging of the bootstrap capacitors [6, 7]. A bootstrap capacitor should satisfy the inequality in (4.5). C_{BS} should be much larger than IGBT gate-emitter capacitance because the capacitor provides current to charge up the gate capacitance and its voltage must not drop too much during this time. The selected

IGBT has a gate emitter capacitor of about 7000 pF for 44 nC gate emitter charge over 15 V, according to IGBT datasheet. C_{BS} should be much higher than this value to confirm that the IGBT can be fully charged. C_{BS} is selected about 150 times higher than this value, i.e. 1 μF.

$$C_{BS} \geq \frac{Q_{(tot)}}{V_{l-l}} \tag{4.5}$$

where Q is total charge, 331 nC. V_{l-l} is gate driver voltage output, 15 V.

The main function of the bootstrap diode is to block the DC-link voltage from driving the gate driver power supply when the high-side IGBT is turned on. The diode must have fast recovery time and low forward voltage drop to maximise the charging voltage for C_{BS} [5]. The current rating of diode must be high enough to allow for the maximum current appearing as C_{BS} charges up. A fast recovery diode, DA2JF8100L, has been used as the bootstrap diode. It is worth noting that a bootstrap circuit requires that the high and low side devices are alternately switched on long enough to charge and discharge the bootstrap capacitor. This is achieved for typical PWM inverter applications as long as the modulation is kept between about 5% and 95%, but not usable for applications where the high side device should be turned on and held on for a long time [8]..

4.2.2 Power section

The power part of the converter consists of DC-link capacitors, heatsinks, IGBTs, gate drivers as well as the measurement sensors. This part is divided into three sub-sections. These sub-sections include the DC-link, heatsink and IGBTs.

4.2.2.1 DC-link

In this thesis the grid-side converter of the WT is not of interest so the DC-link voltage is provided by a DC power supply (CPX 400D, 120 V, 20 A). This power supply cannot sink current, so if the load is operated as a generator a load is needed in parallel with the DC link to sink the generated current. The DC-link voltage can be varied from 0 V to 120 V. Rapid changes in the DC-link current demand (for example during switching transients) are supported by a capacitor closer to the switching devices to compensate the inductance of the connection leads in the power supply. In the designed circuit, the local capacitor was chosen as 100 µF film capacitor 500 V (part number MKP1848C F1 505).

4.2.2.2 Heatsink

An aluminium heatsink with 6 fins and using natural (convection) air flow has been used dissipate heat from the module, as shown in Figure 4.5. (b). The thermal resistance of heatsink is about 3.23 °C/W [9]. The heatsink has been adapted so it can be heated up from within to simulate different levels of power dissipation by means of three parallel high-power resistors inserted into the body of the heatsink.

This helps to control the temperature of heatsink as well as the case of the IGBT by controlling the current through the inserted resistors. The heatsink temperature is measured by a T-type thermocouple. The setup is shown in Figure 4.5(a).

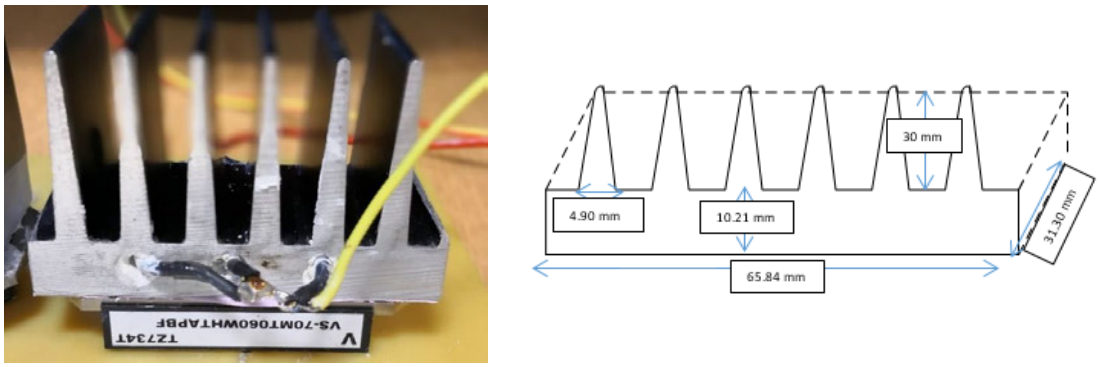


Figure 4.5: Heatsink: (a) Controllable temperature; (b) dimensions

4.2.3 Power circuit implementation

Each of the three legs of the converter has one half bridge IGBT module, as shown in Figure 4.6. The IGBT lids have been removed to allow access to the internal bond wires. Separate ground plane areas are used to separate controller signals from the power section (IGBT and gate driver output) of the power board. Digital isolators (Si8640) are used to isolate the power part of the circuit from the controller signals and controller board.

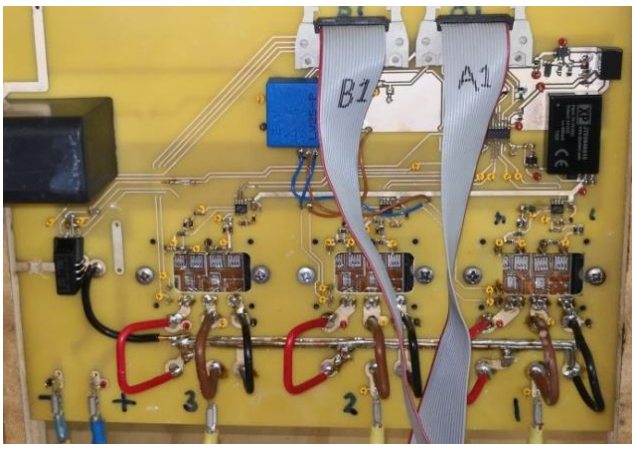


Figure 4.6: Custom-made three-phase converter power board, front side

Figure 4.7 shows the controller section of the power board, where control signals from the controller board are transferred to the power board. The controller section is galvanically isolated from the power section. The power and controller boards require 24 V, 15 V and 3.3 V (DC). The 24 V is provided by a DC power supply, 15 V is provided by a DC/DC converter and 3.3V is provided by a DC regulator.The

inputs of the isolators are PWM signals generated by a microcontroller on the controller board. The outputs of the isolators are the PWM signals to the gate drivers in the power part of the power board.

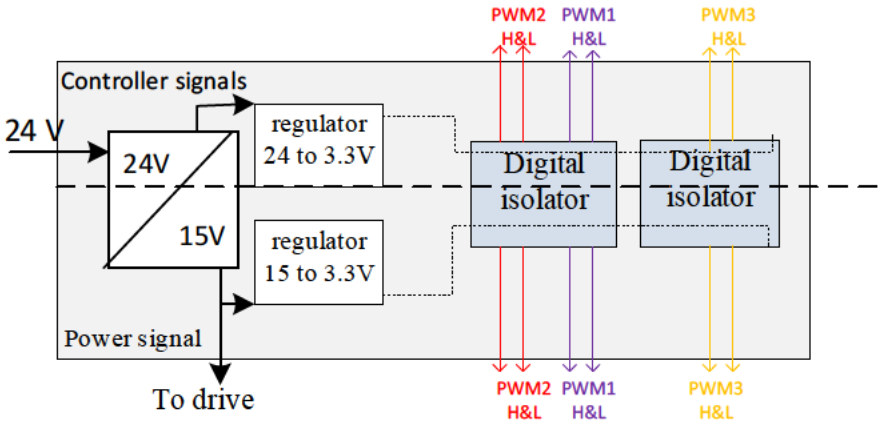


Figure 4.7: Controller signals of power board for the three-phase converter

Figure 4.8 shows power section of the power board. Three PWM signals are sent to the gate drivers from the output of isolators to the power part, which is separately grounded. The signals are then sent to the IGBT gate terminals.

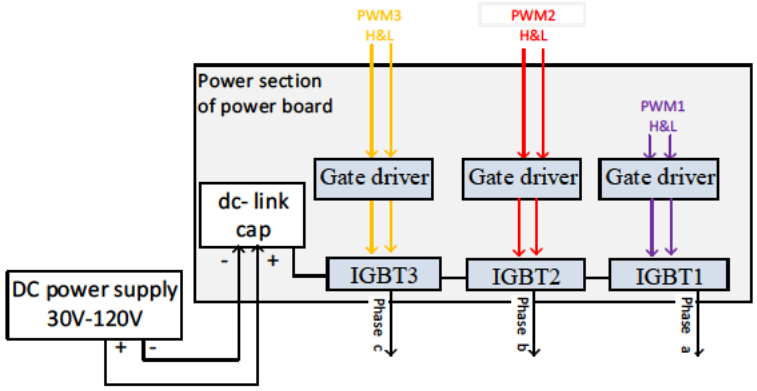


Figure 4.8: Block diagram of power section of the power board

Three IGBTs and heatsinks are attached to the rear of the power board. The design of the rear of the converter is shown in Figure 4.9a. Additional copper wires are soldered to the PCB tracks to carry the required currents as shown in Figure 4.9b. The incoming DC-link power supply contains a LEM current sensor used to detect over-current so that in the event of a fault the microcontroller is quickly turned off.

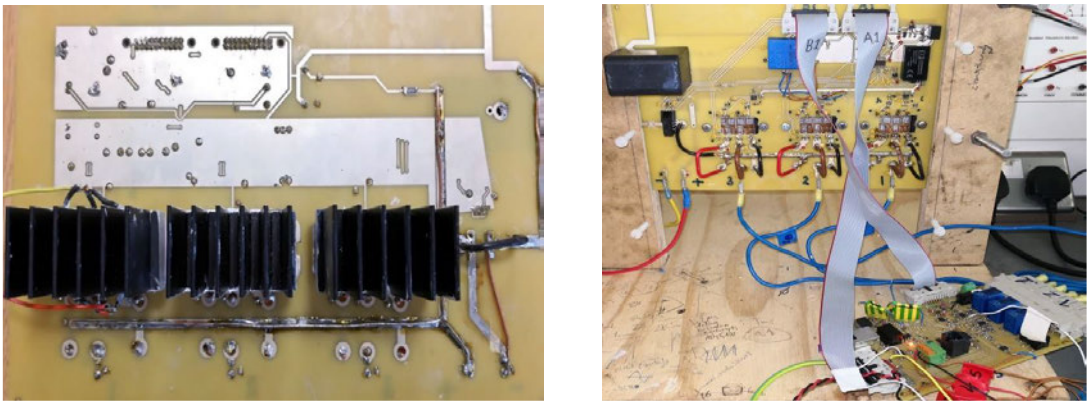


Figure 4.9: Power converter board

4.9. (a): Bottom side of a three-phase converter-4.9. (b): Embedded controller using the dsPIC microcontroller

4.2.4 Controller board

These subsections include the sensors and associated amplifiers, microcontroller, encoder and integrated serial communication (UART). A rotary encoder is used to measure the rotor speed. A UART is provided for debugging and as a serial link for the transfer of data to a laptop. The controller board is designed to generate the six PWM high and low drive signals at 3.3 V. The switching frequency of the converter is programmed at 10 kHz. The controller board hardware is shown in Figure 4.10 and consists of:

- A dsPIC32 microcontroller running at 96 MHz, section 4.2.4.1
- Three LEM current sensors for measuring the phase currents, section 4.2.4.2
- Voltage sensors to measure DC-link voltage, section 4.2.4.3
- Analogue electronics to interface the sensors to the microcontroller, sections 4.2.4.3 and 4.2.4.4
- A shaft speed tacho connection to measure the speed of the electric machine, section 4.2.4.4
- Power supply components to convert generate 3.3 V and 5.0 V power lines from 24 V
- A UART connection to monitor the converter outputs (three phase current and voltage) and controller outputs (components of current and speed controllers), section 4.2.4.5

These different parts are detailed in the following subsections.

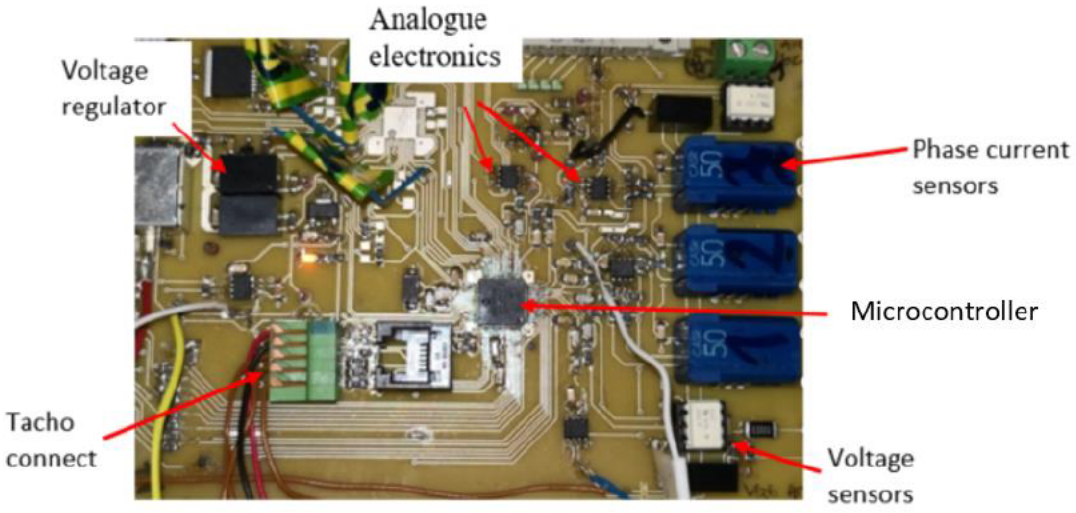


Figure 4.10: Controller board with the microcontroller

The gate drive generates two pulse signals, HO and LO, to drive the high and low side IGBTs in the module. A dead time, when both switches should be turned off, is programmable in the microcontroller PWM hardware. The dead time between two pulse signals is to avoid momentary short circuiting of the module during switching transitions. The dead time should be as short as possible, but long enough to avoid bridge shoot through, i.e. high and low side devices turned on at the same time. The dead time has been set to 0.8 µs, as shown in Figure 4.11. The yellow curve is the voltage across the gate and emitter terminals (V_{GE}) of the high-side IGBT and the blue curve is V_{GE} of the low side IGBT.

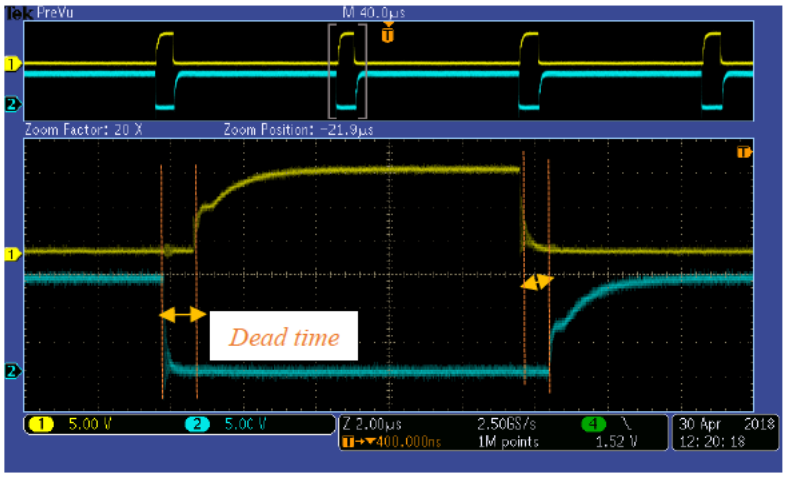


Figure 4.11: Dead time between high side and low side of half bridge

4.2.4.1 Microcontroller

The board is fitted with a dsPIC33EP512MC806 and a digital signal controller (DSC) manufactured by Microchip. The microcontroller has 8 PWM outputs, 4 integrated operational amplifiers (Op-amps), and 12 analogue inputs. A crystal with part number of ABM7-8.000MHz-D2Y-T is used in the microcontroller oscillation circuit, running at 8 MHz, internally converted to 96 MHz. Six PWM signals

are used to generate the high and low A, B and C phase voltage control signals. Five ADC channels are used for measuring the three phase currents (A, B and C), the DC-link voltage, and for reading the temperature from the NTC temperature sensor inside the module. One UART channel is used for communicating with a laptop and the built-in quadrature encoder measure the rotation of the electric machine shaft. The microcontroller firmware contains initialisation code and the current and speed controller loops, explained in section 4.2.5.1.

4.2.4.2 LEM phase current sensors

The phase currents are measured with LEM current transducers (CASR 06-NP). The electrical schematic of the current measurement circuit is shown in Figure 4.12. Non-inverting amplifiers (Microchip MCP6002) are used to convert the current sensor outputs into voltage levels suitable for driving the microcontroller ADC converters. The outputs of the current sensors are used for the current controller loop.

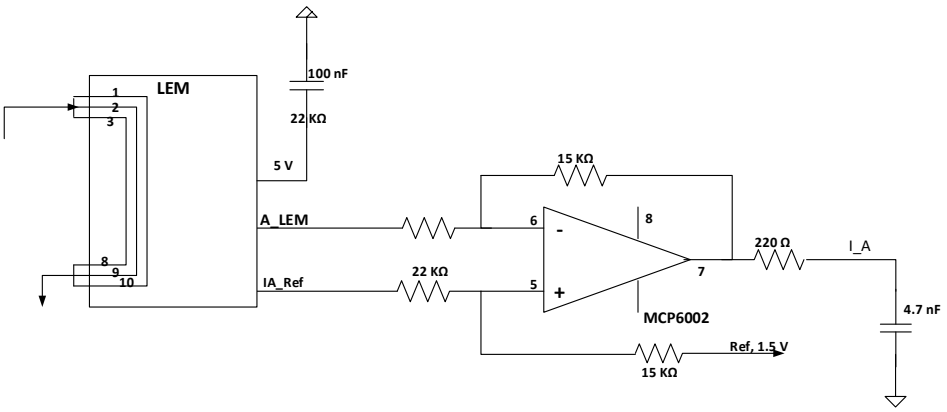


Figure 4.12: Phase current transducer

4.2.4.3 Voltage sensors

An isolated linear analogue sensing IC (HCPL-7510), powered by an isolated DC to DC converter (IK0505S), is used to measure the DC-link voltage. A differential amplifier (Analog AD8276) is used to convert the voltage to a level suitable for the microcontroller ADC input. Figure 4.13 shows an electrical diagram of DC-link voltage measurement.

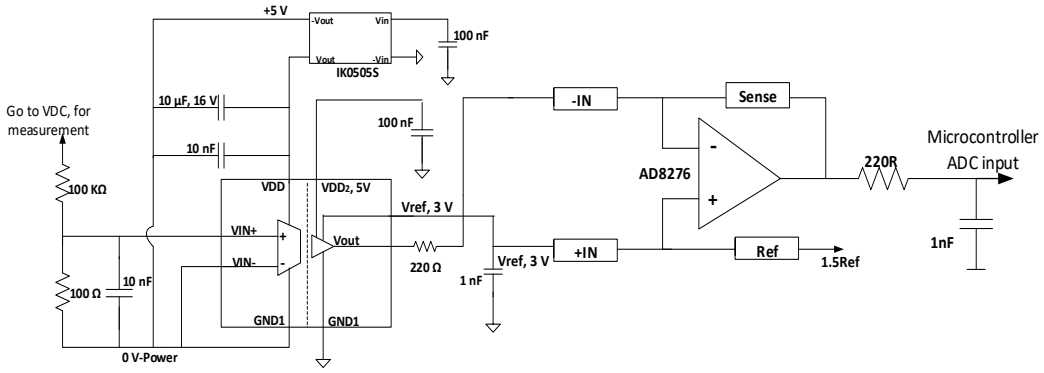


Figure 4.13: DC-link voltage measurement circuit

4.2.4.4 Rotary encoder

A rotary encoder is connected to the machine shaft to measure the rotor position and the shaft rotation rate. The chosen encoder is a quadrature encoder (Kubler 8.3720.5621) with index pulse. The encoder output signals are connected to input pins of the microcontroller quadrature encoder interface through opto-couplers because the shaft of the machine was electrically connected to the common point of the three phase coils. Opto-couplers (TLP521-4) are used to galvanically isolate the encoder outputs from the microcontroller inputs and also to shift the voltage levels to suit the microcontroller input voltage range. Figure 4.14 shows schematic of the encoder electrical connection to an input on the microcontroller. The A channel and the !A channel are used to drive one opto-coupler channel with the B and index pulses similarly managed.

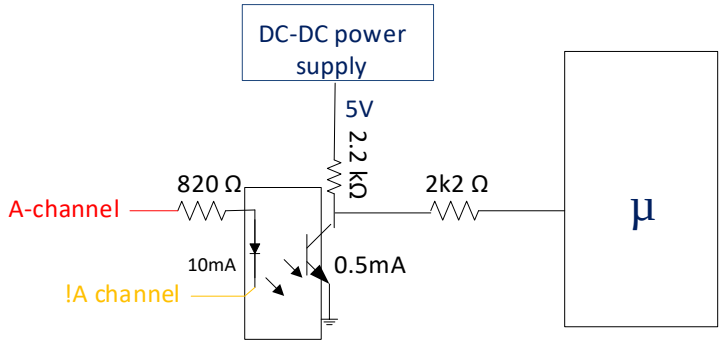


Figure 4.14: Electrical schematic of the wiring connection of encoder to the microcontroller

The maximum mechanical speed of the encoder is 6000 rpm and hence sufficient for the experiments. The output circuit of each channel of the encoder is a push-pull signal. There are 500 pulses per revolution, per channel, converted to 2000 counts per revolution, Figure 4.16. Three different channels, A, B and index signal and also inverted channels !A, !B and !index are used to provide the pulses. The '!' ("not") channels are used to reduce noise and improve the accuracy of measurements. Figure 4.15 shows the decreasing position counting down from 1999 to 0 for each revolution of the shaft.

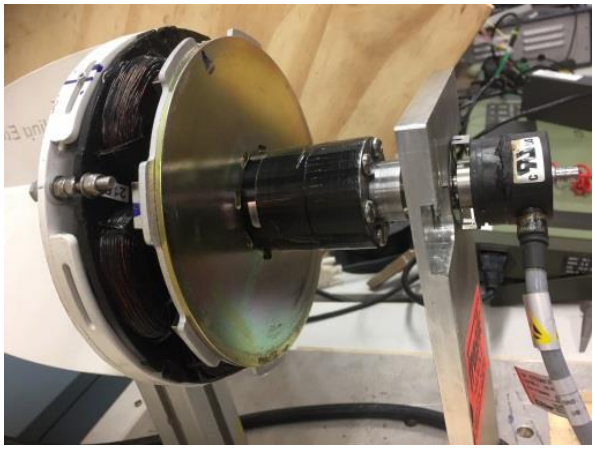


Figure 4.15: Encoder coupled to rotor shaft of the permanent magnet generator

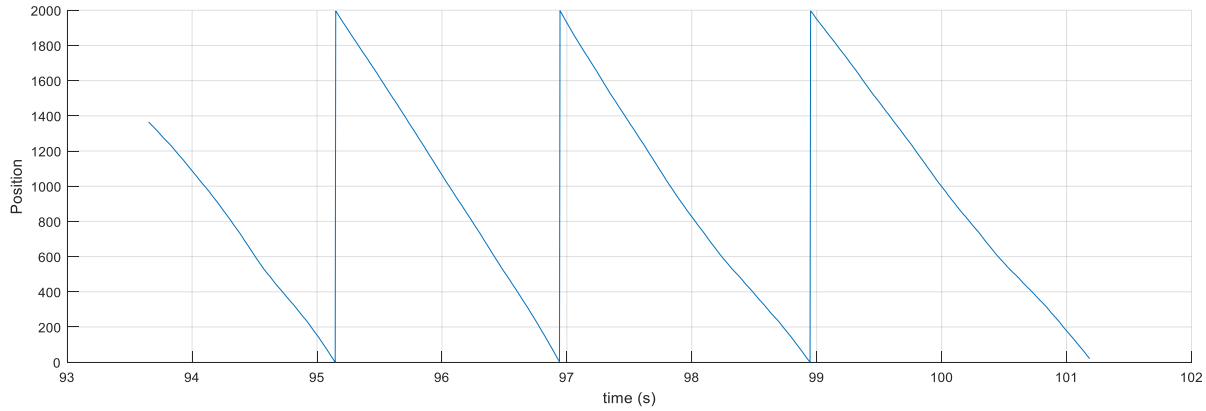
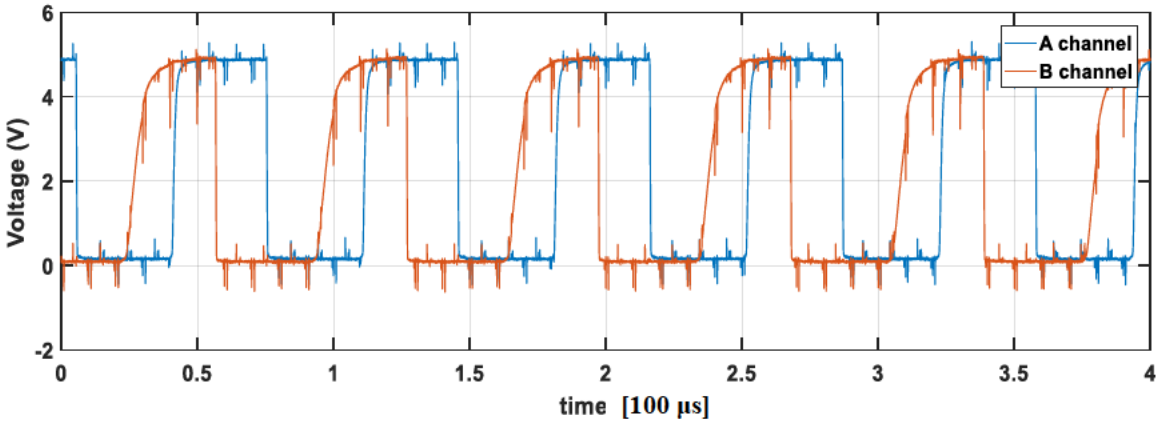


Figure 4.16: Position (angle count 0-1999 for each rotation) vs time

Examples of the output signals *A* and *B* entering the microcontroller are shown in Figure 4.17. The rise time of the output channel is about 10 μs. Some interference is visible at the IGBT switching instants. In this example, each channel sends a pulse with a 15 kHz frequency, corresponding to 1800 rpm (4.6). The index pulse occurs at a particular angle, the constant offset of which from the reference zero angle is removed in the software. Zero reference angle is defined as when the angle between one N-S pole of rotor is aligned 90º to the stator magnetic axis.

$$\text{Pulse per second} = 500 \text{ ppr} * 1800 \text{ rpm} / 60 \text{ s} = 15 \text{ kHz} \quad (4.6)$$

Figure 4.17: Output of the encoder after opto-isolators



4.2.4.5 Serial link

One universal asynchronous receiver-transmitter (UART) in the microcontroller is connected to a laptop via an opto-isolated FTDI USB link. Two digital logic isolation opto-couplers (TLP2630) electrically isolate the microcontroller output signals to protect the laptop from high voltages in the case of a fault connecting the high voltage of the DC-link to the laptop USB port. The implementation circuit of the UART and electrical connections are shown in Figure 4.18. Figure 4.19 shows the physical implementation set up board of the UART. The FTDI cable is a USB TTL serial link, which provides connectivity between USB and serial UART interfaces.

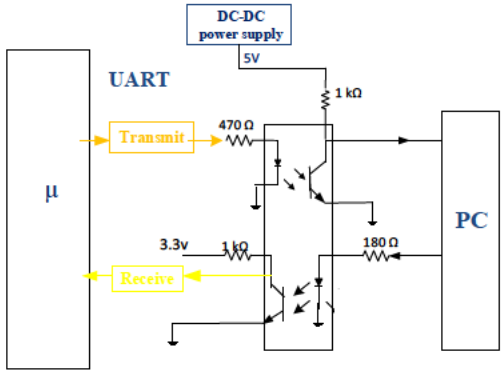


Figure 4.18: Electrical circuit of UART and relevant electrical connections

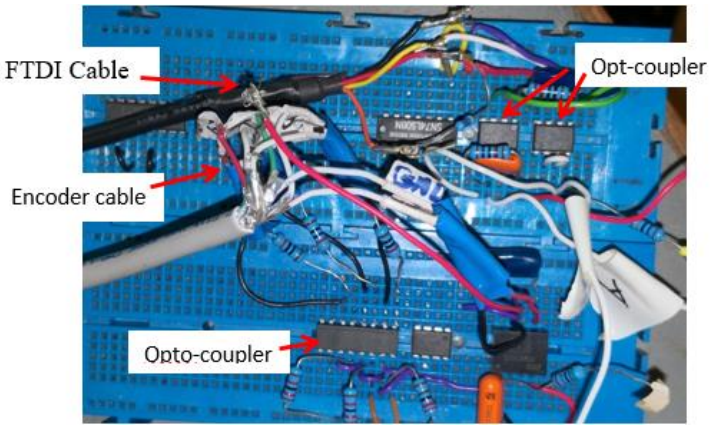


Figure 4.19: UART and encoder circuit set up

The serial link is used to transmit configuration data from a C# program running on a laptop computer while data such as voltages and currents are received for display on the laptop screen and also logged for further analysis. A sample screenshot is shown in Figure 4.20. The UART baud rate is set to 115200 bps.

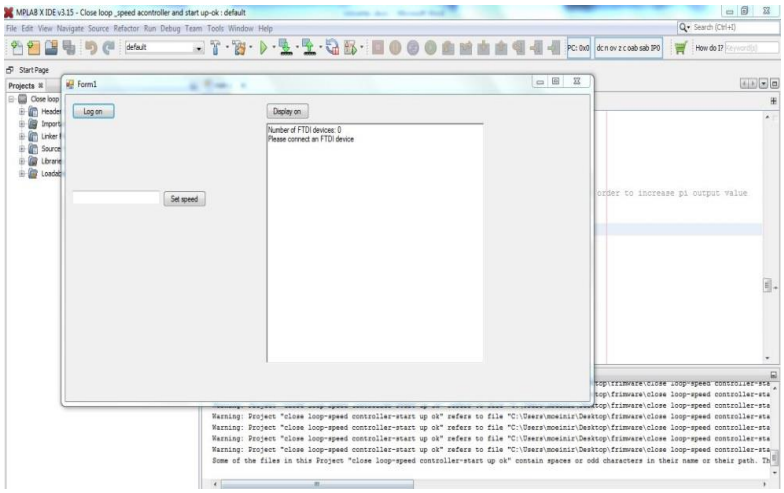


Figure 4.20: Integrated display of UART output

4.2.4.6 Firmware

Current and speed control algorithms are implemented within the microcontroller firmware, although it is also possible to run the converter in open loop if required. Figure 4.21 shows the controller algorithm implemented in the microcontroller. The current controller is the inner controller, which is based on the field-oriented control (FOC) method [9]. The speed controller is the outer loop.

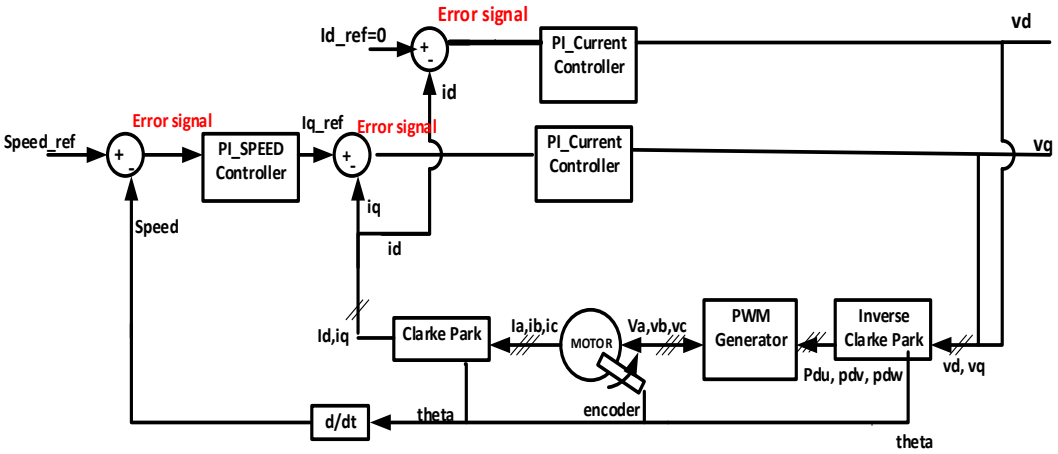


Figure 4.21: Controller block used in the generator side converter

The phase load currents are measured as feedback signals for the current controller. Although all three phase currents are measured, knowing two currents is enough as the third one can be obtained by rearranging equation (4.7).

$$i_a + i_b + i_c = 0 \tag{4.7}$$

A field oriented control (FOC) method is used for transferring these three phase currents to two orthogonal components to allow separate control of the machine flux and torque. A Park transform turns to a three-phase current ($\boldsymbol{i_a}$, $\boldsymbol{i_b}$, $\boldsymbol{i_c}$) into $\boldsymbol{i_d}$ and $\boldsymbol{i_q}$. These are used as a feedback for current controllers to control the torque of the machine according to (4.8, 4.9 and 4.10). A Park transformation converts 3-phase current into a non-rotating frame of reference with two phases, $\boldsymbol{i_\alpha}$ and $\boldsymbol{i_\beta}$, equation (4.8). The forward Park transformation is used to put rotating objects into the same frame of reference with two components of $\boldsymbol{i_d}$ and $\boldsymbol{i_q}$.

$$i_\alpha = i_a, i_\beta = \frac{i_a + 2i_b}{\sqrt{3}} \tag{4.8}$$

Here i_α and i_β are converted to i_d and i_q based on (4.9) and (4.10). These two components are mutually perpendicular with θ being the angle between the rotor flux axis and phase A. θ is obtained from the rotary encoder by finding the rotor angle position where phase a is in the same orientation as the rotor flux angle. The factor of four is introduced because there are four pole pairs on the rotor. Effectively, the sine and cosine components go through four periods during one whole rotation of the shaft.

$$i_d = \cos(4\theta)\, i_\alpha + \sin(4\theta)\, i_\beta \tag{4.9}$$

$$i_q = -\sin(4\theta)\, i_\alpha + \cos(4\theta)\, i_\beta \tag{4.10}$$

Current components i_d and i_q are individually controlled by comparing of the measured and desired current components. The d-axis reference current is called i_d^* and is set to zero to maximise the flux density produced by the permanent magnet machines. The reference current for the q-axis is called i_q^*, provided by the output of speed controller block. The current component i_q controls the amount of

torque generated by the permanent magnet machine. The measured currents are compared to the desired currents to generate error signals. The error signals are applied to proportional integral (PI) controllers to generate a reference voltage for the PWM. The rotor angle is measured to correctly transform the phase currents into the synchronous rotating reference frame. The sine and cosine functions are obtained using a lookup table that contains pre-computed values for $\sin(4\theta)$ and $\cos(4\theta)$ as functions of angle from 0 to 2000 (in pulse units).

The orthogonal voltage components are converted back into three phase voltage values pdu, pdv and PWM as indicated in equations (4.11, 4.12 and 4.13). These three voltages are then properly scaled and used to update the three channels of the PWM generators of the microcontroller.

$$pdu = f_\alpha \tag{4.11}$$

$$pdv = (-\frac{f_\alpha}{2}) + \frac{\sqrt{3}}{2} \times f_\beta \tag{4.12}$$

$$pdw = (-\frac{f_\alpha}{2}) - \frac{\sqrt{3}}{2} \times f_\beta \tag{4.13}$$

The outer controller in Figure 4.23 operates as follows: The rotation speed is estimated as proportional to the encoder count change over a 4 ms moving window. The desired (reference) speed can be set manually over the UART. This speed is compared to the desired speed and the error feeds a PI controller. The output of this PI controller forms the reference input signal for another PI controller that is used for the i_q-axis current controller. The output signal from the speed controller is called $i_{q,ref}$.

4.3 Load test set up

As shown in Figure 4.22, the converter is initially connected to a three-phase permanent magnet machine, a 105 W micro WT (model LE-450 manufactured by Leading Edge Power). The datasheet appears in Appendix B. Table 4.2 shows the electric machine specification used in this WT.

Table 4.2: Specifications of the electric machine used in the wind turbine

Machine type	Power output	Current capacity	Number of pair coils	Number of pair rotor poles
permanent magnet machine	450 W	10 A per phase	3	4

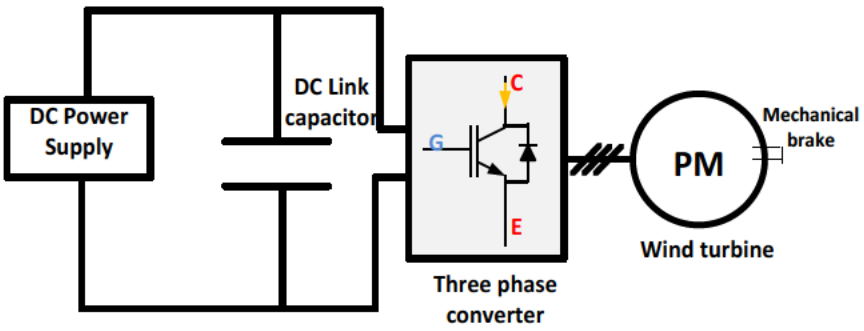


Figure 4.22: The test set up

Due to lack of availability of a suitable wind tunnel facility, the WT was run as a motor instead of as a generator most of the time. Fortunately, the control loops and converter operation are essentially the same as a generator-side converter in WTs. The shaft was also rotated using a drill to test that it could also generate current back to the DC-link (with a suitable load). The equivalent cut-in, rated and cut-out speeds have been measured at 750, 1500 and 3600 rpm, respectively. The WT was also tested in a small wind tunnel to validate the manufacturer data up to 10 m/s. The three-phase output of the wind-turbine machine was connected to a three-phase diode rectifier and the DC output voltage was found variable from 30 V to 120 V. The speed was controlled by setting a desired speed using the serial link. A mechanical brake was added to allow an adjustable braking torque to be applied to the rotor, shown in Figure 4.23. The maximum current flowing in each of the permanent magnet machine coils was 10 A per phase, limited by the current rating of the stator windings.

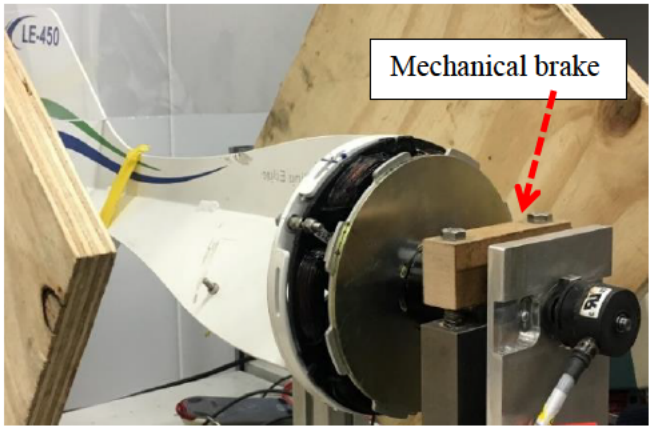


Figure 4.23: The mechanical braking system

4.4 Estimation of the parameters of the permanent magnet machine

The machine electrical parameters have been assessed using a locked rotor test. The inductance was found to be largely independent of the rotor angle. In the locked rotor test, an AC three-phase voltage is applied to the permanent magnet machine stator windings at zero speed until the rated current is

reached. Quantities measured during this test are the stator phase current and the power factor. The current magnitude of the stator and rotor impedances, $|Z|$, is calculated according equation (4.14). As when the rotor is locked the back e.m.f becomes zero, (4.15) becomes (4.16).

$$\text{AC voltage} - \text{back e.m.f} = \text{I} \times \text{Z} = \text{I} \times (\text{R} + \text{X}_\text{L}) \quad (4.14)$$

$$\text{AC voltage} = \text{I} \times \text{Z} = \text{I}e^{-\varphi} \times Z \quad (4.15)$$

$$5 = 0.5\text{e}^{-\text{j}0.5}(\text{R} + \text{j}\omega\text{L}) \quad (4.16)$$

where φ is the measured phase angle of the current. The stator resistance of each phase is estimated as 8.8 Ω for two series coils (the centre point of the Y-connected winding was not available) and hence 4.4 Ω for each phase, as indicated by equation (4.17). The stator inductance is estimated as 15 mH for two series coils, thus 7.6 mH one phase, as indicated by equation (4.18).

$$\text{R} = 10\cos(0.5) = 8.8\ \Omega \text{ for two series coils} \quad (4.17)$$

$$\text{L} = 10\cos(0.5) = 15\ \text{mH for two series coils} \quad (4.18)$$

4.5 Validation of the current controller

Figure 4.24 shows the three-phase current generated by the converter using a static resistive-inductive load using a sampling rate of 30 Hz. As there is no rotating machine, the shaft angle was generated in the firmware. Figure 4.25 shows the output of the current controller for the d- and q-axes. The $i_{d,ref}$ is set zero. i_d is also zero following $i_{d,ref}$. To validate the current controller in the q-axis, $i_{q,ref}$ was set to 2 A. As shown in the figure, i_q follows $i_{q,ref}$. The results were obtained over the UART so are slightly irregular. There is some noise in the measured currents that gets into the i_d and i_q values (

Figure 4.25

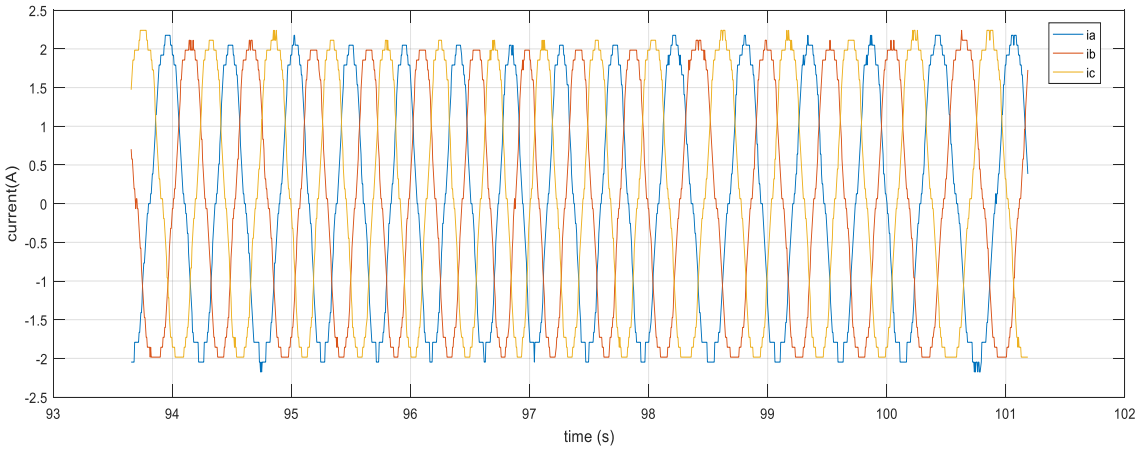


Figure 4.24: Three-phase outputs feeding a static load

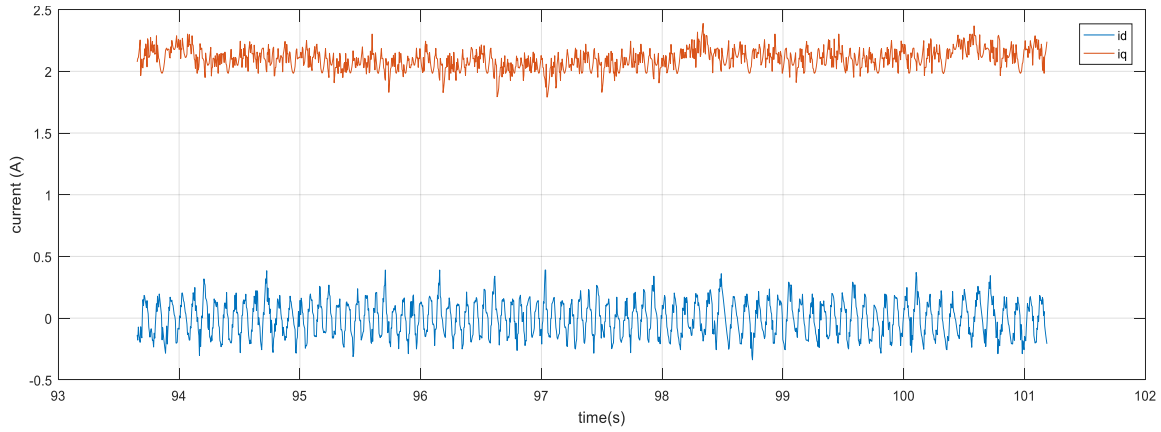


Figure 4.25: Validation of the current controllers

To find the step response time, i_q^* is changed by discrete steps. The reference current, i_q^* is changed from 1 A to 2 A. The proportional gain k_p is 16000 and the integral gain k_i is 400. The rise time of $i_q$measured from 10% to 90% is about 12 µs as shown in Figure 4.26.

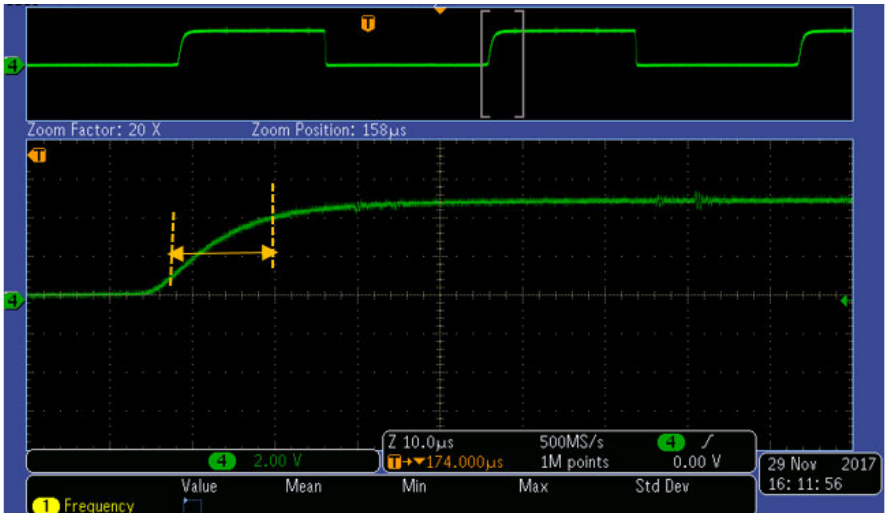


Figure 4.26: The rise time of the current controller

4.6 Validation of the speed controller

The relationship between scaled speed, speed reference to real speed in rpm is obtained by (4.19). Quantity 'speed_ref' is the number of pulses in 4 ms.

$$speed(rpm) = 60 \times \frac{speed\_ref}{2000 \times 4 \times 10^{-3}} \qquad (4.19)$$

To validate the speed controller, speed_ref was initially set to 10 rpm, then increased to 70 rpm for 10 s, and then to 190 rpm for 25 s. Figure 4.27shows that the speed follows speed_ref. Small oscillations when speed changes at 10 and 15 seconds are caused by the PI controller of the speed control loop in combination with quantisation error in the speed computation and current measurements. There should

be no steady-state error when using a PI controller, however when the steady-state error falls below the smallest representable magnitude within the microcontroller, the steady-state error becomes rounded to zero so as far as the controller is concerned there is no error. This was traced to an issue with the representation of numbers inside the firmware and could be improved. The speed signal could be obtained with higher resolution by counting number of pulses over a longer time, however this announces extra delay into the control loop that can lead to controller instability. The speed error is of no consequence in the lab-based experiments, so the speed error was left alone.

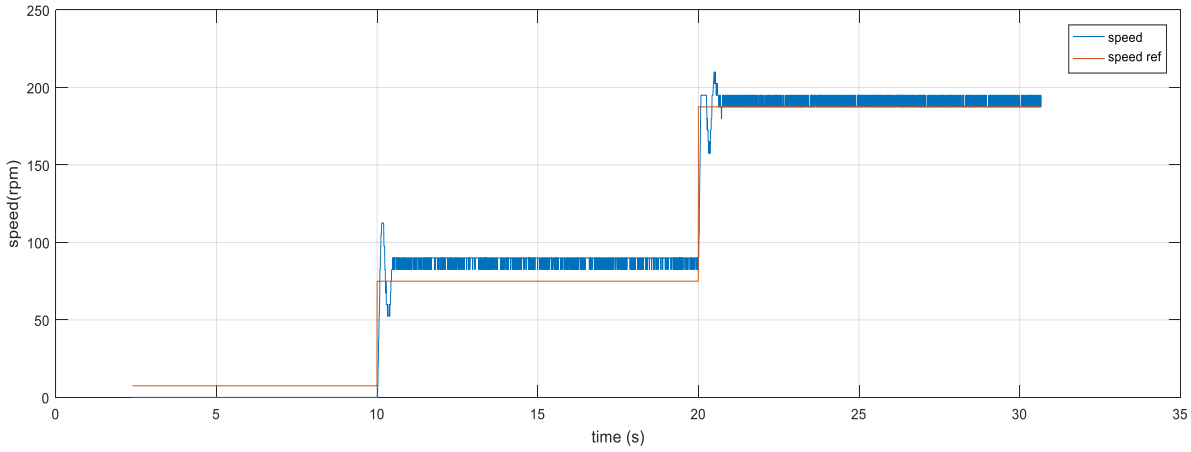


Figure 4.27: Validation of the speed controller

4.7 Summary

A three-phase converter has been designed in the lab. The selected IGBTs have accessible dies to allow simulation of bond-wire lift-off by manually cutting (some of the) bond wires. The inverter is connected to the electrical generator of a small WT to simulate the effect of wind variation and, specifically, variation of the speed shaft and torque. The test setup has been equipped with sensors to measure the three-phase current, the DC-link voltage, the rotating speed and the switching on and switching off times of the IGBTs. The heatsinks of the IGBTs can additionally be externally heated to simulate different thermal environments and externally influence the junction temperature of the devices. This test setup is used in the next chapter to evaluate the effectiveness of two thermally electrical sensitive parameters to estimate the junction temperature and predict the failure of IGBTs.

4.8 References

[1] R.S. Chokhawala, J. Catt ; B.R. Pelly, “Gate drive considerations for IGBT modules”, IEEE, PP. 603 – 611, 1995. Available in 2017 at https://www.vishay.com/docs/94468/vs-50mt060whtapbf.pdf

[2] Available in 2018 at http://www.ti.com/lit/an/slua887/slua887.pdf

[3] Available in 2017 at http://www.ti.com/lit/ug/tidudj9/tidudj9.pdf

[4] Available in 2018 at https://www.infineon.com/dgdl/Infineon-EiceDRIVER-Gate_resistor_for_power_devices-AN-v01_00-EN.pdf?fileId=5546d462518ffd8501523ee694b74f18

[5] Available in 2015 at https://www.infineon.com/dgdl/Infineon-Bootstrap_Network_Analysis-AN-v01_00-EN.pdf?fileId=5546d462533600a40153559692661096

[6] Available in 2018 at https://www.mitsubishielectric-mesh.com/download/app/power/DIPIPM%20Bootstrap%20Circuit%20Design%20Manual.pdf

[7] Available in 2020 at https://www.myheatsinks.com/calculate/thermal-resistance-plate-fin/

[8] L. Harnefors and H-P. Nee "Model-Based Current Control of AC Machines Using the Internal Model Control Method", IEEE Transactions on industry applications, Vol. 34, (1), 1998.

[9] R. Moeini, M. Rafiee and Ebrahim Afjei, "Low Cost Torque Ripple Reduction in SRM Utilizing Resonance Phenomenon in Order to Optimize the Current and Torque Profile", EPE journal, pp 37-47, 23 May 2017.

Chapter 5: Experimental results: Bond wire lift-off

5.1 Introduction

Note that significant parts of this chapter appear in the proceedings of the 2nd International Winercost and Aeolus4Future conference and 6th International conference on clean electrical power (Moeini, Pietro, Hemida and Baniotopoulos, 2016), with appropriate referencing.

The majority of electrical failures in WTs occur in the semiconductor components (IGBTs) of converters. To increase reliability and decrease the maintenance costs associated with IGBTs, several health monitoring methods have been proposed in the literature. Many laboratory-based tests have been conducted to detect failure mechanisms of IGBTs in their early stages through monitoring variations of the thermo-sensitive electrical parameters. The methods are generally researched and validated with a single-phase converter with an air-cored inductive and/or resistive load. However, limited work has been carried out considering limitations associated with measurement and processing these parameters for three-phase converters. Furthermore, looking at just variations of the junction temperature of the IGBT module will most likely lead to unreliable health condition monitoring as different failure mechanisms have their own effects, sometimes opposing effects, on temperature variations of some, or all, of the electrical parameters. A reliable health condition monitoring system is necessary to determine whether the temperature variations are due to the presence of a premature failure or from normal converter operation. To address this issue, the temperature measurement approach should be independent of the failure mechanisms.

In this chapter, temperature is estimated by monitoring an electrical parameter particularly affected by different failure types. Early BWLO is detected by another electrical parameter that is sensitive to the progress of the failure. Consideration two separate electrical parameters, one for estimation of temperature (switching off time) and another to detect the premature BWLO (collector emitter on–state voltage) could increase the accuracy of the temperature estimation as well as premature failure detection.

5.2 Estimation of junction temperature and failure detectors

Many laboratory-based tests have been carried out to examine the failure mechanisms of IGBTs in their early stages for a single-phase converter with an air-cored inductive, or inductive and resistive, load. However, limited work has been carried out in real applications, and essentially none with specific application to WT converters. One challenging issue for the diagnosis of premature failures is the practical implementation of a failure detection method that works when the converter is operating. Another challenge is the effect of wind speed variations on failure detectors that has been overlooked in the literature. In the case of WTs, looking at just the variations of electrical parameters may lead to the inaccurate failure detection. In this section, an overview of proposed failure detection techniques is given. Two thermo-sensitive electrical parameters (TSEPs) are proposed to detect BWLO and SF, namely $V_{CE,on}$ and switching times.

As TSEPs change with temperature, tracking temperature is necessary to correctly interpret the reasons for any changes away from those found in the healthy state. Switching times are used to monitor T_j through the calculation of power losses. Sensitivity and linearity of switching times to temperature as well as to failures are studied in this section. Problems associated with measurement techniques with a three-phase converter under inductive load will be discussed. Method used for capturing relevant electrical parameters and processing data are discussed. Experimental results associated with detection of failures have been compared with a thermo-electrical model of the IGBT. Moreover, the sensitivity of failure detectors to the load and temperature variations has been studied.

5.3 Topology of interest for $V_{CE,on}$ as a failure detector

In recent years, manufacturers have increased the current rating and heat tolerance of IGBT devices by using parallel chips and putting several wires in parallel between the silicon die attach and the emitter terminals. These wires can become detached (lift-off) during power cycling due to temperature stresses. Early failure can be defined as when a single bond wire has lifted up, however the IGBT is still able to function, albeit with a significantly increased risk of total failure. The voltage drop across the emitter bond wires increases as bond wires come adrift. This accelerates the progress of failure within the remaining bond wires as they each have to carry higher currents [1].

The mathematical relationship between i_C and bond wire (as a resistor) is represented by (5.1). The mathematical relation betweenV_{BWLO}, temperature and i_C is given in equation (5.1)

$$R_{BWlo_i} = \rho \frac{L_i}{A}, \quad R_{BWlo} = R_{BWlo_1} || R_{BWlo_2} || \dots || _{R_{BWlo_N}}, \quad V_{BWlo} = R_{BWlo} \times i_{C,on} \qquad (5.1)$$

where R_{BWLO} is the resistance in the emitter bond wire connection; ρ is the resistivity of the bond wire material; L is the length of wire; A is cross-sectional area of wire; N is number of emitter bond wires for IGBT module; and $i_{C,on}$ is current flowing through the IGBT when the IGBT is on. Equation (5.1) states that $V_{CE,on}$ is a function of the collector current as well as temperature. Bond wires are generally made from aluminium with all power connection bond wires having the same width, 15 μm for the IGBT under test. However, each R_{BWLO_i} is proportional to the length of the corresponding bond wire, and they are of differing lengths. Figure 5.1 shows an electrical schematic of an IGBT module as well as a photograph of the physical IGBT with bond wires clearly visible.

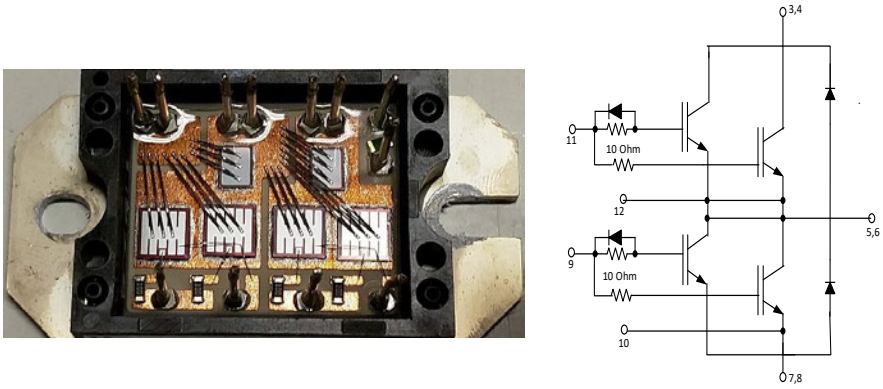


Figure 5.1: Electrical diagram and power bond wires of the IGBT

The relationship between $V_{CE,on}$ and temperature is a function of i_c. At low collector current, $V_{CE,on}$ has a negative temperature coefficient, while at high collector current it has a positive temperature coefficient. The cross-over point where the temperature coefficient changes its sign is called inflection point. $V_{CE,on}$ depends only on the temperature if i_C and V_{GE} are considered to be constant. There are two temperature dependent parameters in (5.21), which gives the collector-emitter on-state voltage in terms of other quantities [2]. Both the resistance of the channel region, R_{on}, increases rapidly with increasing temperature, whereas the forward voltage drop V_{BE} of the base emitter diode of the internal PNP transistor, has a negative thermal coefficient. Therefore, $V_{CE,on}$ of an IGBT is the combination of a voltage with a positive temperature coefficient and a voltage with a negative temperature coefficient.

$$V_{CE} = V_{BE} + R_{on} \times \frac{i_C}{I+\beta_{PNP}} \tag{5.2}$$

As the second term of (5.2) is dependent also on i_C, it can be observed that V_{BE} dominates at very low current levels and so $V_{CE,on}$ decreases with increasing temperature; at higher current levels, such as the nominal operating current, $V_{CE,on}$ largely depends on the second term of the above equation, meaning $V_{CE,on}$ rises with the temperature. Voltage $V_{CE,on}$ is a function of junction temperature, V_{CE} and V_{GE} (5.3) [3]. With increasing temperature, V_{GE} increases with a sensitivity of 800 mV/°C [4]. A temperature-adaptive gate driver can be used to give a uniform driver performance with changing

operating conditions. The gate driver can be itself affected by self-heating. The larger the value of V_{GE}, the lower the value of $V_{CE,on}$, with a sensitivity of almost 200 mV/V [5].

$$V_{CE} = f(T_j, I_C, V_{GE}) \tag{5.3}$$

In this thesis, the gate drive voltage has been checked frequently to make sure it remained more or less constant. In practice, the temperature of the gate driver may vary so it is recommended that in a commercial product a temperature and voltage amplitude regulated gate driver is used.

One of the challenges of using $V_{CE,on}$ as a failure detector is that V_{CE} is switching from a few volts when the IGBT is on to hundreds of volts (the DC-link voltage) when it is off. The DC-link voltage generally far exceeds the maximum allowable input voltage of a conventional op-amp. Additional protection and buffer circuits are required to protect the voltage measurement circuit against transient voltage spikes as well as the high voltage during the off state. This protection and buffer circuit should be capable of accurately dealing with low voltage inputs (typically < 3 V) found during the on-state mode of the IGBT without being destroyed by the high voltage input during the off time. In addition, the transition from a high voltage (causing saturation of the op-amp output) to a low voltage (where the op-amp is in its linear operating region) typically occurs with significant delay. With a PWM frequency of 10 kHz, the time for the op-amp to return to its linear operating region is limited, so care needs to be taken to obtain a sufficiently accurate measurement of $V_{CE,on}$. Using a precision differential amplifier with a very high common-mode voltage input range makes possible the measurement of $V_{CE,on}$ within an operational converter as it can tolerate the high input voltage $V_{CE,off}$. A recently introduced part that allows for this sort of application is the AD8479R-EBZ by Analog Devices.

An evaluation board featuring a precision difference amplifier (AD8479R-EBZ) has been used to allow measurement of $V_{CE,on}$, shown in Figure 5.2. The chip has unity gain, a bandwidth of 130 kHz, and a ±600 V common-mode input voltage range using ±15 V supplies. The rate of recovery from saturation is 7.5 V/µs. The positive input terminal (red wire, +IN) is connected to the collector terminal and the negative terminal (brown, IN-) is connected to the emitter terminal. The output of the amplifier ($V_{CE,on}$) is connected to a National Instruments (NI) analogue-to-digital converter. Moreover, i_C is measured instantaneously through a current probe and logged through another channel of the NI data acquisition device. Measurement is recorded by the NI instrument for the higher side of the IGBT. The higher side IGBT can now be studied because the ground is floating and its voltage changing from maximum DC-link voltage to ground. The lower side IGBT has its emitter grounded so can be measured more simply.

Voltage V_{CE} is observed to be negative across the upper IGBT when current is flowing in the anti-parallel freewheeling diode that happens every time the IGBT turns off. This event results in data with negative voltages that actually show that the anti-parallel diode is conducting. There are also occasional

spikes seen in V_{CE} that arise during the switching instants of the converter, the slow recovery rate of the measurement board (7.5 v/µs) and voltage noise. Figure 5.3 shows an example of $V_{CE,on}$ and current i_c measured at the upper side IGBT with a resistive and inductive load. Current i_c varies from 0 A to 15 A and $V_{CE,on}$ varies from 0 V to 1.3 V. When the current varies from 0 to -15 A, the diode forward voltage (V_F) is changing from 0 V to 1.1 V (negative voltages on the graph).

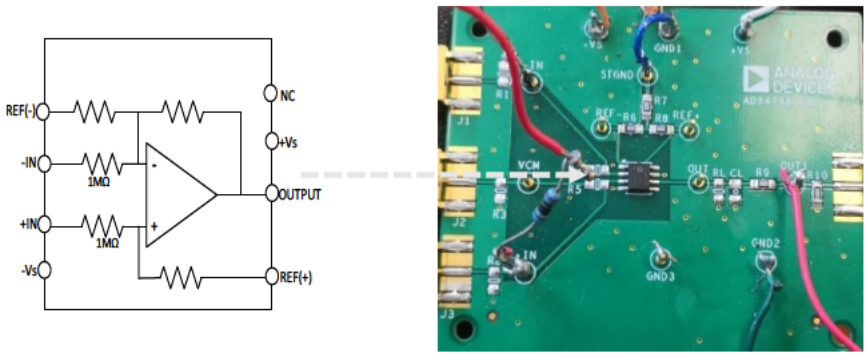


Figure 5.2: $V_{CE,on}$ measurement circuit

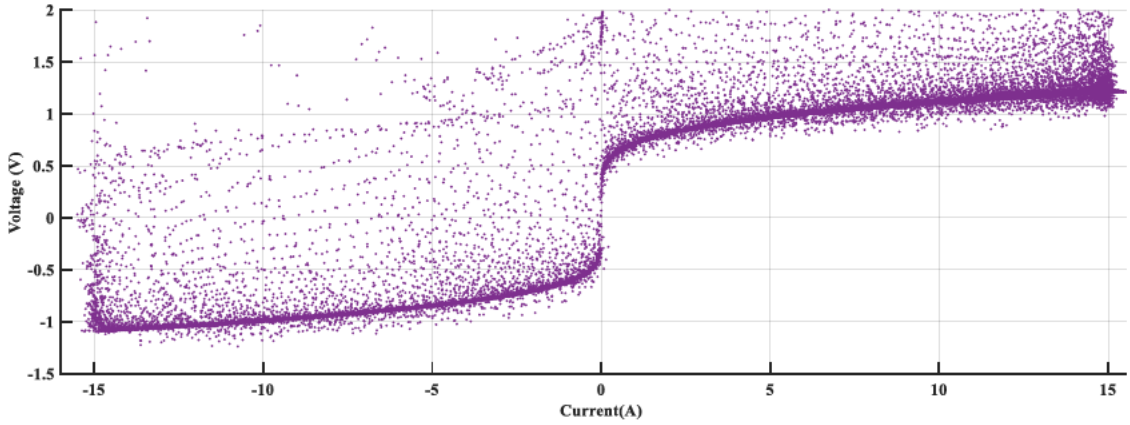


Figure 5.3: $V_{CE,on}$ versus i_C under an inductive load

The figure shows a rather nice pattern of $V_{CE,on}$ against current that represents the IGBT behaviour for positive currents and the freewheeling diode for negative currents. The other data points, as explained above, are data during switching times and during the recovery of the differential amplifier from a high input voltage.

5.3.1 Correlation between $V_{CE,on}$ and temperature

Here, $V_{CE,on}$ has been measured at various currents and temperatures (25, 80 and 150°C) using the high voltage differential amplifier board. A calibration test has been performed through the circuit shown in Figure 5.4. The lower chip is kept off by connecting its gate to its emitter, but the lower side parallel

diode can still carry current. The higher chip is switched on by applying short pulses (20 µs) to avoid self-heating.

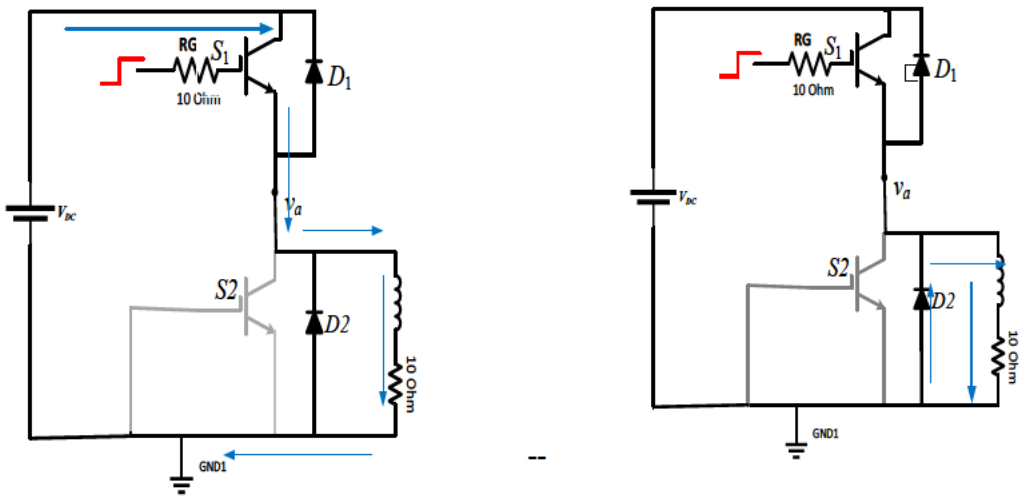


Figure 5.4: The circuit used for calibration of $V_{CE,on}$
(a) Current path, high side on; (b) Current path, high side off

The measurement circuit was used to measure $V_{CE,on}$ while the IGBT module is heated by changing the base-plate temperature. The heatsink temperature (T_H) can be controlled by applying current to power resistors embedded into a heatsink. Three power resistors (10 Ω, 10 W able to withstand a temperature up to 250°C) are connected in parallel and a controlled current is passed through the resistors, shown in Figure 5.5. T_H increases with increasing current, once steady-state has been achieved. T_H is read using a thermocouple connected to an 8 channel thermocouple data logger (Pico Logger TC-08).

Figure 5.5: Parallel resistors inserted inside the heatsink

The junction temperature can be obtained from the NTC in the chip by measuring its resistance and looking up the corresponding temperature. The calibration process between $V_{CE,on}$ and T_j is summarised in five steps:

1. Heat up the controllable heatsink using the internal heating resistors and wait for thermal steady state (about 15 to 30 minutes). The current is adjusted manually to achieve the desired chip temperature as the current required to reach a given chip temperature depends on the ambient temperature. The device is in the off state and hence no power dissipation occurs in the device. T_j can been considered the same as that of the NTC inside the substrate.
2. Force a collector current for a short time, but long enough for $V_{CE,on}$ to be measured. Current is applied for a very short duration so that the power dissipation is small. T_j can be still be considered as equal to the case temperature.
3. Steps 1 and 2 are repeated for different temperatures.
4. The relationship between T_j and $V_{CE,on}$ is achieved by regression between T_j, i_C and $V_{CE,on}$. The case temperature is assumed equal to T_j because of the negligible self-heating of the IGBT.
5. Steps 1-4 are repeated with different collector currents.

Measurement of $V_{CE,on}$ have been carried out for three different temperatures, 25, 85 and 150ºC. There is a negative correlation between $V_{CE,on}$ and T_j before the inflection point and positive after inflection point, shown in Figure 5.8.

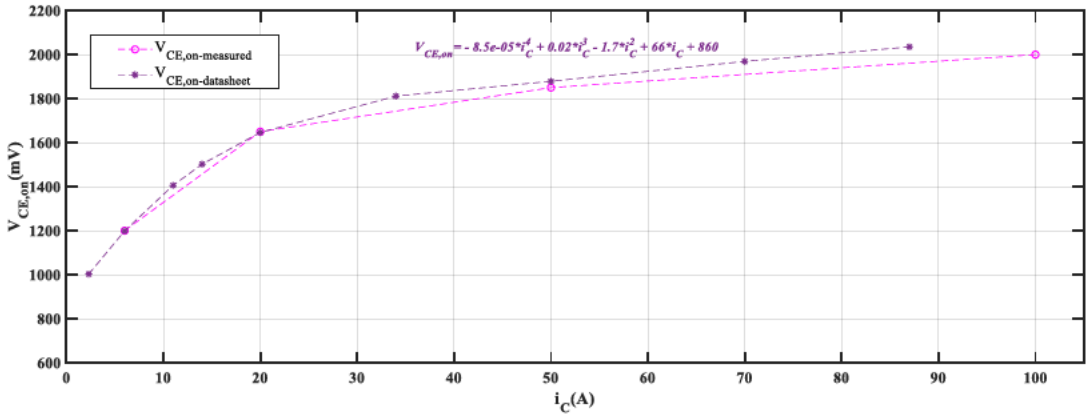


Figure 5.8: i_C versus $V_{CE,on}$ according to the IGBT datasheet at 25°C

As shown in the figure, $V_{CE,on}$ decreases with increasing temperature tothe left of the inflection point. To do fitting between $V_{CE,on}$ and i_C, 2nd- and 4th- order polynomial have been obtained, equations (5.4) and (5.5), respectively.

$$V_{CE,on_{150C}}(datasheet) = -0.072i_C^2 + 21i_c + 75 \quad (5.4)$$

$$V_{CE,on_{25C}}(datasheet) = -(8.5e^{-5} \times i_C^4) + (0.02i_C^3) - (1.7i_C^2) + (66ic) + 860 \quad (5.5)$$

Accuracy of the $V_{CE,on}$ measurement by the difference amplifier has been investigated through these two equations. As it shown in Figure 5.8, the measured $V_{CE,on}$ followed the $V_{CE,on}$ achieved by

datasheet. These two polynomial equations are combined used to find a nonlinear equation using linear interpolation with temperature (5.6).

$$V_{CE,on_X}(Cal) = V_{CE,on_{25C}}\left(1 - \frac{T_x - T_{25}}{T_{150} - T_{25}}\right) + V_{CE,on_{150C}}\left(\frac{T_x - T_{25}}{T_{150} - T_{25}}\right) \quad (5.6)$$

By using equation (5.26), $V_{CE,on}$ has been calculated for different temperatures from 10ºC to 150ºC and plotted in Figure 5.9. As shown in the figure, the sensitivity of $V_{CE,on}$ to the temperature before the inflection point (82ºC) is much higher (4 mV/ºC) than sensitivity after the inflection point (1.1 mV/ºC).

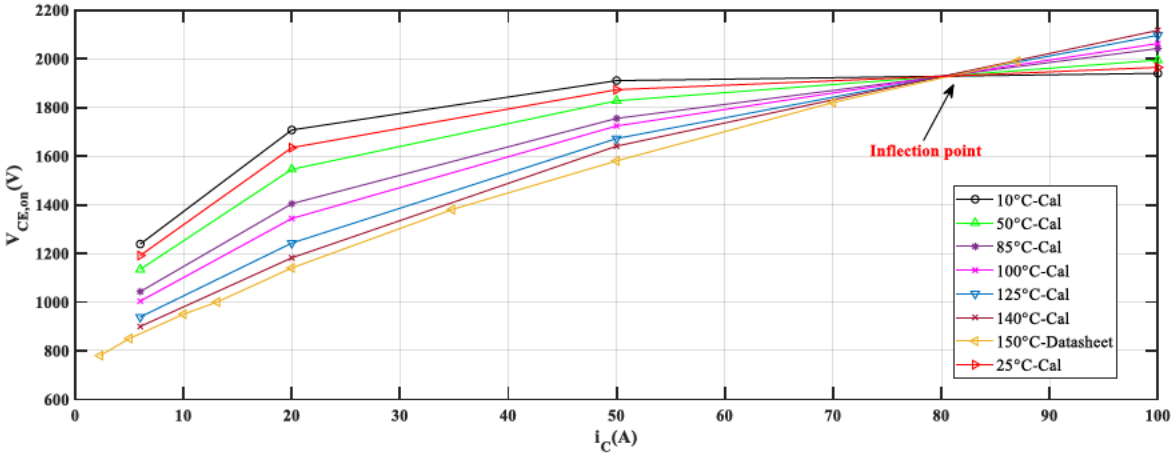


Figure 5.9: $V_{CE,on}$ vs i_c for various temperatures

The current level is chosen in order to have a linear variation of $V_{CE,on}$ to T_j. The dissipated energy is negligible so the temperature change is negligible and does not induce any observable self-heating during the 20 µs calibration time. Sensitivity of $V_{CE,on}$ to i_C is 4.85 mV/A. Sensitivity of $V_{CE,on}$ to T_j is 4 mV/ºC after the inflection point and 1.1 mV/ºC before the inflection point for a temperature range of 10 to 150ºC degree. It shows that $V_{CE,on}$ has lower sensitivity to T_j at about maximum current capability. According to the datasheet, operating i_c value is 50 A and it is 114 A at ambient temperature (25ºC) which means that $V_{CE,on}$ has sensitivity of 2.35 mV/ºC to T_j around typical operating condition.

To estimate $V_{CE,on}$, i_C and temperature should be measured simultaneously. The measurement points are shown in Figure 5.6. The voltage between the collector and emitter terminals is measured using a differential voltage probe and the current is measured using a current clamp. Relationships between

these three parameters are shown in (5.9). Through this equation, T_j can be extrapolated based on i_C and $V_{CE,on}$.

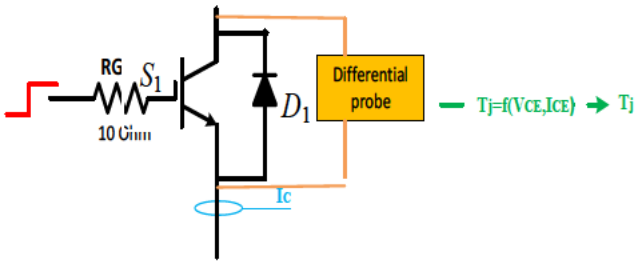


Figure 5.6: Measurement points

Here, V_{be} increases with reducing temperature and increases with increasing i_b. Although V_{be} is more sensitive to i_C than to temperature variations, an opposite trend for V_{CE} (MOSFET part) is expected. Voltage V_{CE} increases nonlinearly with i_C. The IGBT design combines the advantages of both the MOSFET and bipolar junction transistor. It has the thermal stability typical of the MOSFET structure and the low on-state voltage drop of the BJT structure. This is because of the conductivity modulation occurring in the drift-layer of the MOSFET. However, the advantages of the combination of PNP transistor and MOSFET is only achieved if a careful balance between them is carried out.

The MOSFET part of the IGBT introduces a positive temperature coefficient for $V_{CE,on}$ that leads to a homogenous current distribution over the area of the power device. If part of the device area has a higher temperature the local voltage drop is higher compared to the cooler parts of the device. This leads to a reduction in the current following through the hot part and improves temperature balance across the IGBT. However, this is true only if the MOSFET component is dominant. Otherwise a negative temperature coefficient for $V_{CE,on}$ appears. The current density increases in the hottest area because of the lower voltage drop. This leads to the destruction of the device as in the on-state a local hot spot arises with the consequence that the local temperature increases. The analytical model of the three components of $V_{CE,on}$ within an IGBT is shown in (5.7) [6] and detailed analysis of the temperature effect is reported when the collector doping concentration is high enough to avoid Schottky barrier effects.

$$V_{CE,on} = V_{NB} + V_{MOS} + V_{PN} \tag{5.7}$$

For a well-designed IGBT, V_{NB} and V_{MOS} increases while V_{PN} decreases with temperature. However, the increase in V_{MOS} and V_{NB}, equations (5.8) and (5.9), is much higher than the decrease in V_{PN} for well-designed IGBT [7]. An opposite trend can be seen for a thermally unstable IGBT. For a well-designed IGBT, V_{MOS} should be dominant. Voltage V_{MOS} is due to the MOSFET channel, V_{NB} is due to the drift layer, V_{NP} is due to the junction at the collector side [8].

$$V_{PN} = \frac{KT}{q} \ln\left(\frac{P_0^2}{n_i^2}\right) \tag{5.8}$$

In (5.8) and (5.9), K is Boltzmann's constant, P_0 is the hole concentration at the PNP emitter junction, D_a is the ambipolar diffusion, N_D is the drift-layer doping concentration, L_a is the ambient diffusion length, w is the drift-layer width, $b = \frac{\mu_n}{\mu_P}$, L_{CH} is the MOSFET channel length, w_{cell} is the cell pitch and the rest of the symbols belong to the standard notation for semiconductor device modelling [9].

$$V_{NB} = \frac{w_j}{\left(1+\frac{1}{b}\right)\mu_n q n_{eff}} - \frac{D_a}{\mu_n} \ln\left(\frac{P_0+N_D}{N_D}\right) \tag{5.9}$$

In a thermally unstable IGBT, the MOSFET contribution is drastically reduced. A very short MOSFET channel reduces the V_{MOS} component and high lifetime is defined in the drift region. Therefore, the drop in PN junction voltage V_{PN} becomes dominant. V_{on} has a linear decreasing trend with temperature leading to the thermal instability and premature failures due to hotspots.

Another reason for this negative temperature coefficient is the effect of rising of Schottky barrier height at the collector contact for low doping concentrations. However, this phenomenon cannot cause thermal instability. A possible reason for the doping concentration to be too low could be a reduced activation percentage of the implanted dopants. Since the collector diffusion is made by p-type dopant, the Schottky junction operates in reverse conducting conditions. Therefore, for a low V_{CE} the current is sustained by leakage current of the Schottky junction. Higher current levels can flow only if the breaking voltage condition is achieved, which is in range of a few volts. The Schottky barrier introduces an abrupt increase of the V_{CE} after a certain threshold current. With increasing temperature, this threshold current increases. When the temperature increases in the Schottky barrier area, the voltage drop increases. In contrast, if the temperature increases in the area without a Schottky barrier, the voltage decreases with temperature. Then the overall device exhibits a negative $V_{CE,on}$ temperature coefficient. In conclusion, the variation of V_{CE} with temperature is complicated and depends on each particular IGBT design, hence the need for good information before condition monitoring is possible.

5.3.2 Topology of interest to switching times

Not only static power losses (conductance power losses), but also dynamic power losses (switching losses) contribute to the heat generation inside IGBTs. Dynamic power losses can show their effect on dynamic inherent parameters of the IGBT, such as switching times. Switching times of an IGBT have the potential to make an effective failure detector. To date, the sensitivity of these inherent parameters to failure and load variations has not been investigated. The advantage of the set-up proposed in this thesis is accessibility of terminal measurements. Switching times also have the potential to have sufficient sensitivity to temperature and load variations based on (5.11) and (5.12) [10]:

$$t_{on} = R_G\ C_{GC}\left[\frac{V_S - V_F}{V_{GE,on} - V_{miller}(T)}\right], \tag{5.11}$$

$$t_{off} = R_G\ C_{ISS}\, log\left[\frac{I_L}{g_{m,sat}(T) - V_{th}(T)} + 1\right] \tag{5.12}$$

where R_G is the gate resistance. C_{IEE} is the input capacitance, which is constant. i_L is the load current. C_{GC} is the gate emitter capacitor, V_S is the voltage of DC power supply, V_F is the forward voltage across the IGBT. $V_{GE,on}$ is the gate-emitter voltage in the on state. T is temperature, which is constant during the experiment.

Equation (5.11) illustrates that an increase in DC-link voltage causes a reduction of t_{on} [11]. Gate current i_G charges C_{GE}, which is divided into gate oxide capacitance and junction region or depletion layer capacitance. Gate oxide capacitance can be considered constant as long as V_{GE} and temperature are kept constant. Nonetheless, the junction region capacitance increases with increasing V_{GE} as the region becomes wider with a decrease in the voltage across the IGBT [12]. Expansion of this region causes prolongation of switching times in the IGBT. The depletion layer capacitance has a negative correlation with V_{CE} according to equation (5.8) [13], and hence increasing V_{CE} leads to a decrease in $t_{d,on}$ and t_{on}, (5.13) [14]:

$$V_{GE} = \Delta V_s \times \left(1 - e^{-\frac{t}{\tau}}\right),\ \tau = \left(R_{G,ext} - R_{G,int}\right) \times C_{GE},\quad t_{on} = \tau\, log\left(1 - \frac{V_{GE,th}}{\Delta V_s}\right) \tag{5.13}$$

where $R_{G,int}$ is the internal gate resistance and $R_{G,ext}$ is external gate resistance, both are constant values for an IGBT. Here, C_{GE} is the gate emitter capacitance that varies with the DC-link voltage.

Switching times are categorised into switching on time (t_{on}), switching delay on time ($t_{d,on}$), switching off time (t_{off}) and switching delay off time ($t_{d,off}$). Understanding the switching characteristics of an IGBT is essential to estimate switching losses as well as measurements of switching parameters. Detailed switching of the IGBT under an inductive load is shown in Figure 5.9. The switching process can be divided into ten stages, as follows:

- Gate voltage rises to reach $V_{GE,\text{th}}$
- i_C rises
- i_C recovery due to diode reverse recovery
- V_{GE} plateau
- V_{GE} increases to reach the on-state gate voltage
- V_{GE} falling
- V_{GE} plateau
- V_{GE} rises
- i_C falls

- i_C reaches zero and the IGBT is fully off

The IGBT turn-on process starts from phase 1, when the on-state gate drive voltage is applied. Here V_{GE} rises to $V_{GE,th}$ and charges C_{GE} and C_{GC}.

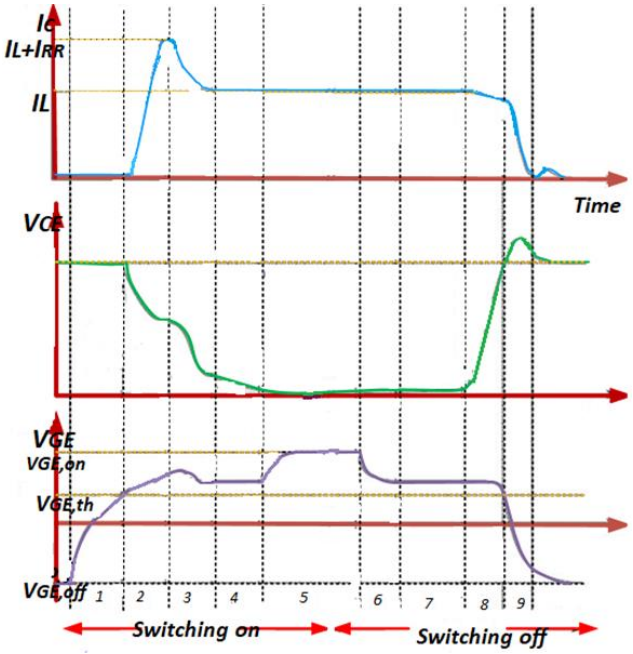


Figure 5.9: Switching waveform of the IGBT under inductive load [15]

Here, C_{GE} is small when the IGBT is off, hence the rise of V_{GE} is dominated by C_{GC}. The IGBT is essentially off until V_{GE} increases above V_{th} at the beginning of phase 2. In this phase, V_{GE} continues to rise. The inversion layer is built by V_{GE} and starts to conduct current, hence i_C begins to rise. As electrons are injected from the emitter to the drift region from the MOSFET channel, holes start to inject from the p-type collector into the drift region to neutralize the space charge.

The excess carrier density starts to rise, so the depletion layer shrinks and leads to a reduction in V_{CE}. In this phase V_{CE} is controlled by the combination of the voltage drops across the depletion layer (V_{dep}) and the drift region voltage drop (V_d). The voltage V_{dep} exponentially decreases as the depletion layer retreats while V_d increases as i_C rises. Since load current (i_L) is almost constant, i_C rises to its maximum value (i_L+i_{RR}) at the end of phase 2 due to the diode reverse recovery current. The MOSFET channel in this phase is saturated since V_{CE} is still high. Therefore, the MOSFET current (I_{MOS}) can be calculated by equation (5.14) [13] where K_{PL} is the MOSFET transconductance coefficient.

$$I_{Mos} = \frac{K_{PL}}{2}(V_{GE} - V_{TH})^2 \tag{5.14}$$

In phase 3, i_C drops from its maximum value towards its steady-state value i_L as the diode current starts to decay towards zero. The voltage V_{dep} continues to decrease as the depletion layer shrinks towards the P-well. V_d starts to drop from its maximum value with a decrease in i_C. The fall of these two voltages leads to the further decrease of V_{CE}. As V_{CE} decreases, the depletion layer under the gate shrinks laterally from the MOSFET channel towards the centre of the inter-chip region. The positive gate charge starts to attract free electrons from under the gate and forms the accumulation layer, which leads to a significant increase in C_{GC} [16].

During phase 4, V_{CE} continues to drop because of the shrinking depletion layer and the V_d drops due to increasing free carrier density in the drift region. However, the voltage across the MOSFET channel is still high enough to maintain its operation in the saturation region. V_{GE} is therefore clamped to the plateau value with a constant i_C. Most of the positive gate current (i_G) flows into C_{GC} to help build up the accumulation layer. Here, i_G can be calculated from (5.15), where $V_{GE,IMOS}$ indicates the required V_{GE} to support the MOSFET current [17]. According to the equivalent circuit shown in Figure 5.7, this could cause V_{CE} to decrease at a rate shown in (5.16) [18].

$$I_G = \frac{VG_{on\,state} - VG_{I,MOS}}{R_G} \tag{5.15}$$

$$\frac{dV_{GE}}{dt} = \frac{dV_{GC}}{dt} = \frac{I_G}{C_{GC}} \tag{5.16}$$

Once V_{CE} decreases and becomes close to its on-state value, the MOSFET channel enters the linear operation zone. Here V_{GE} becomes unclamped and starts to rise towards $V_{GE,on}$ at a time constant given in (5.17) [19].

$$\tau_2 = R_G(C_{GE} + C_{GC}) \tag{5.17}$$

Note that $\tau_2 > \tau_1$ since C_{GC} increases as the accumulation layer forms. The increase in V_{GE} will lead to the further reduction of MOSFET channel voltage and hence V_{CE} drops slightly with the rise in V_{GE}. Finally, V_{GE} reaches it steady on-state value. The IGBT turn-off process is almost the inverse sequence of the turn-on process and consists of the last 5 phases. At the beginning of phase 6, the positive gate drive voltage ($V_{\mathrm{GE,on}}$) suddenly changes to zero, $V_{\mathrm{GE,off}}$. This leads to discharge of C_{GE} and a negative gate current through R_G. The MOSFET channel operates in the linear region during the on-state, so the MOSFET channel voltage increases with the drop of V_{GE}. This leads to the slight rise of V_{CE} at a constant i_C. The voltage drop of V_{GE} due to the discharging of gate capacitance follows the time constant τ_2. At the start of phase 7, V_{CE} is high enough to force the MOSFET channel to enter the saturation region. Hence, V_{GE} is clamped to a constant value to hold the constant load current and consequently enters the plateau region. Therefore, the negative gate current is contributed to by the discharging of Miller capacitance (C_{GC}). As the accumulation layer disappears from the centre of the inter chip area towards

the MOSFET channel, C_{GC} starts to decrease and the resistance of the drift region increases which leads to the rise in V_{CE}.

The process enters phase 8 when C_{GC} is reduced significantly and its discharging current cannot support the negative gate current. Here, C_{GE} starts to discharge hence leads to decreasing V_{GE} and consequently decrease in i_C. Fewer excess carriers are injected into the drift region and the depletion layer, (or V_{CE}), builds up quickly. At the beginning of phase 9 as V_{GE} falls below V_{TH}, the MOSFET channel vanishes an all the DC voltage is appears across the IGBT.

As the MOSFET channel disappears, i_C drops sharply and produces a voltage across the circuit stray inductance (L_S) in the same direction as V_{DC}. This leads to V_{CE} turn-off overshoot and therefore forward bias of the freewheeling diode. The current then flows from the IGBT into the freewheeling diode. V_{CE} overshoot decays when di/dt decreases as the current commutation between IGBT and diode completes. Note that there might be some small oscillation in i_C at the end of this phase due to the interaction between the capacitance of IGBT and the stray inductance. V_{GE}, i_C and V_{CE} reach their final stable value in phase 10, where the turn-off process terminates.

In this work, switching parameters are obtained based on their standard definitions as explained in Figure 5.7 [20]:

- $t_{d,on}$ - turn-on delay time is the time from when the gate emitter voltage rises past 10% of the drive voltage to when the collector current rises past 10% of the specified load current.
- $t_{d,off}$ - turn-off delay time is the time from when the gate emitter voltage drops below 90% of the drive voltage to when the collector current drops below 90% of specified load current. This gives an indication of the delay before current begins to transition in the load.
- t_r - Current rise time is the time between the collector current rising from 10% to 90% of the load current.

In order to study the repeatability of measurements, each measurement was conducted three times. The mathematical relationships between rise time and fall time are described in (5.18) and (5.19). Measurement of switching times as failure detectors is challenging due to high sampling rate required to track V_{GE} and i_C in a fast switching converter. In order to evaluate switching time parameters of the proposed IGBT, an experiment setup has been built.

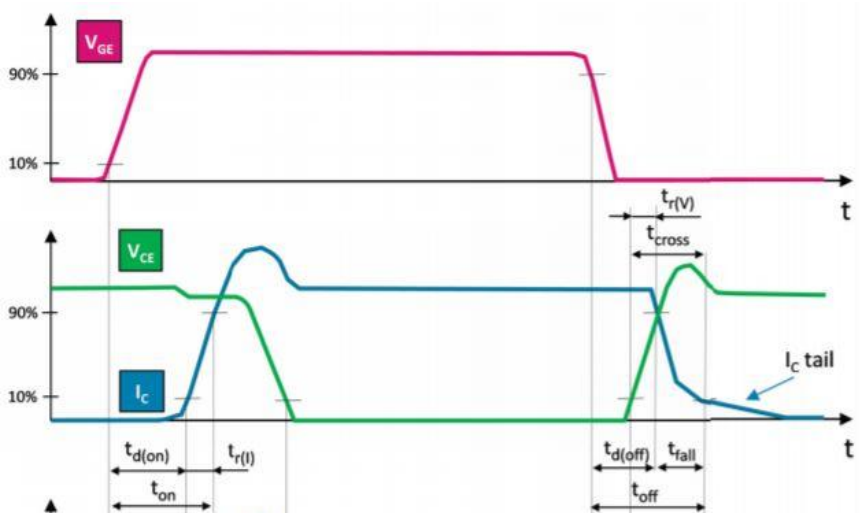


Figure 5.7: Switching time parameters [15]

$$t_{on} = t_{d,on} + t_r \tag{5.18}$$

$$t_{off} = t_{d,off} + t_f \tag{5.19}$$

5.4 Calibration of switching times

In order to calibrate switching times according to junction temperature variations, a double pulse test is run on one IGBT of one module with an inductive load. The pulse durations for the test are short so that the self-heating is negligible. Therefore, T_C is measured and assumed to be the same as T_j. The schematic of this test setup is shown in Figure 6.10. A predefined ambient temperature is important for this test. Thus, the tests are run in a lab environment. Ambient temperature is continuously monitored by a Pico data logger in order to make sure there is no deviation from the initial set temperature. The temperature can be set to a higher ambient temperature by means of the heated heatsink. The case temperature, heatsink and substrate temperatures are continuously measured during the test to monitor any deviation from the set temperature. The gate of the high-side IGBT is connected to its source to keep the upper IGBT off (open circuit). Its parallel freewheeling diode is conducting current through a pre-charged inductor. The low-side chip IGBT is used to divert this current away from the diode. This will initiate the reverse recovery of diode.

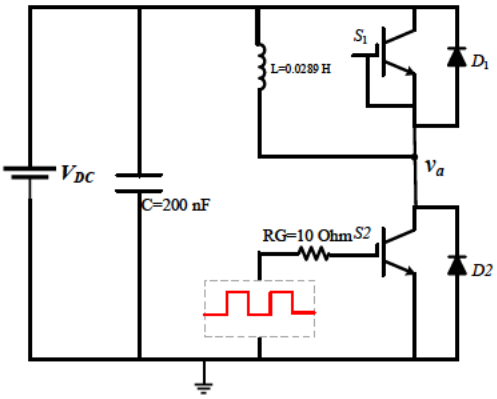


Figure 5.8: Electrical schematic of double pulse test

Figures 5.9 to 5.12 show the double pulse test in different stages. The direction of current can be followed in these figures according to the stage of the gate pulse applied to the lower side IGBT. As shown in the first stage (Figure 5.9), when the low side IGBT is switched on, the current in the inductor increases linearly with time, at a rate depending on the inductance and power supply voltage (V_{DC}). In the next stage (Figure 5.10), when the IGBT is switched off, the current flows through the high-side diode. A current loop between the inductor and diode will be generated so that the current remains nearly constant (it does decay by a small amount). In third stage (Figure 5.11), the lower IGBT is again turned on, the stored current in the inductor flows through the low-side IGBT. In the last stage (Figure 5.12), loop current is again generated and current circulates it falls to zero because of loop resistance.

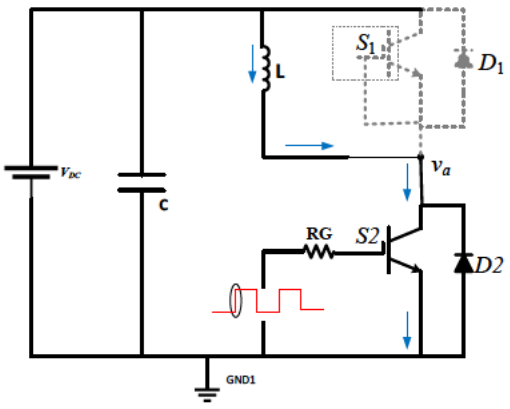


Figure 5.9: Stage.1: the inductor current ramps up by the DC power supply

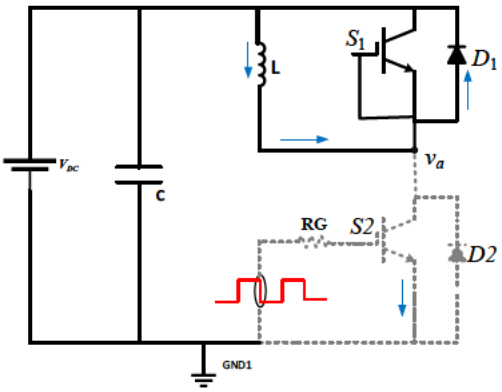


Figure 5.10: Stage.2: current path through high side the freewheeling diode and inductor

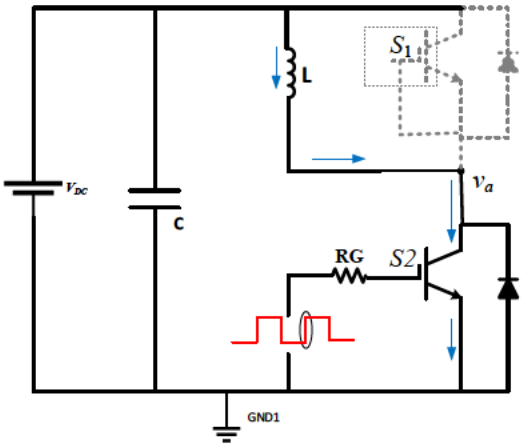


Figure 5.11: Stage.3: discharge the inductor to the low side IGBT

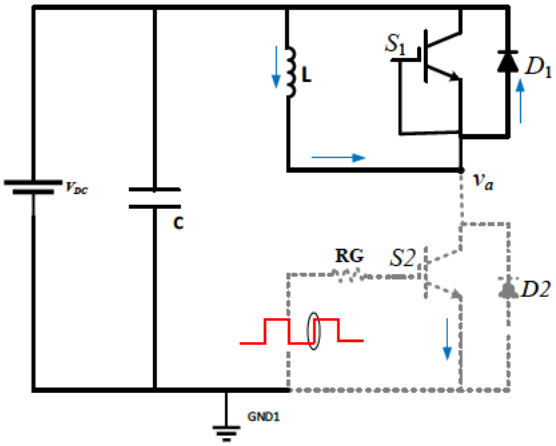


Figure 5.12: Stage.4: current circulation in the inductive loop

The measurement has been carried out at several temperatures (25 and 150 ºC) in order to calibrate variations of switching times with temperature. Relationship between T_j and switching times t_{on}, t_{off}, $t_{d,off}$ and $t_{d,on}$ have been identified. An example of the gate pulse voltage, load current, collector current and collector emitter voltage are shown in Figure 5.13. The DC power supply is 100 V and the

load current is 80.3 A at 25º C. Although the power supply cannot sustain 80 A, its internal capacitance allows this high current to be reached for a short time. The pulse durations are indicated in Figure 5.15 The first pulse duration determines the magnitude of the load current. Temperature is recorded by T-type thermocouples attached to case of the IGBT. The measurement strategy is discussed later in section 5.6.

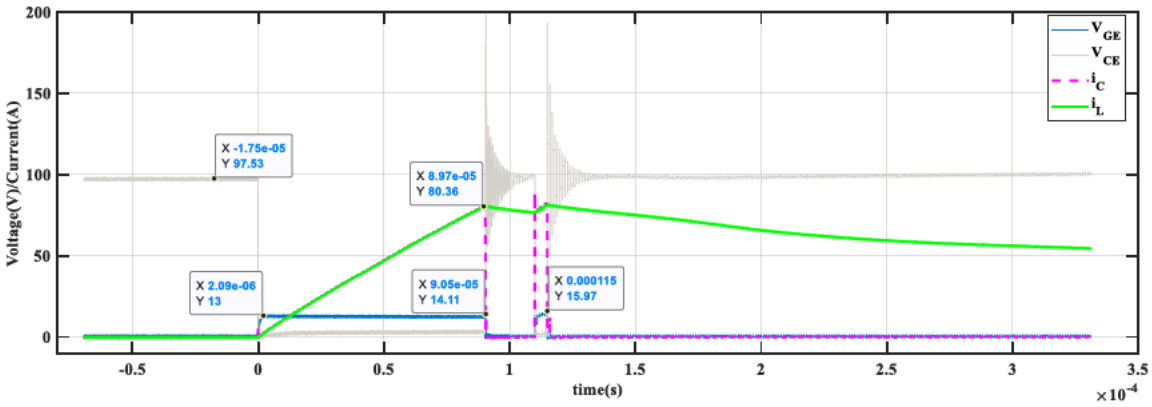


Figure 5.13: Signal outputs seen during a double pulse test

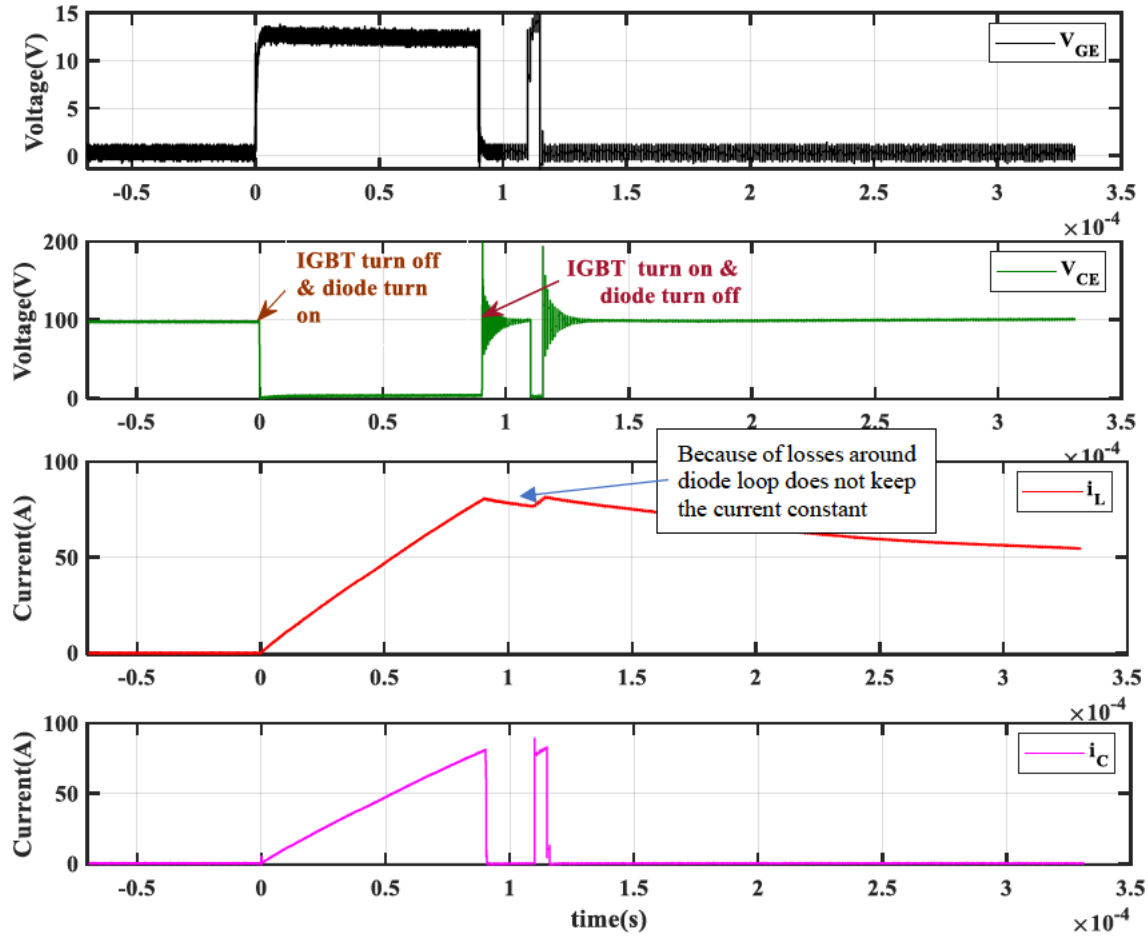


Figure 5.14: Example of double pulse test output

5.5 Results of calibration

Three different parameters, V_{GE}, V_{CE} and i_c, have been measured simultaneously to obtain switching times. The associated turning on switching times, t_{on} and $t_{d,on}$ are obtained at three different temperatures: 25, 80 and 150ºC. The best fit lines and the temperature variations are shown in Figure 5.15 and Figure 5.16. The results show that t_{on} decreases very slightly with temperature but increases with current (but only by about 15 ns for a current increase of 20 A). The sensitivity of t_{on} to temperature increases with increasing load current, but the change of switching time with temperature is already so low that this is of no consequence. On the other hand, $t_{d,on}$ shows a reduction with increasing temperature, but shows a smaller change with current, about 5 ns for a 20 A change. The sensitivity to temperature (slope) is independent of the load current. Switching time $t_{d,on}$ is measured while no current is flowing in the device, action just takes place in the MOSFET structure, while the gate-emitter capacitance (C_{GE}) is charged. Consequently, the switched current should not affect $t_{d,on}$. Among all the switching times, this one changes least with load current.

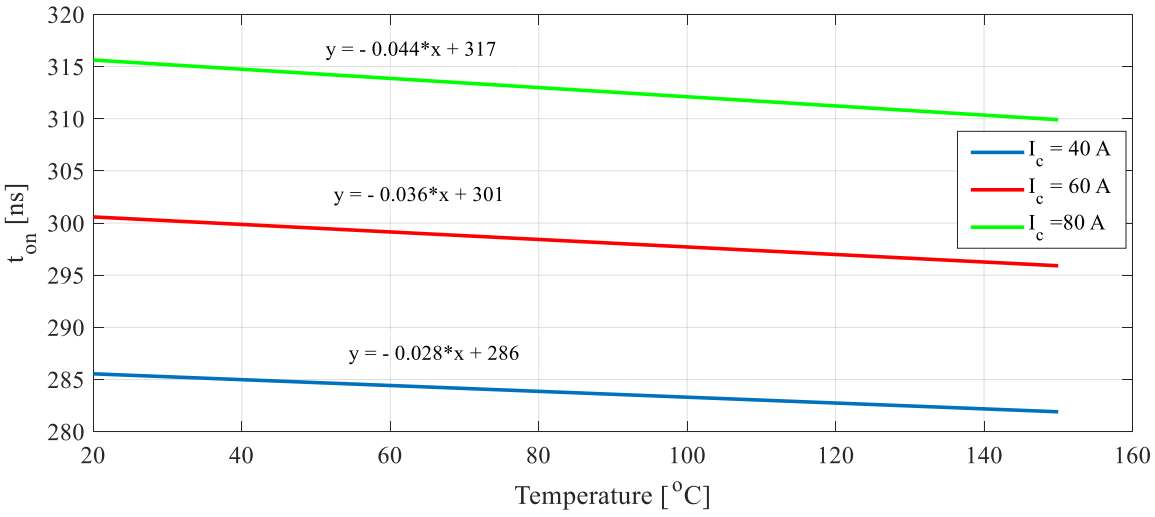


Figure 5.15: t_{on} versus temperature at different load currents

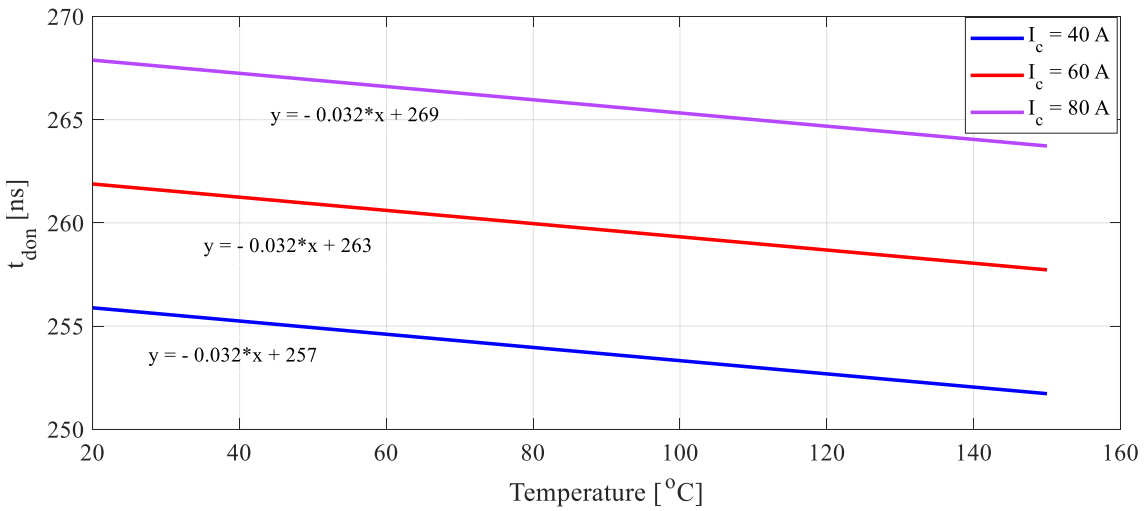


Figure 5.16: $t_{d,on}$ versus temperature at different load currents

Switching time parameters associated with the turning off of the IGBT (t_{off} and $t_{d,off}$) are also compared at different temperatures and load currents, Figure 5.17 and Figure 5.18. The results show a positive correlation between T_j and t_{off}. Time t_{off} increases with temperature faster for higher load currents while $t_{d,off}$ has increasing sensitivity to temperature at higher currents but has a crossover point where all the load currents show about the same $t_{d,off}$. A comparison table between sensitivity of switching time parameters to the temperature is shown in Table 5.1. The sensitivity of t_{off} to temperature is higher than other switching times parameters listed below.

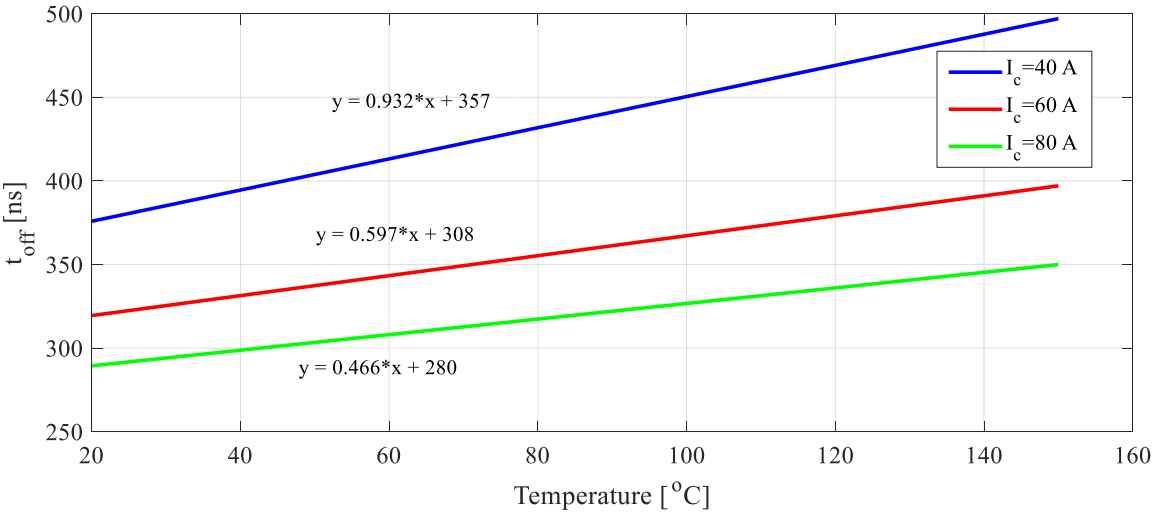


Figure 5.17: t_{off} versus temperature at 3 different load currents

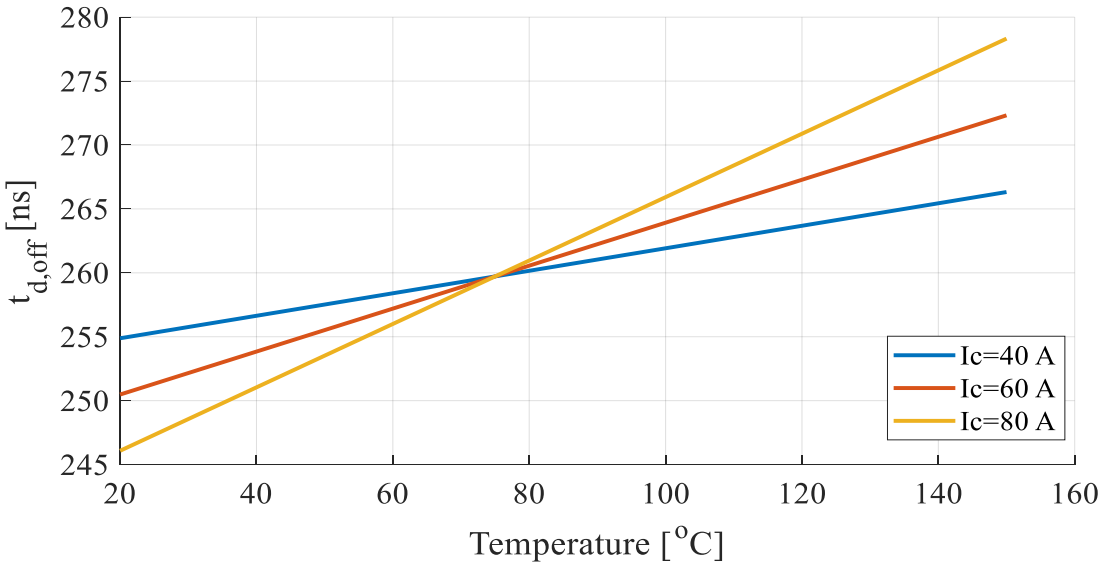


Figure 5.18: $t_{d,off}$ versus temperature at 3 different load currents

Table 5.1: Sensitivity of switching times to temperature (at 70V)

Sensitivity of switching times to temperature (ns/°C)				
i_L	t_{on}	$t_{d,on}$	t_{off}	$t_{d,off}$
40 A	-0.028	-0.032	0.932	0.088
60 A	-0.036	-0.032	0.597	0.168
80 A	-0.044	-0.032	0.466	0.248

The switching times are also variously sensitive to the DC-link voltage (that can be regarded as V_{CE}). However, this is not considered to be important here because the DC-link voltage, and hence the voltage of operation of the IGBT devices, is almost constant for a given application.

Based on available data, equations were estimated for the switching times. Most are linear, the changes in switching time are not large, but one has an exponential term as using a linear fit led to negative switching times at some temperatures so an exponential term made more sense.

At 25° C degrees, 70 V:

$$T_{don} = 243.724 + 0.3I_c \quad (5.20)$$

$$T_f = 11.68 + 0.45I_c \quad (5.21)$$

$$T_{on} = T_{don} + T_f = 268.904 + 0.75I_c \quad (5.22)$$

$$T_{doff} = 263.32 - 0.2I_c \quad (5.23)$$

$$T_f = 152e^{\frac{-(I_c-30)}{28.3}} + 18.45 \quad (5.24)$$

$$T_{off} = T_{doff} + T_f = 281.77 - 0.2I_c + 438.7594\, e^{\frac{-I_c}{28.3}} \quad (5.25)$$

At 150º C degrees, 70 V:

$$T_{don} = 239.724 + 0.3I_c \quad (5.26)$$

$$T_f = 14.18 + 0.4I_c \quad (5.27)$$

$$T_{on} = T_{don} + T_f = 253.9 + 0.7I_c \quad (5.28)$$

$$T_{doff} = 254.32 + 0.3I_c \quad (5.29)$$

$$T_f = 18.45 + 847.0693\, e^{-0.0346 I_c} \quad (5.29)$$

$$T_{off} = T_{doff} + T_f = 272.77 + 0.3I_c + 847.0693\, e^{-0.0346\, I_c} \quad (5.30)$$

A contour plot for T_j as a function of t_{off} and I_c is shown in Figure 5.19. This was generated by computing the switching times as functions of temperature and current but then using Matlab to plot the contour graph using current and switching time as the x and y axes and temperature as the z axis. This leads to some odd behaviour at high and low temperatures where the contour fitting does not have enough information to fill in the lines, but continuous lines should be imagined.

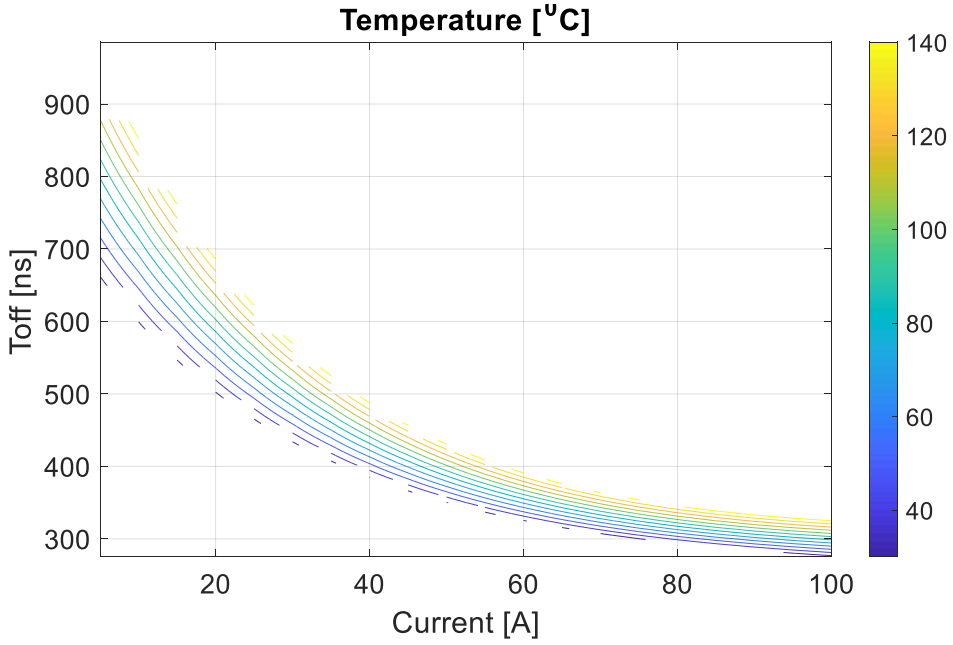


Figure 5.19: A 2D contour plot for t_{off} under a DC link voltage of 70 V

Based on this relationship, the T_j can be estimated given a collector current and a switching time t_{off}.

5.6 Emulating failure mechanisms

Two common failure mechanisms, BWLO and SF, are simulated in this section. Sensitivity of failure detectors to these failures is evaluated. Figure 5.20 is used to study sensitivity of $V_{CE,on}$ to progress of SF and BWLO.

5.6.1 Imposing bond wire lift-off

As explained in the previous chapters, $V_{CE,on}$ is not an appropriate quantity to estimate the temperature. Firstly, $V_{CE,on}$ has higher sensitivity to temperature in comparison with the failure mechanisms. Secondly, the relationship between temperature and $V_{CE,on}$ is nonlinear for low i_C in most IGBTs and shows higher sensitivity to the current variations with a positive correlation [16]. That is why $V_{CE,on}$ can be an efficient failure detector for detecting premature BWLO. However, BWLO also coincides with a noticeable change in temperature at high load currents. In the presence of BWLO, temperature increases at the PN junction, increasing the intrinsic carrier concentration. This will result in voltage drop at the PN junction. This will also coincide with a significant increase in V_{cost} due to a decrease in internal emitter resistance (5.31).

$$V_{CE,on} = V_j + V_{drift} + V_{mos} + V_{const} \tag{5.31}$$

where V_j is P^+ - N^- junction drop. V_{drift} is drift region drop (N^- layer). V_{mos} is accumulation region drop (P^- layer) and V_{const} is electrical constant resistance.

BWLO has been imposed on the experimental test rig in a discrete way by cutting wires manually. The temperature of the IGBT is kept constant by applying only short gate pulses. The case temperature is continuously monitored by thermocouples. This helps to separately study the sensitivity of failure detectors at difference health levels. Different health levels go from healthy (no bond wires cut) to most unhealthy (5 bond wires cut). The status of 6 bond wires having been cut is excluded as this is the broken state and is easy to detect.

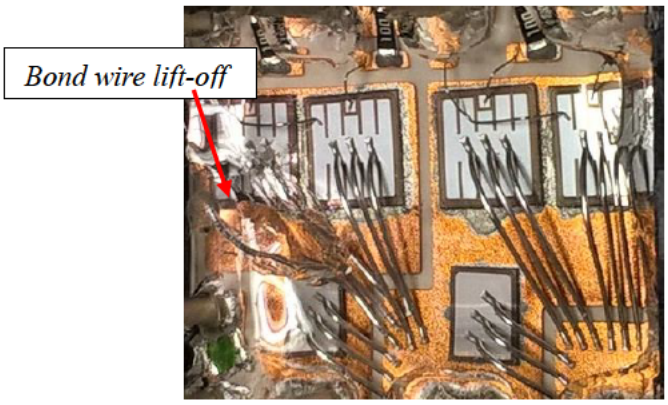


Figure 5.20: BWLO

5.6.2 Detection of bond wire lift-off

The bond wires that connect the silicon die to the terminal pins can be modelled by a resistor in series with an inductor. The resistances are calculated based on length and thickness of the bond wires that are shown in Figure 5.23. The diameter of the power connection wires is 0.381 mm and 0.15 mm for the signal connections. The electrical resistance of the power bond wires are a matter of concern in this work and they have two different values for resistance as the lengths are not same for two parallel chips, about 0.14 mm difference due to the geometry of IGBT module. The bond wire resistances are assumed similar for all bond wires, 0.522 mΩ. In experimental model bond wire however apply through manually connecting the bond wires and detected as described below.

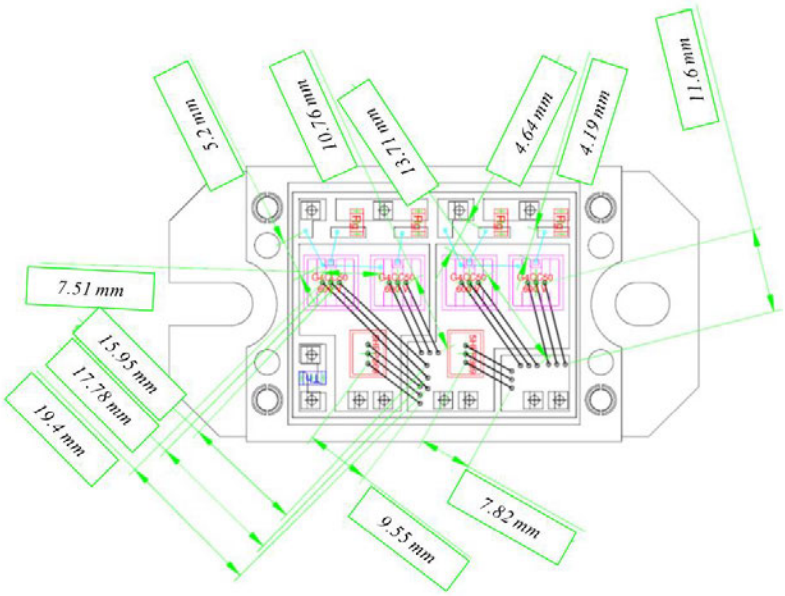


Figure 5.23: Bond wires dimensions

BWLO is detected through monitoring $V_{CE,on}$ at predefined i_C and T_j values. Load current i_C is continuously measured through a current sensor and recorded by an NI instrument. Temperature T_j is extimated by obtaining t_{off} as a temperature detector. The fitting equation (5.6) is used to estimate T_j for a given DC voltage. The relationship between $V_{CE,on}$ and T_j is shown in (5.29). Any deviation from $V_{CE,on}$ can be interpreted as indicating the presence of BWLO. The calibration circuit is used to examine the variation of $V_{CE,on}$ at different levels of bond wires lift-off, i.e. from one bond wire cut to 5 bond wires cut. Higher sensitivity of $V_{CE,on}$ to i_C make this parameter a good failure detector of BWLO. This is due to the increase in emitter resistance caused by cutting additional bond wires, summarised in Figure 5.21.

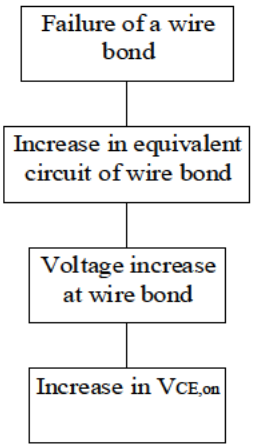


Figure 5.21: Detection of BWLO

An NI instrument was used to measure $V_{CE,on}$ as a failure detector parameter. Any deviation of $V_{CE,on}$ at a certain i_C and T_j can be interpreted as possible changes in the bond wires. As shown in Table 5.2, the sensitivity of $V_{CE,on}$ to T_j increases as the number of cut wires increases from -0.8 to +1.6 mV/C. In addition, the change in $V_{CE,on}$ sharply increases with an increasing number of cut bond wires. Figure *5.22* shows the sensitivity of $V_{CE,on}$ to BWLO at different initial temperatures, varying from 25, 85 and 150ºC. With an increasing number of cut wires, a higher increase in $V_{CE,on}$ can be observed. As shown in this figure, with increasing temperature, $V_{CE,on}$ shows lower sensitivity to BWLO.

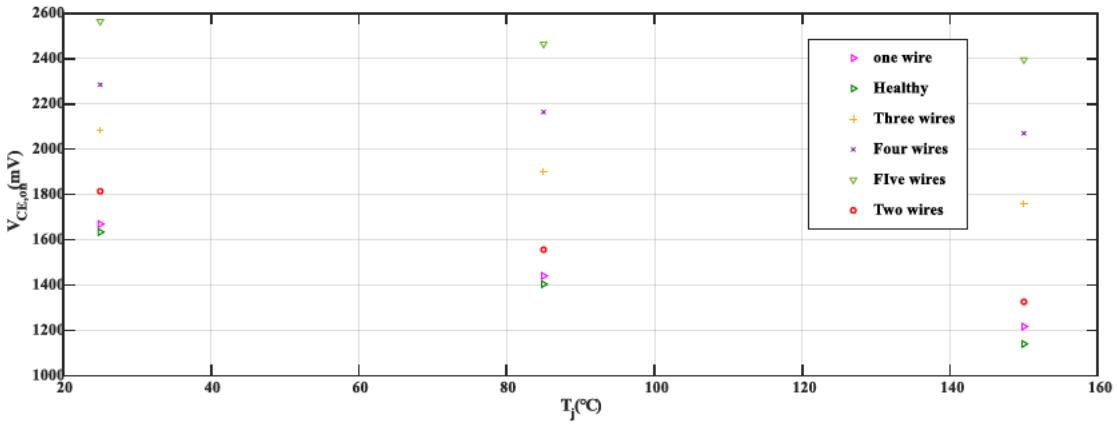


Figure 5.22: Sensitivity of $V_{CE,on}$ to BWLO at 85 A

Table 5.2: Sensitivity of $V_{CE,on}$ to T_j with the progress of bond wire lift off

Temperature (°C)	Healthy (mV)	One bond wire cut (mV)	Two bond wires cut(mV)	Three bond wires cut(mV)	Four bond wires cut(mV)	Five bond wires cut(mV)
25	1634	1669	1814	2084	2284	2564
85	1404	1440.5	1556	1900	2164	2464
150	1140	1216.8	1326	1760	2070	2395

5.6.3 Detection of BWLO using $V_{CE,on}$ as failure detector and t_{off} as a junction temperature estimator

Load current i_L was simultaneously recorded with an NI equipment. Temperature T_j is estimated by monitoring t_{off}. This switching time parameter shows the highest sensitivity among other tested switching times (t_{on}, $t_{d,on}$ and $t_{d,off}$) as discussed in section 5.9. As previously discussed, switching time varies with load current, T_j and DC power supply voltage. The DC voltage was kept constant and hence a three-dimensional equation (5.5) can be applied to estimate T_j. Load current was also measured with a current sensor at the same time. In order to study effect of load variations (wind speed) on the TSEPs, the WT without blades (explained in chapter 5) was used as a load for the converter. Figure 5.23 shows this test set up. The three-phase converter was initially run with a WT (as a PMSM) and later on, to draw higher current, another motor was added in parallel with the WT.

Failure detectors are calibrated to monitor the temperature and load variations. Failure has been applied to the IGBT and their effect on the proposed failure detector, $V_{CE,on}$ and the switching times, has been studied. Effect of failures on the failure detectors should be studied from the early stages degradation to full breakdown of the IGBT. In next step, the effect of wind speed variations on the IGBT is been emulated through variation in generator current and frequency. To clarify this effect on IGBT, sensitivity analysis was applied to different load variations.

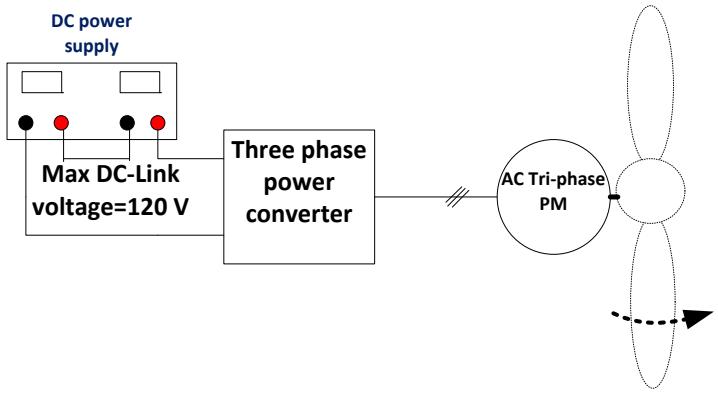


Figure 5.23: The test set up

A current of 5 A to 6 A is enough for calibration of the IGBT failure detectors. However, it is not enough for studying the effect of failure mechanisms on failure detectors. With a rated current of 50 A at 100°C and due to lack of facility, reaching this value was not possible. One way to increase the load current is to add load in parallel with the wind turbine. This was done by adding two AC-DC motor-generator sets, with or without the PMSM, as shown in Figure 5.24 and Figure 5.25. The motor-generator set conveniently had variable electrical load on the DC side, so the load, and hence current, could be varied up to a maximum of 17 A per phase that was used to reach 20 A on the converter side.

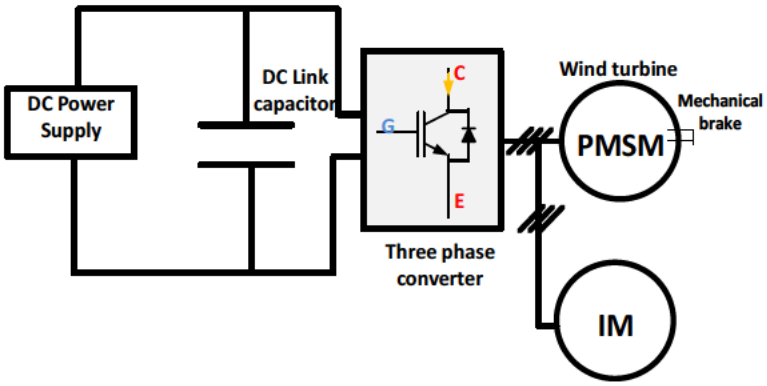


Figure 5.24: Induction machine in parallel with PMSM

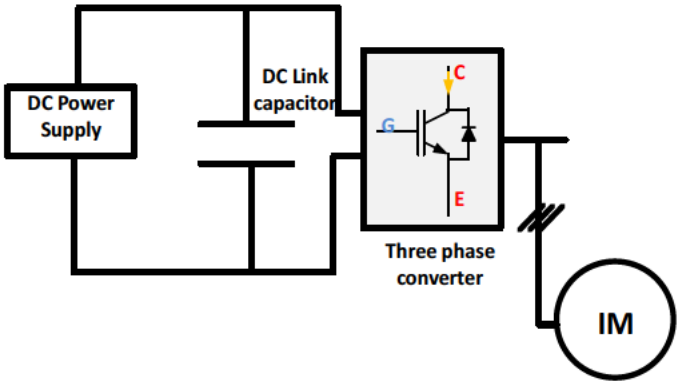


Figure 5.25: Induction machine only

5.7 Measurement of switching time

The switching time parameters measured for this test were the switching-on time (t_{on}), the switching delay on time ($t_{d,on}$), the switching-off time (t_{off}), and the switching delay off time ($t_{d,off}$). Four additional parameters were measured at the same time: T_j, i_C, V_{CE} and V_{GE}. The measurement data are shown in Figure 5.26. Various measurement tools were used to measure output voltages and currents of the converter as well as the electrical parameters of the IGBT. A digital storage oscilloscope (with part number MSO 3054, 500 MHz) was used. Two current probe amplifiers (TCP A300, 500 MHz bandwidth) with current probes (TCP 305A, bandwidth 50 MHz) were used. Differential voltage probes (P5200A, 50 MHz bandwidth) and low output impedance were used to measure $V_{CE,on}$ and V_{GE}. The output of the oscilloscope, sampled at 2.5 GS/s, was saved for further processing in Matlab. There are oscillations present, particularly in the V_{GE} and i_C signals. These are caused by stray inductance and parasitic elements of the IGBT and the surrounding power circuit. A 4th-order low-pass discrete-time Butterworth filter with a normalised cut off frequency ω_n of 0.025 was applied to the original waveform. This filter helps to reduce large oscillations at high frequencies.

A state machine algorithm was developed to process the measured data to end up with switching time parameters. These tests were run with a three-phase sinewave PWM signal on a high voltage IGBT module at temperatures from 25 to 150°C. This operating mode is more like to be used in a real application than that of adopted in the usual DC power cycling load test (using constant current) which has been used in previous studies.

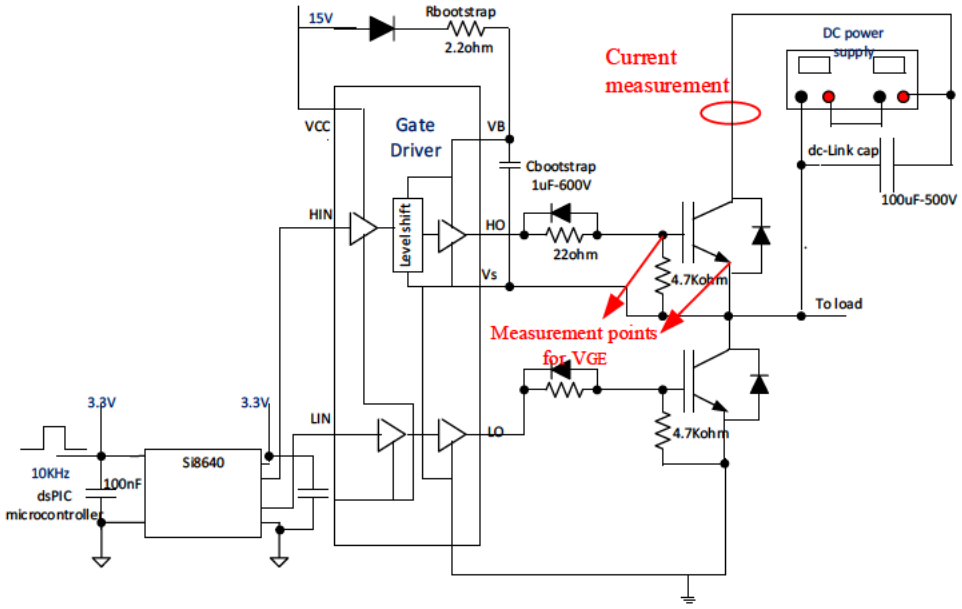


Figure 5.26: Measured points to measure V_{GE} and i_c

To find the 0% and 100% levels of V_{GE} (off/on levels), a histogram was constructed to find out where the data spent most of its time. The two peaks show the 0 and 100% signal levels. The same technique was used to find 100% of load current from i_C. Once the 0% and 100% levels are known, it is relatively simple to find values for 10% and 90% assuming a linear change of the variables.

Subsequently, the fall time of $V_{GE}$from 90% of the steady state to 10% was estimated. In Figure 5.27 the red dots show 90% of V_{GE} during fall time and blue dots show 10% of V_{GE} during the rise time. Later, the 90% fall time and 10% time of i_C were found. Red dots in Figure 5.10 show 90% i_C and blue dots show 10% i_C. The rise time is defined when i_C goes to maximum value and the IGBT is turned on. Fall time is defined when i_C goes to zero and IGBT is turned off.

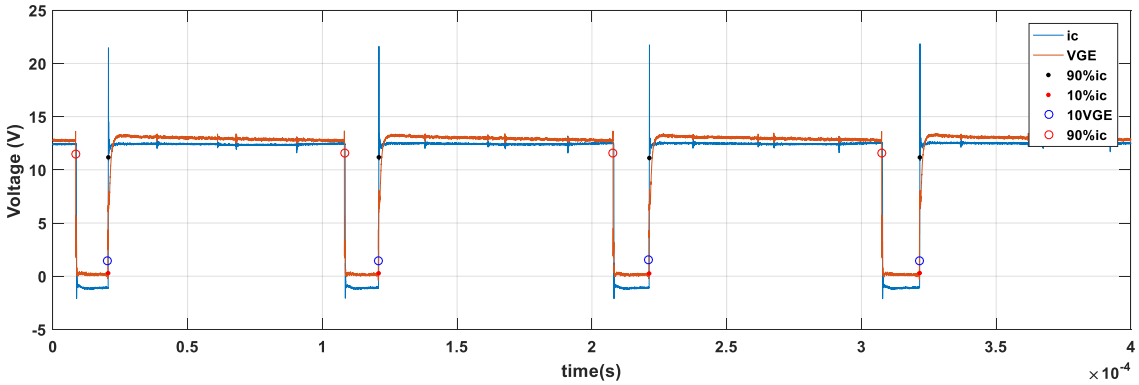


Figure 5.27: 90% and 10% of i_c

The challenging issue of this measurement is the oscillations of the waveforms within switching of the other IGBT modules as well as stray inductance and other parasitic elements of IGBT, tracks and capacitors. Figure 5.28 shows that several points are picked up as 90% V_{GE} (black dots) and 10% of V_{GE} (green dots). The experiment results in Figure 5.28 and Figure 5.29 were obtained with a 50 V DC-link voltage, and with i_C about 2 A. The measurement was done with a healthy IGBT at an ambient temperature of 25° C.

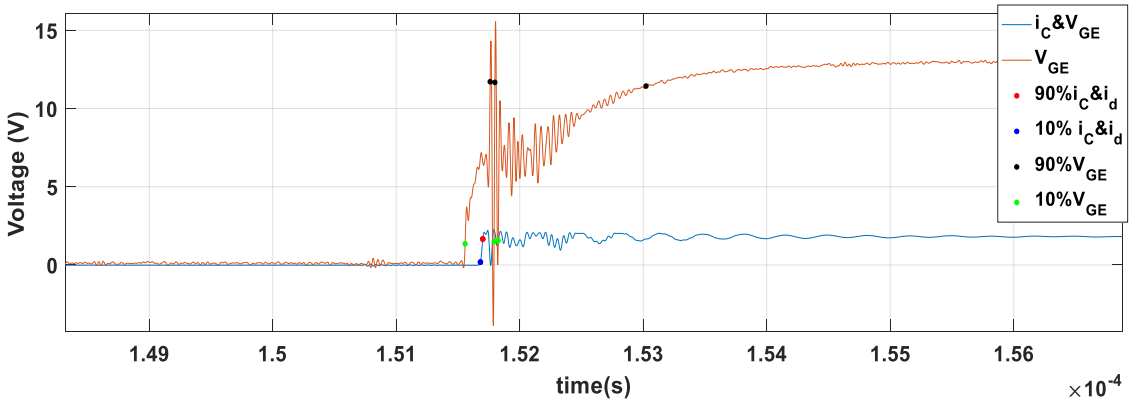


Figure 5.28: 10 % V_{GE}, 10% and 90% of i_c

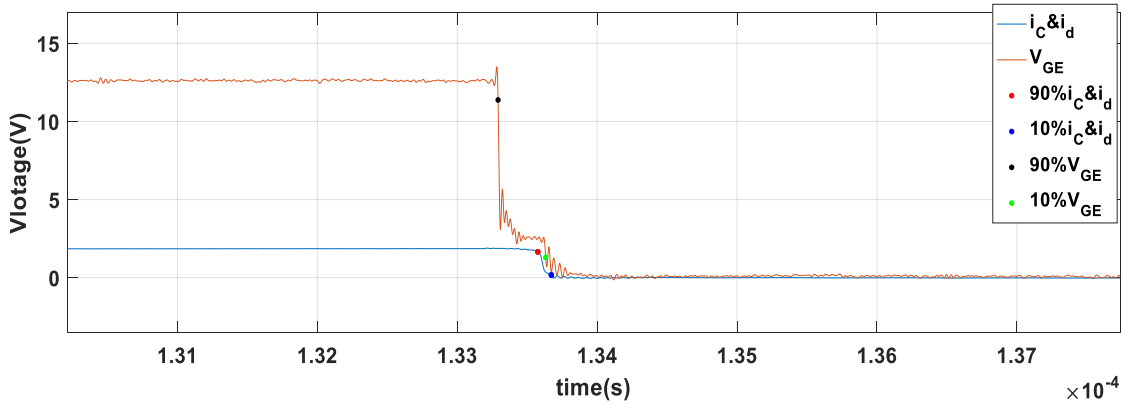


Figure 5.29: 90% V_{GE}, 10% and 90% of i_c

To find 10% of i_C, the correct point is defined based on the closest points to 10% of V_{GE}. To find 90% of i_C during rise time, correct point is defined based on the closest point to 10% of i_C. This is shown more clearly in Figure 5.30. To find 90% of V_{GE} during the fall time, the correct point is defined based

on considering the closest points to 10% of V_{GE} as a reference point. To find 10% of i_C, the correct point is defined based on the closest points to 90% of i_C as reference. This is shown more clearly in Figure 5.31.

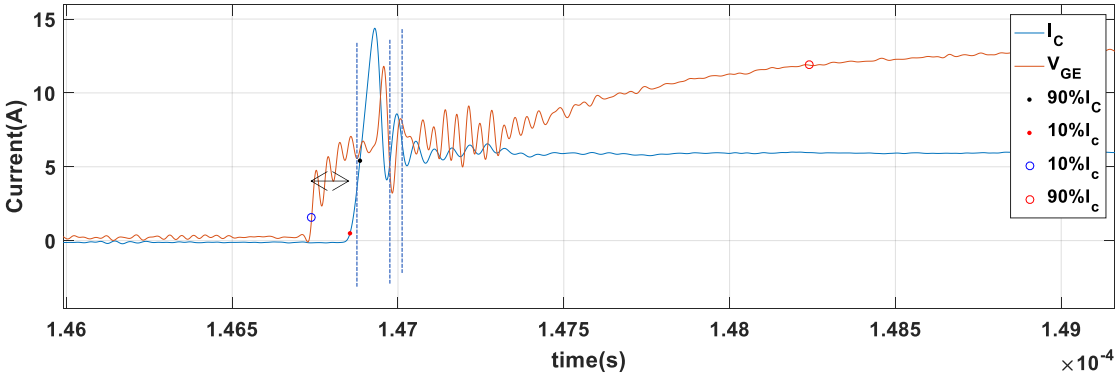


Figure 5.30: Switching-on time of the IGBT

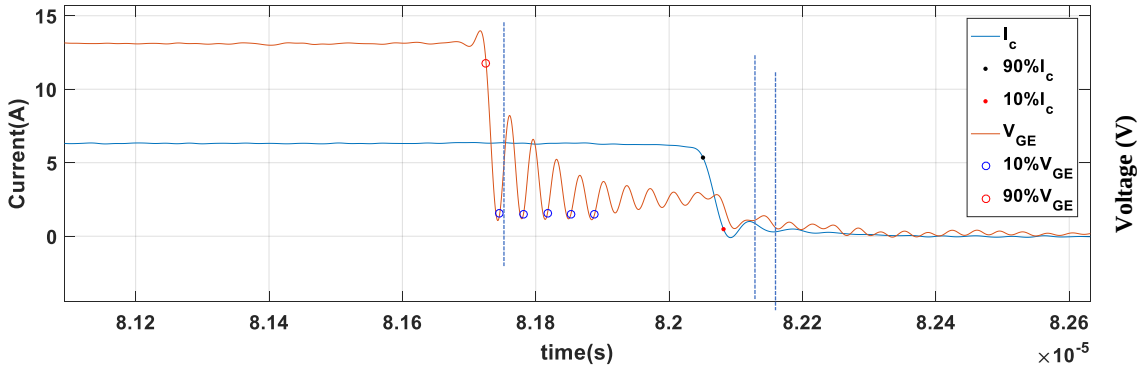


Figure 5.31: Switching-off time of the IGBT

Voltage $V_{CE,on}$ was measured with the evaluated board. Current i_C and V_{GE} and i_L were simultaneously measured and recorded. The measured $V_{CE,on}$ was compared with $V_{CE,on\ cal}$. That was obtained from a calibration test. BWLO was altered in a discrete way, as previously, by cutting the bond wires one by one. The amplitudes of spikes can be reduced by adding a snubber circuit across the module. However, still a certain oscillation can be observed due to fast switching of IGBTs and its effect on LC components within the circuit.

The purpose of the snubber circuit is to limit the value of dv/dt across the module to reduce the switching power losses [22]. Figure 5.32 shows the snubber circuit that consists of a capacitor, a diode, and a resistor connected across the gate to emitter terminals. At the IGBT is turned off, the current will be diverted into the snubber capacitor, C_s through the diode D_s. The IGBT voltage is clamped to the capacitor voltage, which is initially zero. The larger the capacitor, the slower the rise of the device voltage for a given load current.

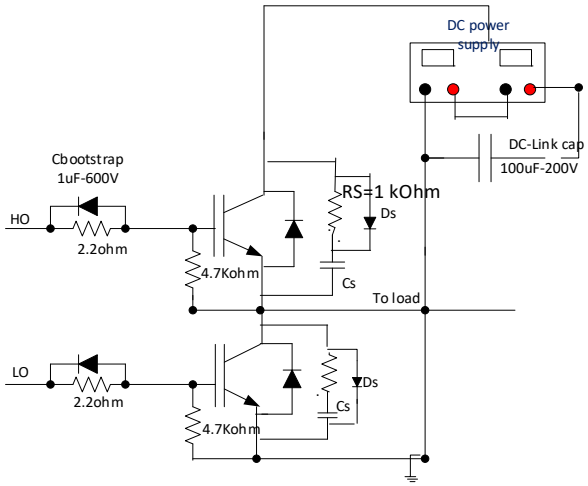


Figure 5.32: Circuit schematic including the snubber

A snubber circuit can be designed using the capacitance calculated by (5.32). Each phase of the converter is designed to carry a maximum current of 20 A. Therefore, the IGBT's current is assumed to be 20 A and the turn-off linear current time was measured without considering the snubber circuit (t_{fi} = 150 ns). Substitution these values in equation (5.33), the snubber's capacitance is calculated as shown in equations (5.34) and (5.35) [23].

$$i_{sw=C_s\frac{v_{sw}}{t_{fi}}} \tag{5.32}$$

$$C_s = (20) \times \frac{150ns}{V_{dc_{link}}(100V)} = 30\ nF \tag{5.33}$$

The snubber's capacitor is discharged during turn-on and must be discharged within the switch minimum on-time, $t_{on,\min}$. This means that the time constant of the designed RC snubber circuit must be much smaller than $t_{on,\min}$

$$R_sC_s \ll t_{on,min} \tag{5.34}$$

Considering a minimum duty cycle of 10% (δ_min = 10%), a switching frequency of 10 kHz and the value of $t_{on,min}$ is approximately five times R_sC_s, the snubber resistance is:

$$R_sC_s = t_{on,min} = \frac{\delta_{min}}{f_{sw}} = \frac{0.1}{10000} \quad R_s = 66.6 \approx 68\Omega \tag{5.35}$$

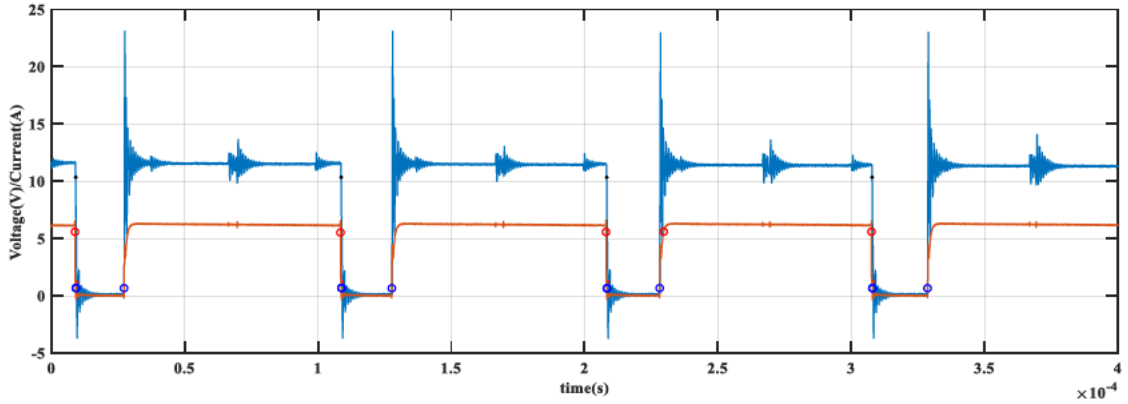


Figure 5.33: V_{GE} (blue) and I_C (orange) without snubber

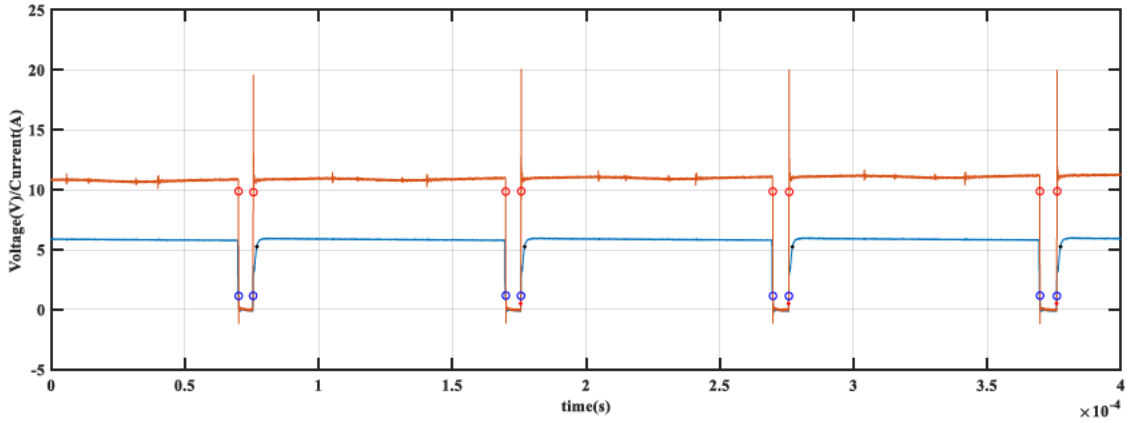


Figure 5.34: V_{GE} (blue) and I_C (orange) with snubber

As shown in Figure 5.33 and Figure 5.34, current oscillations are reduced by adding the snubber circuit. This reduction eases processing of the measured data to find switching times. However, the RC components of snubber circuit increase the switching times of the IGBT and hence switching losses. Thus, the snubber circuit should be designed to make a trade-off between increase in switching times and reduction in current oscillations. The designed processing algorithm can pick the correct 90% and 10% points of V_{GE} and i_C with or without a snubber being present. In a real converter operation, the switching times are assumed to be fixed once the snubber circuit is fixed, so variations in switching time are all that is required for fault detection. Table 5.3 shows measured switching times with and without the snubber circuit being present, showing that the snubber circuit affects the measured switching time, increasing each one when present.

Table 5.3: Switching times with and without snubber circuit

DC-link voltage is 50 V at 150ºC, 80 A	t_{off} (ns)	$t_{d,off}$ (ns)	t_{on} (ns)	$t_{d,on}$ (ns)
without snubber circuit	275	230.3	260	212.2
Including snubber circuit	319.7	262.2	310.2	263.2

A number of tests were carried out to measure the sensitivity of switching parameters for a different numbers of cut bond wires. As shown in Figure 5.35, the sensitivity of $t_{d,off}$ to the number of cut wires is about -0.8 (ns/number of cut wires) although it increases to -4.2 ns from healthy to only one bond wire remaining. A significant increase in t_f is related to the earlier turn off mode. Sensitivity of $t_{d,off}$ to the number of cut wires is about -28 (ns/number of cut wires) although it increases to -160 ns from healthy status to 5 bond wires lifted off. This significant change should be due to the faster discharge of IGBT parasitic capacitances within the progress of failure and decrease in the length of the Miller plateau. The low negative sensitivity of t_{off} to the progress of BWLO is because the switching t_f increases with increase in number of cut wires and $t_{d,off}$ reduces significantly. A significant increase of the fall time t_f is related to the earlier turn off mode, the variations of $t_{d,on}$ and t_r are smaller due to the lower earlier turn on mode.

Decrease in $t_{d,off}$ and increase in t_f results in t_{off} being almost constant with the progress of BWLO. In fact, t_{off} is almost independent of BWLO. This independence makes it possible to use t_{off} as a good temperature sensor. It is necessary to mention that the variations of $t_{d,off}$ and t_f cannot alter the switching speed of the devices. In fact, the $t_{d,off}$ plus t_f (t_{off}) remain almost constant after cycling. In Figure 5.35, 0 represents the healthy state, and 1 is one wire lifted off, 2 is two bond wires lifted off, and so on.

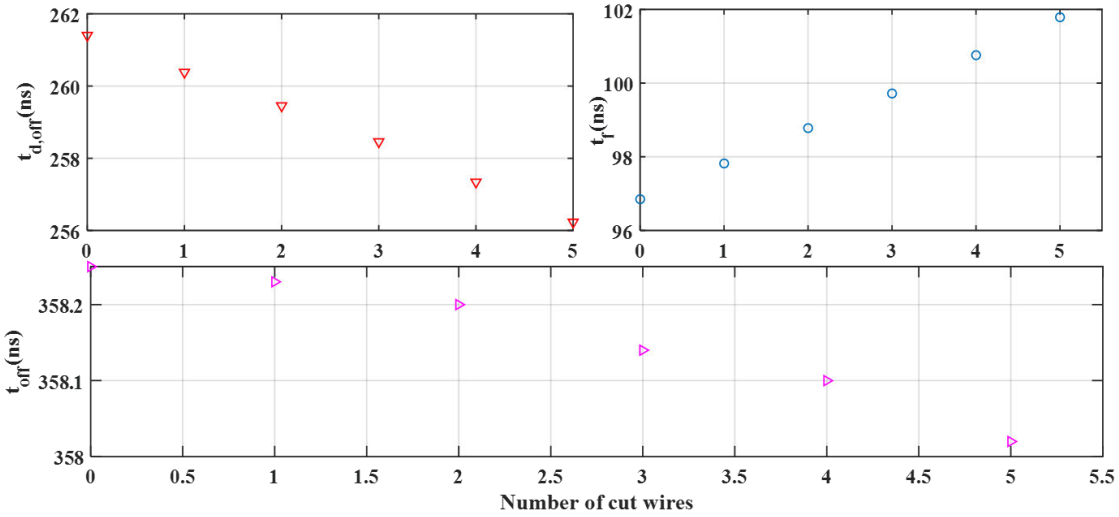


Figure 5.35: Variations of $t_{d,off}$, t_f and t_{off} with the number of cut wires

Quantity $V_{CE,on}$ was sensed using a precision difference amplifier that can accept a common mode voltage of up to 600 V. Variation of $V_{CE,on}$ has been studied in presence of BWLO for the three-phase converter (shown in Figure 5.11). T_j is estimated at 65ºC through (5.46). The figure shows a pattern of $V_{CE,on}$ against current that represents the IGBT behavior for positive currents. As shown in Figure 5.36, $V_{CE,on}$ increases from healthy mode to 5 wires cut within operation of the converter.

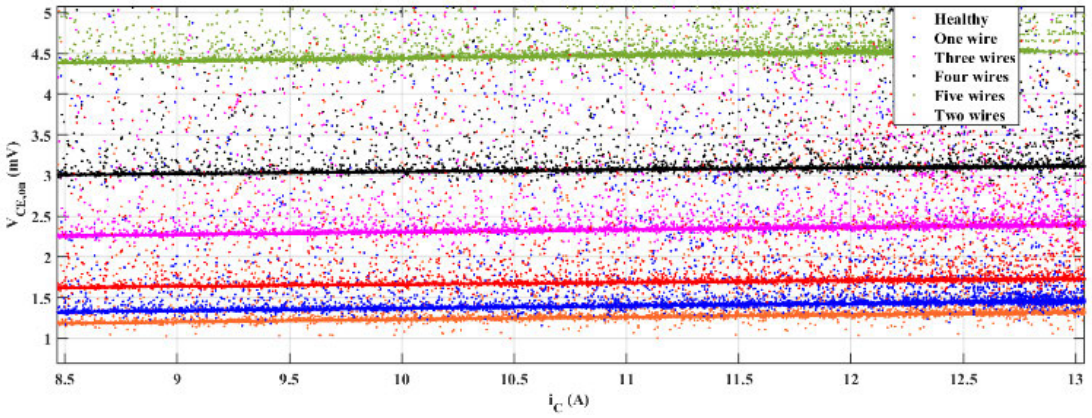


Figure 5.36: $V_{CE,on}$ *versus* i_c *in different level of healthy status*

5.8 Summary

Unpredictable nature of wind speed causes stress, degradation and subsequent reduction in lifetime of IGBTs used in a WT converter. Healthy monitoring of the IGBT can reduce downtime of the WT converter. In this chapter, two separates IGBT electrical parameters are used to estimate junction temperature (switching times-(5.46)) and to detect BWLO ($V_{CE,on}$). Collector emitter on-state voltage

shows a positive sensitivity to the progress of the BWLO. With progress of BWLO, the voltage increases from its value in a healthy state. The voltage has linear relationship to the collector current and junction temperature. Therefore, to use this voltage as a failure detector, the temperature and current should be simultaneously measured. Switching off time shows a negligible sensitivity to the progress of BWLO, which makes this parameter as a good choice of estimating junction temperature. In chapter 6, SF is detected by $V_{CE,on}$. A thermal electrical modelling of the IGBT conducted to study the variations of $V_{CE,on}$ to the progress of BWLO and SF in order to validate trend variations of $V_{CE,on}$ according to experiment results represented in this chapter.

5.9 References

[1] Q.Kong, M. Du, Z.Ouyang , K. Wei and G.Hurley, "A Method to Monitor IGBT Module Bond Wire Failure Using On-State Voltage Separation Strategy", journal energies, May 2019.

[2] Y.-S. Kim and S.-K. Sul, "On-line estimation of IGBT junction temperature using on-state voltage drop," in Proceedings of the 1998 IEEE Industry Applications Conference. Part 1 (of 3), October 12, 1998 - October 15, 1998, St.Louis, MO, USA, 1998, pp. 853-859.

[3] M. M. R. Ahmed and G. A. Putrus, "A method for predicting IGBT junction temperature under transient condition," in Industrial Electronics, 2008. IECON2008. 34th Annual Conference of IEEE, 2008, pp. 454-459.

[4] T. Bruckner and S. Bernet, "Estimation and Measurement of Junction Temperatures in a Three-Level Voltage Source Converter," Power Electronics, IEEE Transactions on, vol. 22, pp. 3-12, 2007.

[5] High Common-Mode Voltage Difference Amplifier AD629 Datasheet. In 2018, available: https://datasheet.octopart.com/AD629BRZ-Analog-Devices-datasheet-9629089.pdf [6] B. Ji, V. Pickert, and B. Zahawi, "In-situ Measurement of the Bond Wire Lift-off in IGBT Power Modules," presented at the Intelligent Motion and Power Quality(PCIM) Europe, Nuremberg, Germany, 2011.

[7] U.Scheuermann and R.Schmidt, "Investigations on the VCE(T)-Method to Determine the Junction Temperature by Using the Chip Itself as Sensor," presented at the Intelligent Motion and Power Quality (PCIM) Germany, 2009.

[8] S. Hartmann, M. Bayer, D. Schneider, and L. Feller, "Observation of chip solder degradation by electrical measurements during power cycling," in Integrated Power Electronics Systems (CIPS), 2010 6th International Conference on, 2010, pp. 1-6.

[9] D. Bergogne, B. Allard, and H. Morel, "An estimation method of the channel temperature of power MOS devices," in Power Electronics Specialists Conference, 2000. PESC 00. 2000 IEEE 31st Annual, 2000, pp. 1594-1599 vol.3.

[10] R. Bonyadi, “Reliability Assessment and Modelling of Power Electronic Devices for Automotive Application and Design”2016.

[11] J. Á.O. González, “Electrothermal Characterisation of Silicon and Silicon Carbide Power Devices for Condition Monitoring”, PhD thesis, Jul 2017.

[12] P. Sun, et al, “Online junction temperature extraction with turn-off delay time for high power IGBTs”, IEEE energy conversion congress and exposition (ECCE), 2014.

[13] On-line available in 2018 at https://www.infineon.com/dgdl/Infineon-1EDN7550B-DS-v02_00-EN.pdf?fileId=5546d46262b31d2e01635d9799ef264f

[14] F. F. Mazda, “Power electronics handbook”, Elsevier. pp. 45-89, 1997.

[15] K. Sheng, B.W. Williams, and S. J. Finney, “A review of IGBT models”, IEEE Trans. Power Electron., vol. 15, no. 6, pp. 1250-1266, 2000.

[16] Available in 2012 at https://www.infineon.com/dgdl/Infineon-IGBT_Characteristics-AN-v01_00-EN.pdf?fileId=5546d462533600a40153559f8d921224

[17] K. Ma, M. Liserre, F. Blaabjerg and T. Kerekes, “Thermal loading and lifetime estimation for power device considering mission profiles in wind power converter”, IEEE Trans. Power Electron., vol. 30, no. 2, pp. 590-602, 2015.

[18] A.Singh, “Online Condition Monitoring of Insulated Gate Bipolar Transistor (IGBT)” MSC thesis, 2016.

[19] J.Hu,“Finite Element Electrothermal Modelling and Characterization of Single and Parallel Connected Power Devices” , PhD thesis, 2016.

[20] Syed H. Ali, “Investigation of Collector Emitter Voltage Characteristics in Thermally Stressed Discrete IGBT Devices”, IEEE Energy Conversion Congress and Exposition (ECCE), 2017.

[21] D.W. Brown, “Turn-Off Time as an Early Indicator of Insulated Gate Bipolar Transistor Latch-up”, IEEE Trans on power electro, Vol. 27, (2), FEB 2012.

[22] V. G, L. FL, R. M, H. A, and W. B, “Intelligent fault diagnosis and prognosis for engineering systems”, 1st ed ed. Hoboken (NJ): John Wiley & Sons, Inc., 2006.

[23] M.Quraan, “Modular multilevel converter with embedded battery cells for traction drives” PhD thesis, 2016.

Chapter 6: Experiment results II: Detection of solder fatigue

6.1 Introduction

The previous chapter described experiments with BWLO. In this chapter, another common failure mechanism, namely SF, is discussed. SF is deterioration of the solder joint between the silicon chip die and the substrate layer, typically caused by thermal cycling of the solder layer and its neighbours. This chapter first describes the use of modelling and simulation to estimate the thermal behaviour across the layers of an IGBT. A thermal network based on a Cauer model represents the heat flow from losses in the chips through the IGBT layers and finally out through the heatsink. A PLECS/MATLAB model is used for thermo-electrical simulation purposes to demonstrate the thermal behaviour of an IGBT. The model is partially validated by comparing the rising temperature of a real IGBT with a heatsink in a lab-based converter to that predicted by the simulation.

As it is difficult to introduce a known amount of SF into an IGBT, the effect of SF degradation is emulated by the use of either thermal grease or one of two thermal pads inserted between the device baseplate and its heatsink, increasing the thermal resistance between the semiconductor junctions and the heatsink. Variation of $R_{th,j-C}$ for different levels of SF is then possible. The effect of SF was investigated by considering the temperature difference between baseplate and junction terminal for different levels of power loss. The thermal model was tuned and validated by applying the same power loss to the model based on the physical IGBT. Subsequently, the sensitivity of the collector-emitter on-state voltage, used as a failure detector, to the progress of both SF and BWLO have been studied and compared with experimental results.

6.2 Thermal modelling of the IGBT

Both Foster and Cauer thermal networks are widely used to model the thermal behaviour of IGBTs (and other devices). The Cauer model is more suited to represent the layered structure of the IGBT but an equivalent Foster model is equally possible. Both types of model are briefly discussed below, a fuller discussion can be found in [1].

6.2.1 Foster model

The Foster model is based on the assumption that the IGBT is a small cube with thermally isolated walls that is attached to an ideal heatsink. A defined power (heat source) is applied at the top surface to emulate the heat source of the junction, assumed to be uniformly distributed over the surface of the junction layer. A simple thermal-model of a one-stage $R_{th} - C_{th}$ network is shown in Figure 6.1. This consists of a thermal resistance (R_{th}) and thermal capacitance (C_{th}) connected in parallel. In analogy with electrical circuit modelling, heat flow is like current and temperature difference is like potential difference (voltage) between two points. The ambient temperature is the ground potential. The initial junction temperature can be set equal to the ambient temperature, the capacitance initially has no 'voltage' across it. Other initial conditions are similarly possible.

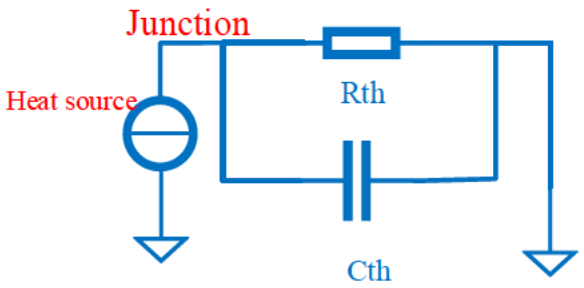


Figure 6.1: Foster model

If a heat source (power input, P_H) is applied to this model, the T_j will rise from initial temperature T_0 as equation (6.1).

$$T(t) = T_0 + P_H \times R_{th}\left(1 - e^{\left(-\frac{t}{\tau}\right)}\right), \quad \tau = R_{th} \times C_{th} \tag{6.1}$$

A Foster RC thermal network is often given in manufacture datasheets due to its simplicity in determining the thermal parameters of the equivalent circuit, but also for analytical calculation of temperature curves. The Foster network is a purely mathematical model with limited linkage to the physical structure of the IGBT. As such, this model structure is unsuitable for assessing the temperatures of different IGBT layers. As the temperature of different layers is important for consideration of SF, a Cauer model is preferred.

6.2.2 Cauer model

A Cauer network has a close relationship to the layers of real IGBT, allowing the internal temperature variations of each physical layer to be examined [2]. An example of one stage of a Cauer thermal network is shown in Figure 6.2.

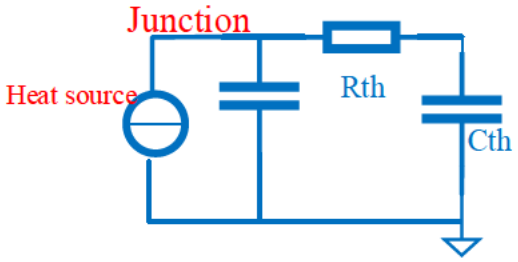


Figure 6.2: Simple Cauer thermal network

The material and geometry position of each layer can be modelled by R_{th} and C_{th} in order to accurately describe the heat conduction mechanisms. The thermal resistors and thermal capacitors of each layers are calculated from the following equations (6.2-6.4).

$$R_{th} = \frac{d}{A \times k_{th}} \tag{6.2}$$

$$C_{th} = v \times \rho \times C_P \tag{6.3}$$

$$\tau = R_{th} \times C_{th} \tag{6.4}$$

where d is layer thickness (m), A is the effective cross-sectional area (m^2) and v is the effective volume (m^3), k_{th} is the thermal conductivity ($W.m^{-1}.K^{-1}$) and C_P is the specific heat capacity (J/kg. K). ρ is density (kg/m^3).

The thermal resistance is smaller for a thinner layer, or a larger effective cross-sectional surface area. The thermal capacitance depends on the volume, density and thermal capacity of the material. The time constant relates to how long it takes for a given heat passing through the layer to establish a temperature difference across the layer. Small layers have small thermal capacitances and small thermal resistances, so their time constants are rather small, of the order of milliseconds. In contrast, a heatsink typically has a large thermal capacitance and being thicker has a higher thermal resistance so its time constant is typically of the order of minutes.

A chain of $R_{th} - C_{th}$ elements forms a Cauer model with each layer having its own thermal resistance and capacitance with a good correlation between the model and the real physical temperatures of the individual layers. Therefore, the 1-D Cauer model using thermal resistance and thermal capacitance of each layer is used as the structure of the thermal model of the IGBT henceforth.

Table 6.1 lists the material properties and dimension of each layer of the IGBT used in lab experiments.

Table 6.1: IGBT layer dimensional properties

	Material layer	Length (mm)	Width (mm)	Thickness (mm)	Effective area (mm^2)	Effective volume (mm^3))
1	Chip IGBT	6.5278	6.604	0.381	43.083	16.414
2	Chip diode	6.5278	4.3942	0.381	43.083	16.414
3	Solder (Sn96.5Ag3.5)	6.5278	6.604	0.1	43.92	4.392
4	Copper	38	23	0.3	49.39	14.816
5	AL_2O_3	38	23	0.25	57.42	14.355
6	Copper	38	23	0.3	66.06	19.818
7	Solder (Sn96.5Ag3.5)	23	38	0.1	72.72	7.272
8	Baseplate	31.8	63.5	2.5	123.82	309.569
9	Thermal grease	31.8	63.5	0.1	188.45	18.845
10	Gap pad1	31.8	63.5	1	200.80	200.8
10	Gap pad2	31.8	63.5	2	214.5	429.06
11	Heatsink	65.84	31.30	10.21×2	1172.91	23950.85

6.2.3 Heat spreading for each layer

In an IGBT module, heat is generated at the junction (top) layer on a relatively small silicon chip and passes through a layered structure towards the baseplate. Heat spreads out laterally from centre of the chip as it passes through the layers. Although the heat moves laterally as well as vertically, the three-dimensional heat flow can be approximated by a 2D-dimension model. This then links to the Cauer model with equivalent thermal resistances and capacitances [4]. The fixed angle heat spreading assumes the heat path having a shape as such the pyramid structure shown in Figure 6.3.

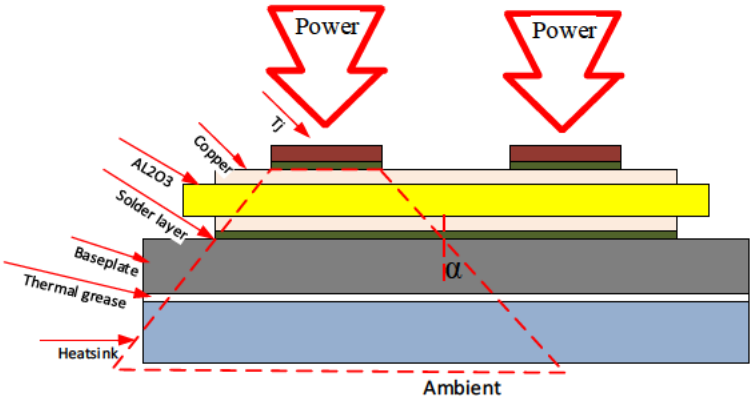


Figure 6.3: A pyramid heat flow structure of the IGBT

The silicon chip is the heat source for an IGBT. The angle α is defined between each side-wall of the pyramid and vertical axis (α is shown between two layers solder and the baseplate). The 'one-dimensional' thermal resistance is defined by using the mean cross-sectional area along the heat path for each layer. The total thermal impedance is then considered as many slices in series. Thermal resistances and capacitances are calculated and presented in Table 6.2 for the lab IGBT.

Table 6.2: IGBT layer thermal characteristics

	Material layer	Thermal conductivity ($W\ m^{-1}.K^{-1}$)	Specific heat capacity (J/kg. K)	Density (kg/m^3)	Thermal resistance (K/W)	Thermal capacitance
1	Chip IGBT	163	735	2330	0.054	0.029
2	Chip Diode	163	735	2330	0.054	0.029
3	Solder (Sn96.5Ag3.5)	50	150	9000	0.045	0.006
4	Copper	400	385	8960	0.0152	0.051
5	AL_2O_3	27	900	3900	0.1612	0.1157
6	Copper	400	385	8960	0.01135	0.068
7	Solder (Sn96.5Ag3.5)	50	150	9000	0.0275	0.0098
8	Baseplate	27	900	3900	0.13	1.087
9	Thermal grease	0.71	1000	2100	0.2	0.0396
10	Gap pad 1	3	1000	3200	1.66	0.642
	Gap pad 2	5	900	2700	3.11	1.373
11	Heatsink	160	900	2700	0.11	58.2

Each layer in the Cauer thermal network can be modelled as a 'T' model ($R-C-R$) or 'L' model ($R-C$). The 'T' model is used here, splitting the thermal resistance of the IGBT layer into two equal resistances while the capacitance is connected from the centre to the ground, as shown in Figure 6.4.

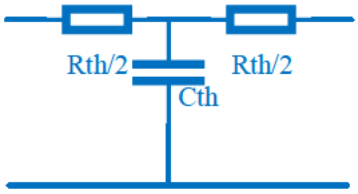


Figure 6.4: RCR model

This approach essentially defines the temperature at the middle of each layer. The first layer (silicon) and last layer (heatsink) are exceptions. Regarding the silicon layer, a step change input power to the RCR model would cause a step change in the temperature variations while in practice the silicon temperature does not go through the step change. Regarding the last layer, the thermal time constant of the heatsink is much higher than those elsewhere in the IGBT device. As such, the thermal temperature in this layer does not go through a step change. Thus, these two layers are modelled by a simple RC model as shown in Figure 6.5 [2].

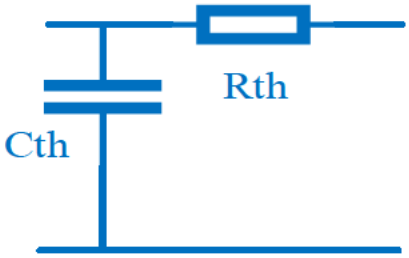


Figure 6.5: RC model

The thermal capacitance of the heatsink is obtained according to the time constant of the physical heatsink. Figure 6.6 shows the temperature rise of heatsink as measured in a lab-based experiment in a physical system. Heat was generated in the form of losses at the junction of one IGBT pair and this causes the temperature of the IGBT and heatsink to rise. The time constant is the time taken for the temperature to rise (above the initial temperature) by 63% of the steady-state temperature rise and is calculated by (6.6). The time constant of the heatsink is 560 s and, therefore, the thermal capacitance is about 314 J/°C.

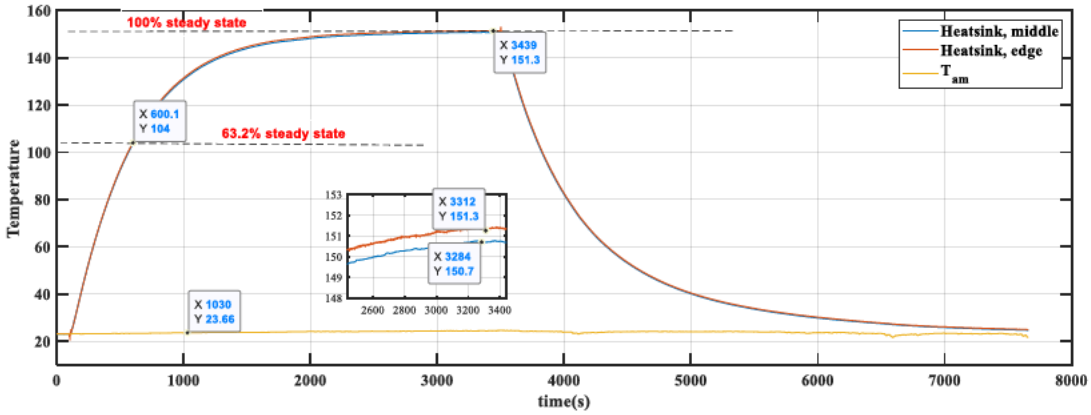


Figure 6.6: Time constant of heatsink

A 9-layer Cauer type model of the thermal network of the IGBT used in the lab is shown in Figure 6.7. As discussed previously, the IGBT half-bridge module used has two parallel chips for the high side and two for the low side. These two chips are on separate silicon chips but the solder layer for each die and the rest of layers are common to all chips. As such, the extra chip (parallel chip) and solder joint are parallel with the rest of the model in order to emulate the heat effects of two parallel IGBT. Both parallel chips have a freewheeling diode.

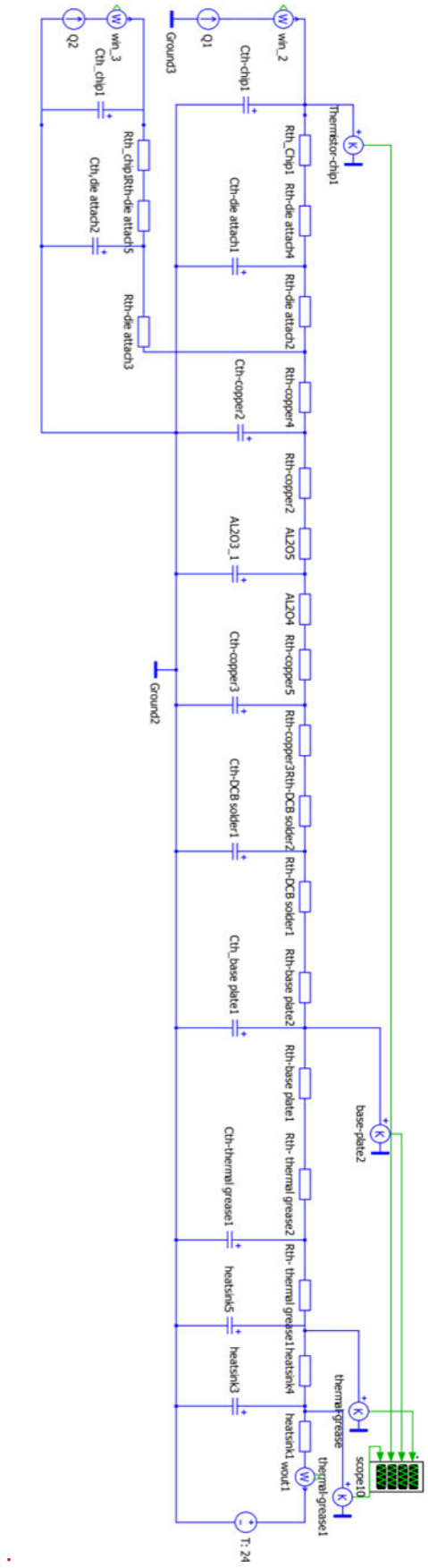


Figure 6.7: The thermal network of the IGBT

The temperature profiles of each layer (from the model) are shown in Figure 6.8 for an applied heat power of 28 W. The steady-state temperature difference between the junction of the device and the middle of the heatsink interface is 14°C in the model. The temperature difference between two parallel chips is less than 0.1°C because of symmetry in the early part of the model. The applied power loss of 28 W corresponds to the difference between the electrical input and output powers as measured in the lab-based setup for one experiment.

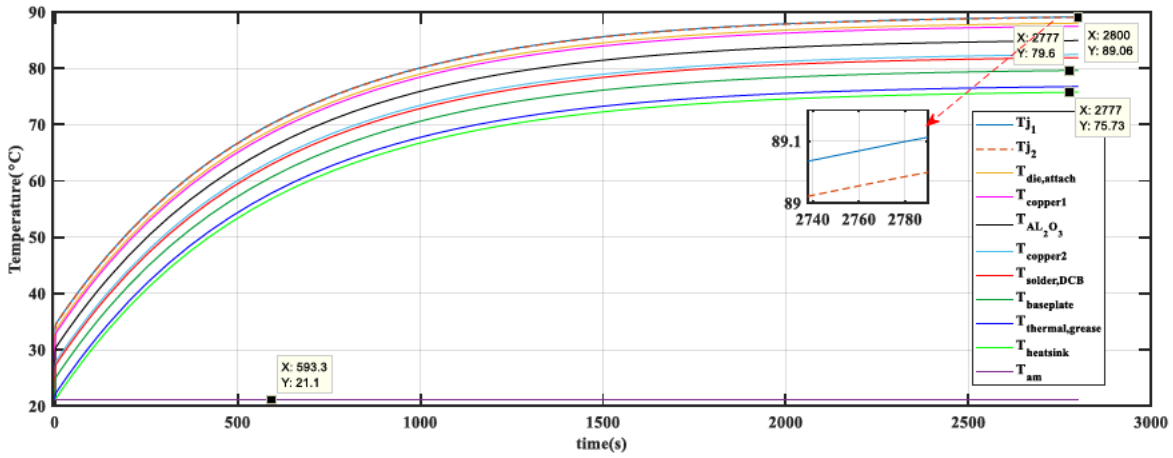


Figure 6.8: Temperature behaviour in IGBT layers

A very rapid initial temperature rise at the junction and other upper layers is caused by their short time constants (compared to that of the heatsink).

6.3 Temperature measurement/estimation of the IGBT

Temperatures $T_{baseplate}$ and $T_{Heatsink}$ are measured by thermocouples touching the baseplate of the IGBT, located in grooves in the heatsink. The two different metals in the thermocouple legs generate a potential difference. The temperature difference between hot and cold junctions can be calculated by measuring the voltage difference at the cold junction, as shown in Figure 6.9.

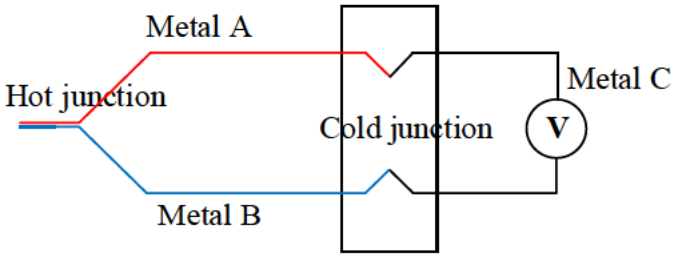


Figure 6.9: Thermocouple Principle

To measure a single temperature, one junction, normally the cold junction is maintained at a known constant reference temperature, or in practice compensated by electronic circuits inside the

measurement device. In this work, K-type thermocouples are used to measure T_C. This type of thermocouple is the most common general purpose thermocouple with a sensitivity of approximately 41 µV/K. A K-type thermocouple is able to sense temperatures between -200° C and +1350° C, which covers the designed T_C range. Thermocouples are also attached to the baseplate by inserting them inside slots, shown in Figure 6.10a, to read and track T_C. Two thermocouples are inserted inside the heatsink to measure $T_{Heatsink}$, shown in Figure 6.10b. Temperature $T_{baseplate}$ is measured by averaging the temperature at three different spots. The baseplate temperature is 79.6°C in the thermal model and is measured by inserting thermocouples in drilled locations on the IGBT's baseplate, which is 79.81°C, Figure 6.11.

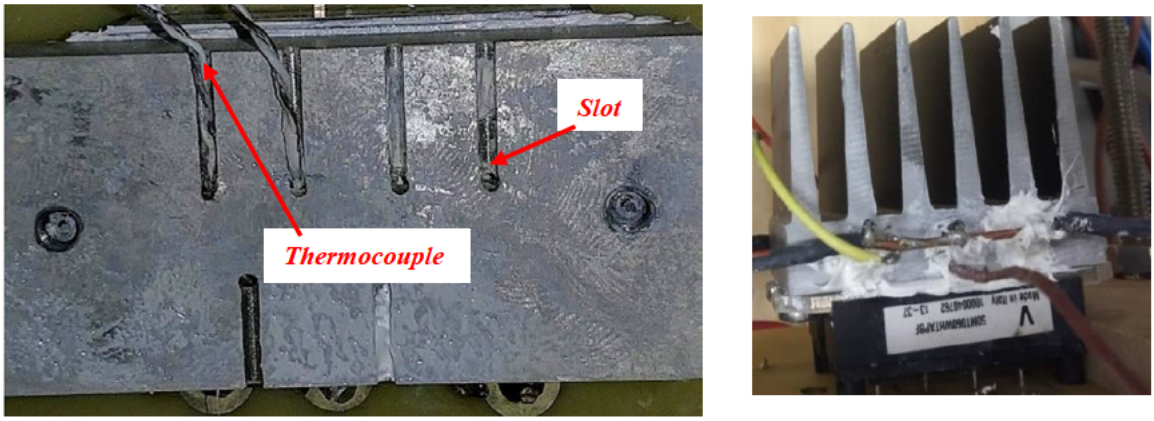


Figure 6.10: Baseplate thermocouple arrangement (left) Heatsink thermocouples (right)

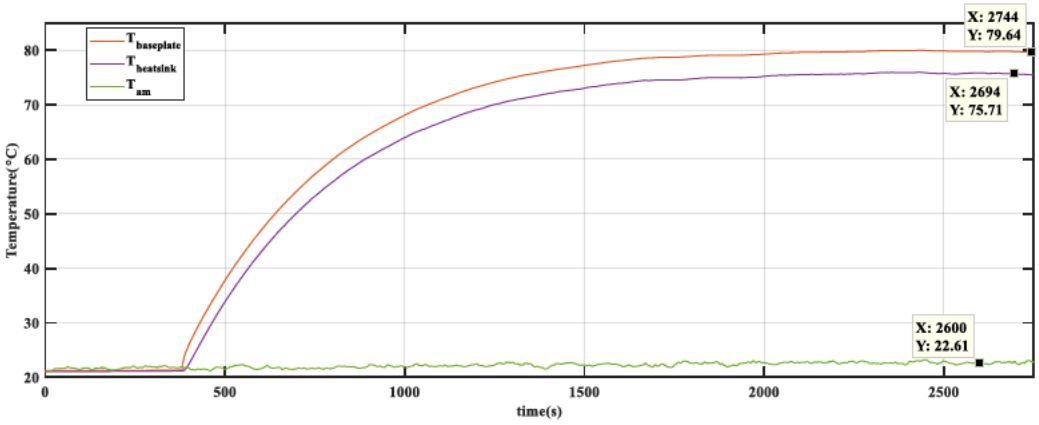


Figure 6.11: Temperature of heatsink and baseplate

The idea was to place the thermocouples underneath each IGBT chip. Baseplate temperature ($T_{baseplate}$) is calibrated by adjusting to the room temperature when the equipment has been off, for example overnight. The substrate layer temperature is measured by an NTC (negative temperature coefficient) sensor inside the module. The NTC thermistor is a resistor with a negative temperature

coefficient, so the resistance decreases with increasing temperature. The NTC is attached on copper inside the module by the manufacturer and the two terminals are available externally, Figure 6.12.

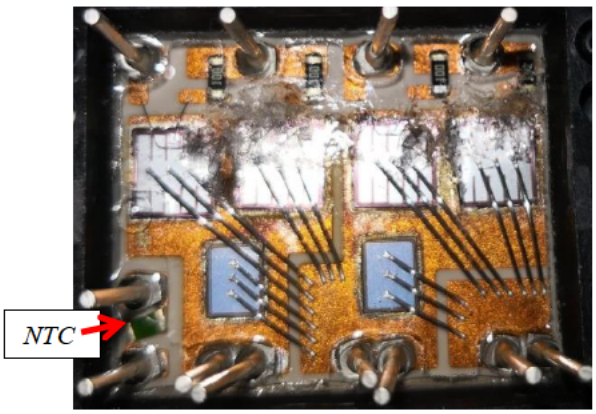


Figure 6.12: NTC inside module

The NTC terminal is connected to a microcontroller through a non-inverting amplifier, MCP6002 (manufactured by microchip, gain bandwidth product: 1 MHz). The configuration of the NTC measurement circuit is shown in Figure 6.13.

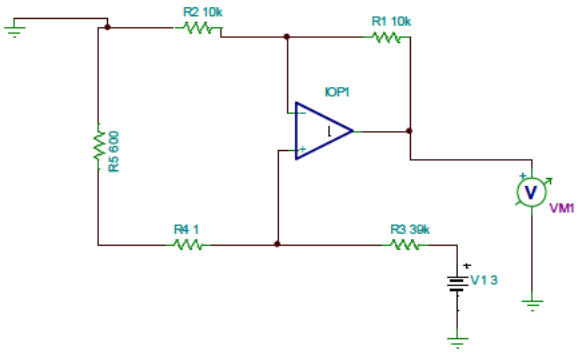


Figure 6.13: Configuration of amplifier connected to the NTC terminals

The temperature measured and monitored through a microcontroller ADC that connects to the NTC terminals, shown in Figure 6.14. Substrate temperature is obtained based on a fitting equation (6.5). The equation gives the NTC temperature (T_{DCB}) against resistance is given in kΩ. Quantity x in this equation is the ADC value.

$$T_{DCB} = -0.173\left(\frac{(x-25130)}{4910}\right)^5 - 1.1043\left(\frac{(x-25130)}{4910}\right)^4 - 2.605\left(\frac{(x-25130)}{4910}\right)^3 - 5.107\left(\frac{(x-25130)}{4910}\right)^2 - 20.42\left(\frac{(x-25130)}{4910}\right) + 56.02 \quad (6.5)$$

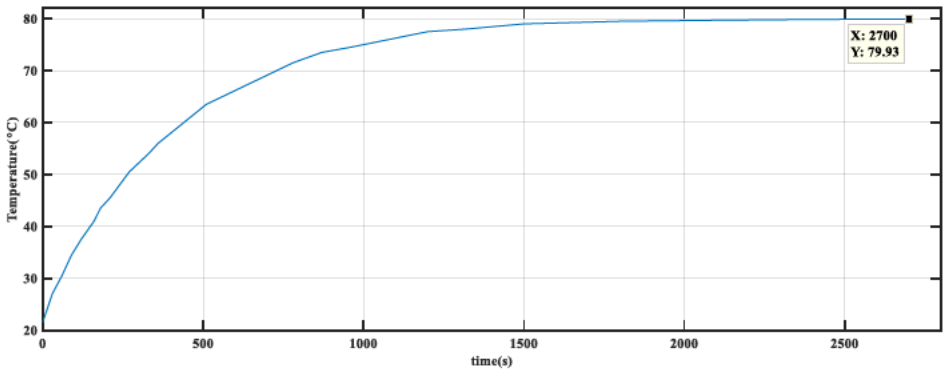


Figure 6.14: Output of NTC temperature

T_j is estimated as described in chapter 5 through monitoring t_{off} and i_c. Three required electrical parameters, V_{CE}, V_{GE} and i_C are measured by a Tektronix oscilloscope for different condition to build a 3D look up table. One example is shown in Figure 6.15. The DC-Link voltage is 20 V and the ambient temperature about 23°C. These parameters are sampled within the operation of the built converter.

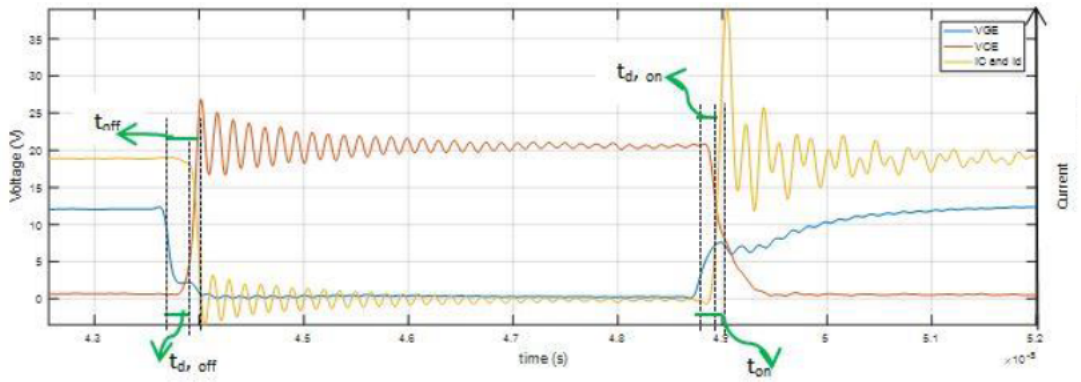


Figure 6.15: Switching parameters of the IGBT under test

6.4 Power loss calculation

In power electronic converters the IGBTs and diodes experience self-heating as electrical current flowing through the devices. During IGBT (and diode) operation, static power losses (conduction power losses) and transient power losses (switching power losses) contribute to heat generation inside the devices. The resulting cyclic heating contributes to a reduction in the expected lifetime of the IGBT.

The average power loss in one cycle (period T) for a device are given by

$$P_{loss} = \frac{1}{T}\int_{t_0}^{t_0+T} v \times i \, dt$$

where v is the voltage across the device and i is the current through the device. The instantaneous power loss is $v \times i$. From lab measurements of voltage and current it is possible to evaluate this value on a

point by point basis and find the loss using the integral above. However, for the purposes of modelling the losses are divided into two parts: the conduction losses and the switching losses.

During modelling it is assumed that the voltage across the device and the current through the device during the on time are constant. The voltage across the device is the on-state voltage drop, the current through the device is the operating current. The conduction losses are then given by the product of the constant voltage with the constant current. As the device is only conducting when it is on, the losses in one cycle only happen some proportion of the time, given by the duty cycle D. The average conduction losses of an IGBT, with duty cycle D are given by (6.6) [3].

$$P_{Con,ave} = V_{CE,on} \times i_C \times D \tag{6.6}$$

For the purposes of modelling, the switching losses are the sum of the turn-on and turn-off switching losses for each IGBT and diode. Generally, the switching loss is described as E_{on}, the energy lost during each switching-on event, and E_{off}, the energy lost during each switching-off event. The power lost through switching losses is the total on and off time energy in one second which is given by equation (6.7)

$$P_{sw,av} = f_s E_{on} + f_s E_{off} = f_s(E_{on} + E_{off}) \tag{6.7}$$

where f_s is the switching frequency.

The input characteristics of the IGBT are the same as a MOSFET, and hence the capacitors C_{GC} and C_{GE} should be taken into account when transient or switching power losses are considered. In order to explain switching losses and reason of its presence assume IGBT is in the off state. In this case the load current is only flowing through the freewheeling diode and V_{CE} is equal to the DC-link voltage. A voltage is then applied to the gate to turn on the IGBT. This voltage cannot turn the IGBT on instantaneously. Voltage V_{GE} increases exponentially with a time constant equal to R_G (C_{GC} +C_{GE}). Once the voltage reaches $V_{GE,th}$, the collector current i_c starts to flow (this small period of delay is defined as the turn on switching delay). Voltage V_{GE} will continue to increase, leading to an increase in collector current. However, the diode is forward biased although with less current flowing in it (i_d =i_L-i_C). The diode stored charge has to be removed in this stage, when IGBT is fully turned on, i_C reaches load current (i_L) and diode goes into recovery mode. Voltage V_{CE} shows a small voltage as the on-state voltage. Switching turn off loss ($P_{sw,off}$) occurs when no current flows to diode (reverse blocking state).

Once again, when the command gate voltage becomes zero, the IGBT cannot be turned off immediately as it takes time to discharge the gate capacitors through the gate resistors. Diode starts conducting current while both V_{GE} and i_c decreases. This process continues until V_{GE} reaches $V_{GE,th}$ and collector

current becomes zero. This small period of delay is defined as $t_{d,off}$. From when the V_{GE} becomes zero to i_c become zero is called t_{off}. The switching losses for a diode is negligible when it is turned on. Switching loss energy is generated during reverse recovery of the diode. The recovery phenomenon of the diode will limit the switching speed, the current and voltage rate of the IGBT. When the diode is turned off, excess charge is removed from the P-N junction (t_1). The total excess carrier concentration in the junction is reduced to zero and during this stage, the voltage across the diode increases and the depletion region gets wider until it reaches its maximum (t_2). The recovery energy is expressed through equation (6.6). By applying equation (6.8), the average conduction and switching power losses are obtained in one period of switching time.

$$P_{av} = V_{ce,sat} I_l \, D + f_s E_{on} + f_s E_{off} \tag{6.8}$$

For the calculation of the switching losses, a linear approximation of the IGBT switching process has been assumed. The switching losses are computed using the switching energies. The turn-on and turn-off switching energy losses, $E_{sw,on}$ and $E_{sw,off}$, are given by equations (6.9) and (6.10) [5]. Conduction power loss is calculated by equation (6.11). Figure 6.16 shows conduction and power losses of IGBT under test that are obtained by multiplication of $V_{CE,on}$ and i_C.

$$E_{sw,on} = \int_a^b V_{ce} I_c dt \tag{6.9}$$

$$E_{sw,off} = \int_c^d V_{ce} I_c dt \tag{6.10}$$

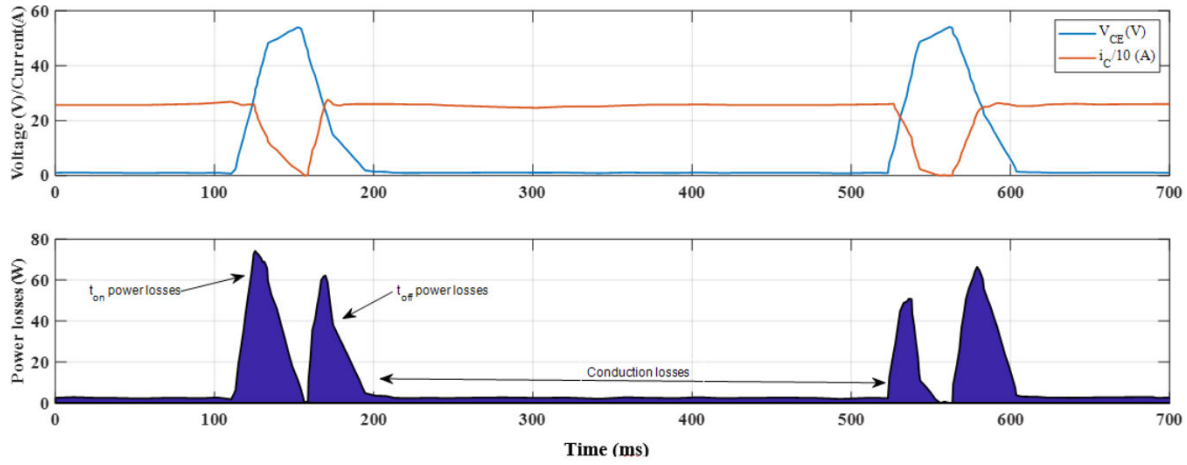


Figure 6.16: Power losses of the IGBT under test at ambient temperature

The division between conduction loss and switching loss is not always clear, but as long as all the loss is accounted for, it is not important. It is apparent that on-state losses can be simply determined since the IGBT operates in a static state. However, it is difficult to obtain the switching loss as the transient times are only of the order of hundreds of nanoseconds. The precise measurement of the voltage and current profile require a sophisticated measuring systems to allow the product of voltage across the device and current through it to be multiplied instant by instant. In practice, a precise health condition

monitoring system based on such measurements is not cost-effective. Transient power losses are commonly obtained through the use of a 3D look-up table [9]. The look-up table data is provided by measurement of different parameters: i_C, DC-link voltage and T_j in the laboratory. Subsequently, switching losses can be directly determined by measuring the relevant parameters with much lower computational costs.

6.4.1 *Steady state thermal analysis*

The purpose of discussion about $R_{th,j-c}$ is that this will be used as the main criterion for thermal path degradation to be utilised subsequently. Based on thermal laws, $R_{th,j-c}$ can be calculated as the difference in temperature between two close thermal surfaces in (6.12).

$$R_{th,j-c} = \frac{T_j - T_{ref}}{P_{loss}} \tag{6.12}$$

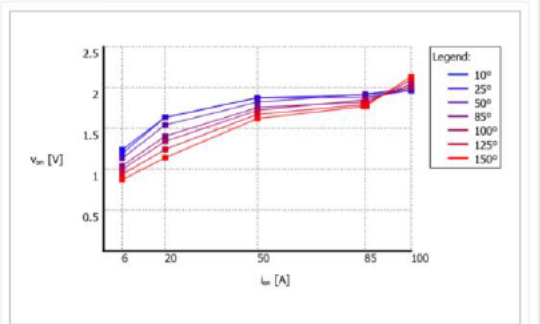
where T_j and T_{ref} are the reference temperatures and P_{loss} is the amount of heat flow under steady-state conditions. In this work, $T_{baseplate}$ is considered as a reference temperature. $T_{base,plate}$ is the baseplate temperature on the bottom side of the module, measured directly beneath the chip via a drill hole in the heatsink. The thermal resistance is normally given in the datasheets with some safety margins and can be only used to calculate steady state T_j.

6.4.2 Transient thermal analysis

In general, the thermal impedance (Z_{th}) describes the way in which heat propagates from the junction through the layers inside the IGBT to the baseplate surface, finally to be dissipated through the heatsink to the environment. Thermal impedance (Z_{th}) is described in (6.13).

$$Z_{th,j-c} = \frac{T_j - T_{ref}}{P} \tag{6.13}$$

The table can be extracted from the datasheet, switching and forward characteristic experiments, physics-based device modelling [7-9]. In this work, switching and forward characteristic experiment methods are used to obtain this model. Power loss has been calculated based on the circuit below by applying a known power source and knowing the base temperature. The electro-thermal network of the IGBT was developed based on conduction and switching losses. A 2D lookup table and 3D lookup table for conduction loss and switching loss were developed. The 2D table is based on T_j, conduction loss, $V_{CE,on}$ and i_c. The 3D lookup is based on T_j, $V_{CE,off}$ and i_c, shown in Figure 6.17.



	6 A	20 A	50 A	85 A	100 A
10°	1.238 V	1.634 V	1.873 V	1.912 V	1.96 V
25°	1.191 V	1.634 V	1.872 V	1.88 V	1.964 V
50°	1.134 V	1.54 V	1.82 V	1.918 V	1.99 V
85°	1.042 V	1.403 V	1.754 V	1.82 V	2.041 V
100°	1 V	1.34 V	1.72 V	1.85 V	2 V
125°	0.938 V	1.242 V	1.672 V	1.79 V	2.09 V
150°	0.873 V	1.141 V	1.62 V	1.77 V	2.13 V

Figure 6.17: The 2D conduction energy loss look-up table

With regard to the 2D look up table developed, conduction loss has been keep more or less constant for a set of junction temperatures T_j by regulating i_c and $V_{CE,on}$. The data is achieved by experimental results is explained in the next subsection.

6.4.3 Power loss in experiment: switching and conduction losses

Initially, power losses are measured using the experimental setup shown in Figure 6.18. A certain power loss was been generated inside the IGBT (by varying the dc supply voltage, the duty cycle and the load. The temperature rise of the substrate, baseplate and heatsink were measured and the junction temperature estimated. The low-side gate terminal is held at zero so that the lower IGBT is held off. Power losses occur in the upper IGBT and the lower parallel diode.

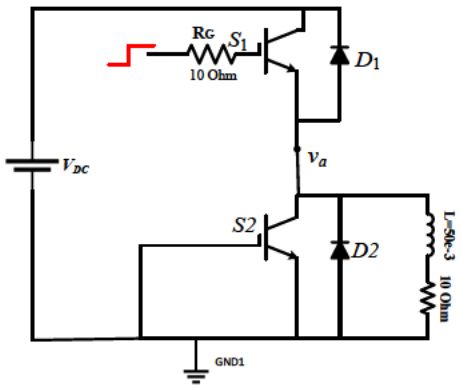


Figure 6.18: Schematic of the test steup for calculation of power losses

This test is run with a constant load to examine the power losses generated by the IGBT itself and not the heat variations that can be generated by variable load current. To build the look up table power loss has been measured for two different DC power supply voltages (24 V and 50 V) and two different

currents (8 and 13 A) and four different temperatures, 25, 50, 100 and 150° C. A (static) electric machine is used as a large inductive load with a small resistance, so the load current remains almost constant. The switching frequency is 10 kHz. Data were collected with a differential probe used to monitor the full range of V_{CE}, right up to $V_{CE,off}$, examples shown in Figure 6.19 and Figure *6.20*. However, the differential voltage probe is not accurate enough to measure the small voltages $V_{CE,on}$, so data were also collected using a unity gain differential amplifier that can withstand a high voltage difference between the input terminals without damage. Using this device, the conduction loss can be found. The device also allows the wide range differential voltage probe to be calibrated for accurate low voltage measurement that is used to calculate switching on and off energy from the cumulative power. The cumulative power is shown in Figure 6.21, based on the cumulative product of voltage with current. The initial steep rise represents E_{on} and the gentler slope represents the conduction loss energy E_{con} while the second steep rise represents E_{off}. Ideally, conduction power loss can be calculated by equation (6.13) and switching loss is calculated by equation (6.14). *D* is the duty cycle and it is the percentage when the IGBT is on (conducting current) [5].

$$P_{cond,loss} = D \times i_C \times V_{CE,on} \tag{6.13}$$

$$P_{sw,loss} = \frac{1}{2} \times i_C \times V_{CE,off} \times (t_{on} + t_{off}) \times f_{sw} \tag{6.14}$$

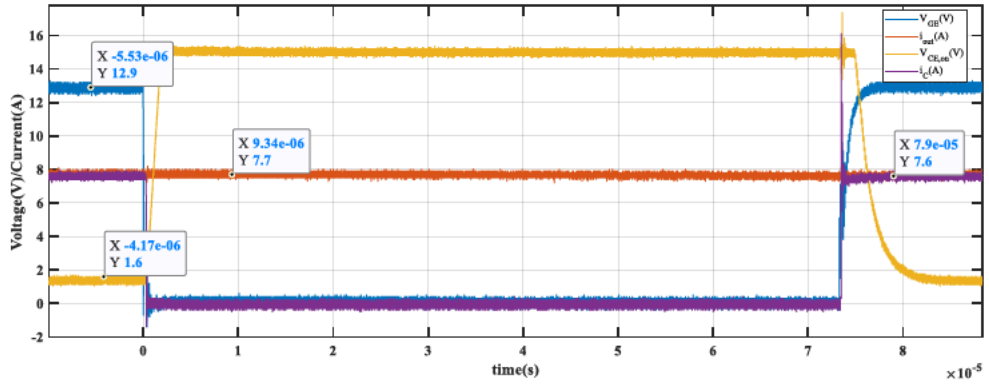


Figure 6.19: Electrical parameters of the IGBT to find conduction loss

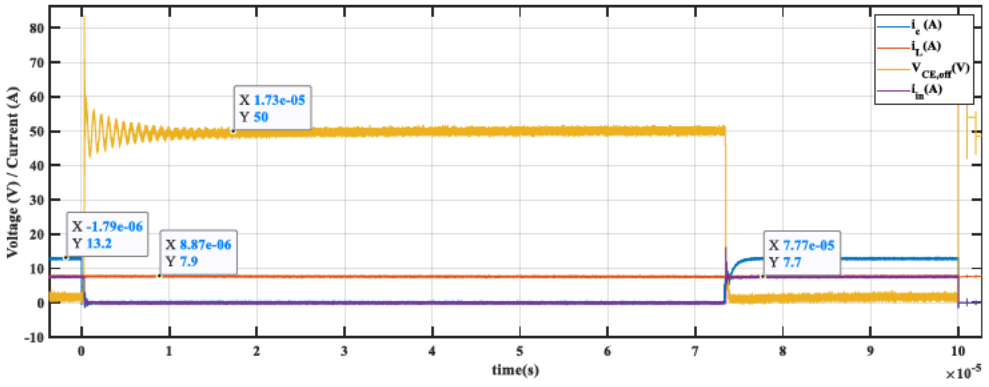


Figure 6.20: Electrical power loss of the IGBT to find switching loss

The duty cycle was set to 53 % and 0.47% of this time was allocated for turning on the freewheeling diode and diode losses. The diode voltage drops to 1.6 V and i_d reached about 8.67 A. The test was run with an initial temperature of 65ºC. The total power losses was 28.4 W. Conduction losses were 4.72 W and switching losses 2 W. $V_{CE,on}$ was 1.62 V and i_C was 8.6 A. The estimated T_j was 89ºC at steady-state using the look up table from chapter 5. The cumulative power and switching on and off energies, are shown in Figure 6.21.

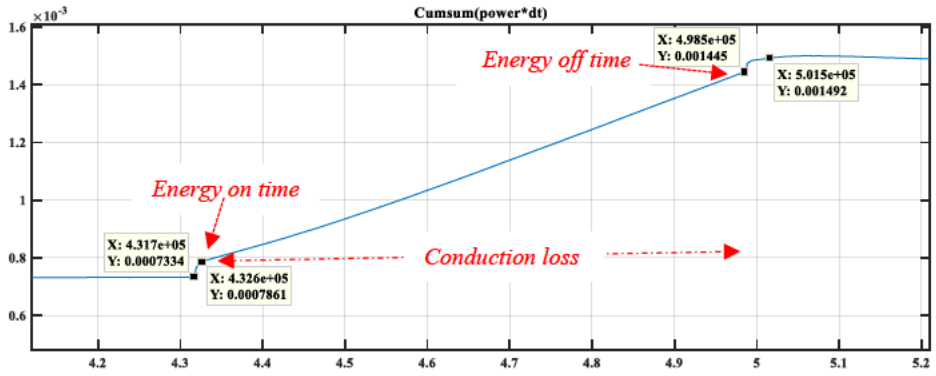


Figure 6.21: Cumulative power loss

To tune the IGBT electrical parameters according to the physical IGBT, the same amount of power was applied to the IGBT modelled in PLECS, as shown in Figure 6.22. Using calibration data from chapter 5, a 2-D look up table was built to calculate the conduction power loss, shown in Figure 6.23. The lookup table agrees with the power loss experiment results using measurement of the conduction loss through the common voltage amplifier and considering i_c and duty cycle. A 3D lookup table was built and attached to the IGBT to calculate switching power loss. Switching energy on and off losses are achieved obtained from two different lookup tables. These look up tables can generate E_{on} and E_{off} according to $V_{CE,off}$, i_c and T_j shown in Figure 6.23. Temperature T_j is calculated in the PLECS model by applying the power losses and observing the results from the thermal network. The temperature behaviour of the thermal model of the IGBT is shown in Figure 6.24. Temperature T_{DCB} is compared in both physical model (via NTC sensor) and thermal model to find out the accuracy of the model. This model is, later on, used to analyse the effect of BWLO and SF on T_j and $V_{CE,on}$.

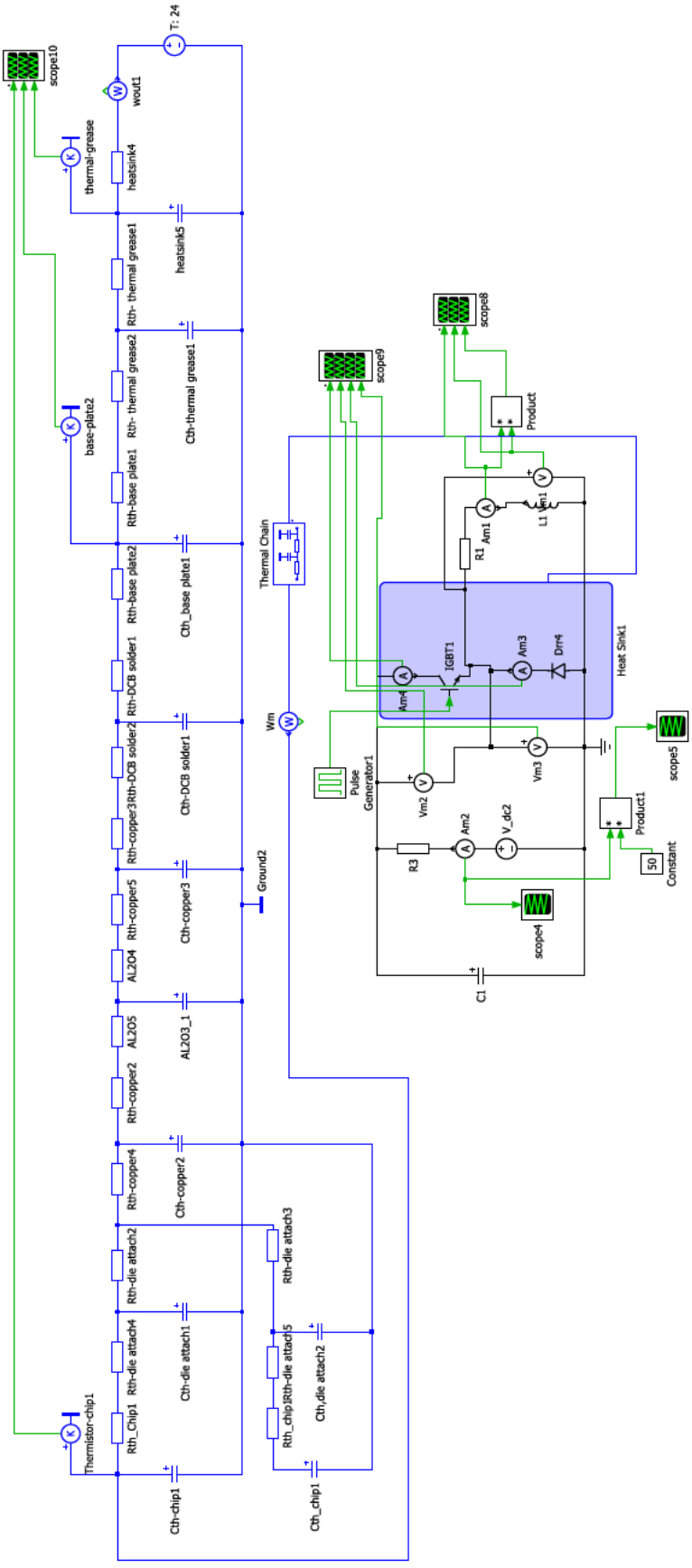


Figure 6.22: Thermo-electric model of IGBT

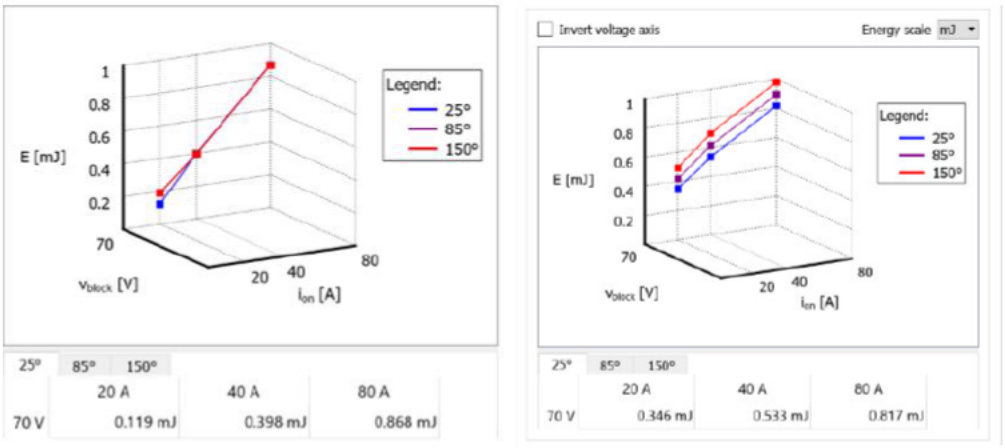


Figure 6.23: Switching loss of the IGBT added to PLECS model
energy loss during turn on(left)-energy loss during turn off (right)

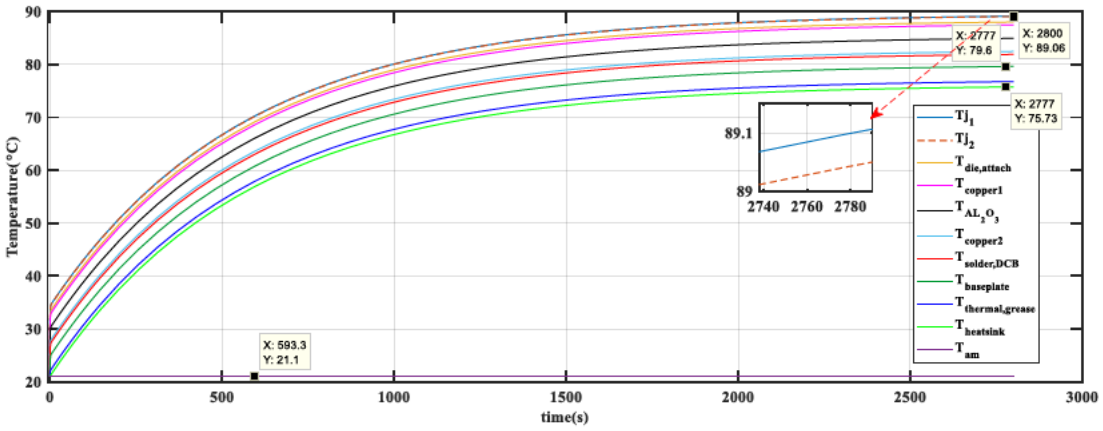


Figure 6.24: Temperature rise in DCB silicon and baseplate layers

6.5 Detection of solder fatigue

The IGBT module undergoes thermal cycling (either by self-heating from power cycling or by changes in the environment). Due to thermal expansion coefficient mismatch (TEC) fatigue cracks that affect the heat dissipation of the IGBT chips. An IGBT encounters thermal cycling frequently during the operation of a WT. Repeated thermal stress and consequent mechanical deformations expand the area of fatigue cracks and cause detachment of part of the baseplate solder joint. SF can reduce the effective area for heat conduction and increase $R_{th,j-C}$, leading to increased T_j [6] and ionize more hot carriers to change the junction capacitances such as C_{GE} [7]. Degradation of the solder layer causes an exponential increase in T_j due to poor heat conduction. Variation of $R_{th,j-C}$ can be used as a failure detector for SF.

In order to obtain $R_{th,j-C}$, two temperatures, T_C and T_j, are measured/estimated for known power losses. Solder degradation affects the thermal distribution inside the IGBT. Solder degradation causes a 20% increase in thermal resistance of the IGBT [8]. In order to study the effect of SF on the proposed failure detectors, the thermal resistance in the substrate layer should be changed. However, this layer is not accessible and hence thermal resistance is changed instead between the baseplate and the heatsink. To emulate SF, $R_{th,j-C}$ between the IGBT baseplate and heatsink is increased by inserting a 'Gap pad' thermal pad [14], Figure 6.25Figure 6.25: Emulating solder fatigue by adding thermal pad. Two different thermal pad with thermal conductivities of 3 and 5 W/m.K and thicknesses of 1 mm and 2 mm were available.

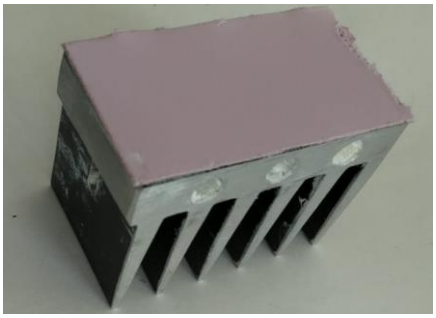


Figure 6.25: Emulating solder fatigue by adding thermal pad

The datasheet for the IGBT gives $R_{th,j-C}$ as 0.38 ºC/W whereas $R_{th,j-C}$ was estimated as 0.445ºC/W for a healthy IGBT (without thermal grease and baseplate) and 0.514 ºC/W considering the baseplate and thermal grease. Detection of SF can be observed by monitoring of $T_j - T_C$ for a known power loss. Various thicknesses of thermal pad (Gap pad @ 3100 [15]) were inserted to increase the total thermal resistance by 10% to 50% to observe the effect of SF on the thermal model and physical experiments. A 20% increase in $R_{th,j-C}$ (i.e 0.59 ºC/W) is generally taken as full SF degradation. The thermal resistance, $R_{th,j-c}$ of the IGBT was increased by 0.54 W/m for 10% of healthy state, 0.57 W/m.K for 15% and 0.74 W/m.K for 50% of SF. The healthy state is assumed when thermal grease with a conductivity of 0.71 W/m.K is used. Figure 6.26 shows the healthy thermal path of the IGBT in top of the figure and unhealthy thermal path (presence of SF) in real work in the middle and unhealthy IGBT module in the lab in bottom. The bottom one shows where SF/ thermal pad has been added to the thermal path of the IGBT under test.

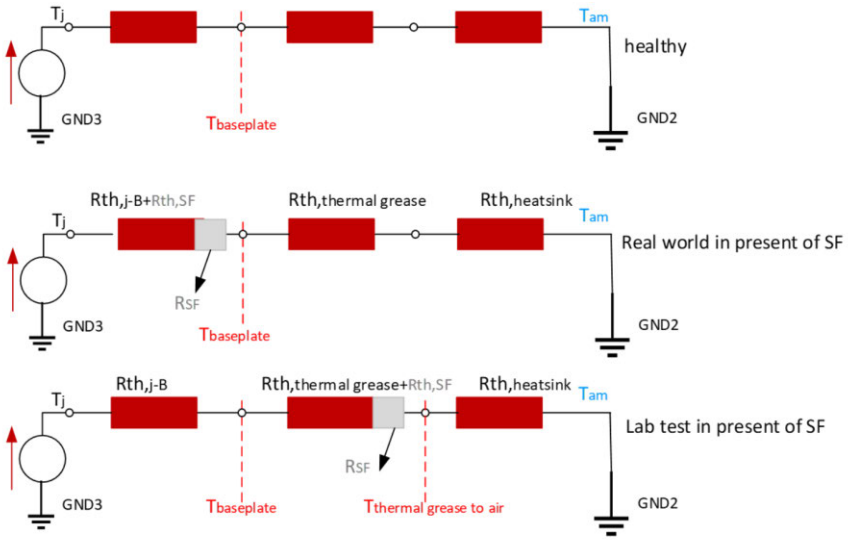


Figure 6.26: Change in thermal path for IGBT in the presence of SF

The thermal conduction path was investigated in different health states through changing $R_{th,j-c}$ in the appropriate layers of the thermal model, described below. The same heat flow was applied for these states and the first (healthy status) was considered as the reference state.

1) A healthy IGBT module using thermal grease
2) An IGBT module excluding heatsink with 50% increase of $R_{th,j-c}$ at DCB solder layer.
3) An IGBT module excluding heatsink with 20% increase of $R_{th,j-c}$ at DCB solder layer.
4) An IGBT module excluding heatsink with 15% increase of $R_{th,j-c}$ at DCB solder layer.
5) An IGBT module excluding heatsink with 10% increase of $R_{th,j-c}$ at DCB solder layer.

The dissipated heat takes a certain amount of time to propagate from the junction terminal through the various layer inside the package to the outside baseplate surface. The heat finally dissipated through the heatsink and to the immediate environment. An of 20% increase in $R_{th,j-c}$ with respect to its initial value is a commonly recognised failure criterion. The thermal conductivity and the heat conduction area were defined and varied using the thickness of the Gap pad. The thermal resistance $R_{th,j-c}$ increases to 0.548 ºC/W and 0.74 ºC/W using two thermal pads (vs-50mt060whtapbf) for 10 % and 50% degradation respectively. In order to determine the $R_{th,j-c}$ over time, T_j , T_{ref} and P_{loss} need to be known. Temperature T_j was been obtained by means of the lookup table in Figure 5.19. The temperature can be measured either during cooling down or heating up of the IGBT. Taking the temperature during the cooling requires heating up the IGBTs to thermal stability. Heating source is normally provided by the current flowing in the IGBT module.

The temperature falls at turn off time when the IGBT has reached thermal stability and is measured with calculation of t_{off}. The temperature measurement of the reference point has been done with three thermocouples and logged by a Pico Logger. The heating technique requires sampling the temperature during the heating of the device again by using a TSEP parameters. This method, however, requires expensive on-line power measurement. The disadvantages of the cooling technique is that, to reach thermal stability, a sufficient effective cooling facility and a long experiment time are required. These conditions are not effective for real applications. The resolution and the accuracy of T_j and T_c measurements are critical in calculating $R_{th,j-c}$. The resolution and accuracy of T_j measurements are necessary in calculation of $R_{th,j-c}$.

The reference T_{ref} is measured by two thermocouples inserted between the thermal grease and the heatsink in the physical model and between thermal grease and air for the thermal model, shown in Figure 6.27. High resolution and accuracy of T_j and T_c measurement/estimation are critical for calculating the thermal impedance. T_c measurement has a 0.1ºC peak to peak noise. Measurement resolution can be improved by increasing the power losses and generating a larger temperature gradient at given thermal resistance. Obtaining a current of more than 20 A was not possible for the proposed set up experiment due to lack of facility, however it is suggested to increase the power losses for calibration purposes in a real application to increase the accuracy of the T_j. The added generated heat should not cause the T_j to exceed 150ºC degree else the chip will be likely damaged.

Figure 6.28 shows ΔT_{j-am} . The temperature rises to 63.51ºC for a 10% increase in thermal resistance and to 64.96ºC for 15% , to 66.41C for 20% and to 75.09ºC for 50%.

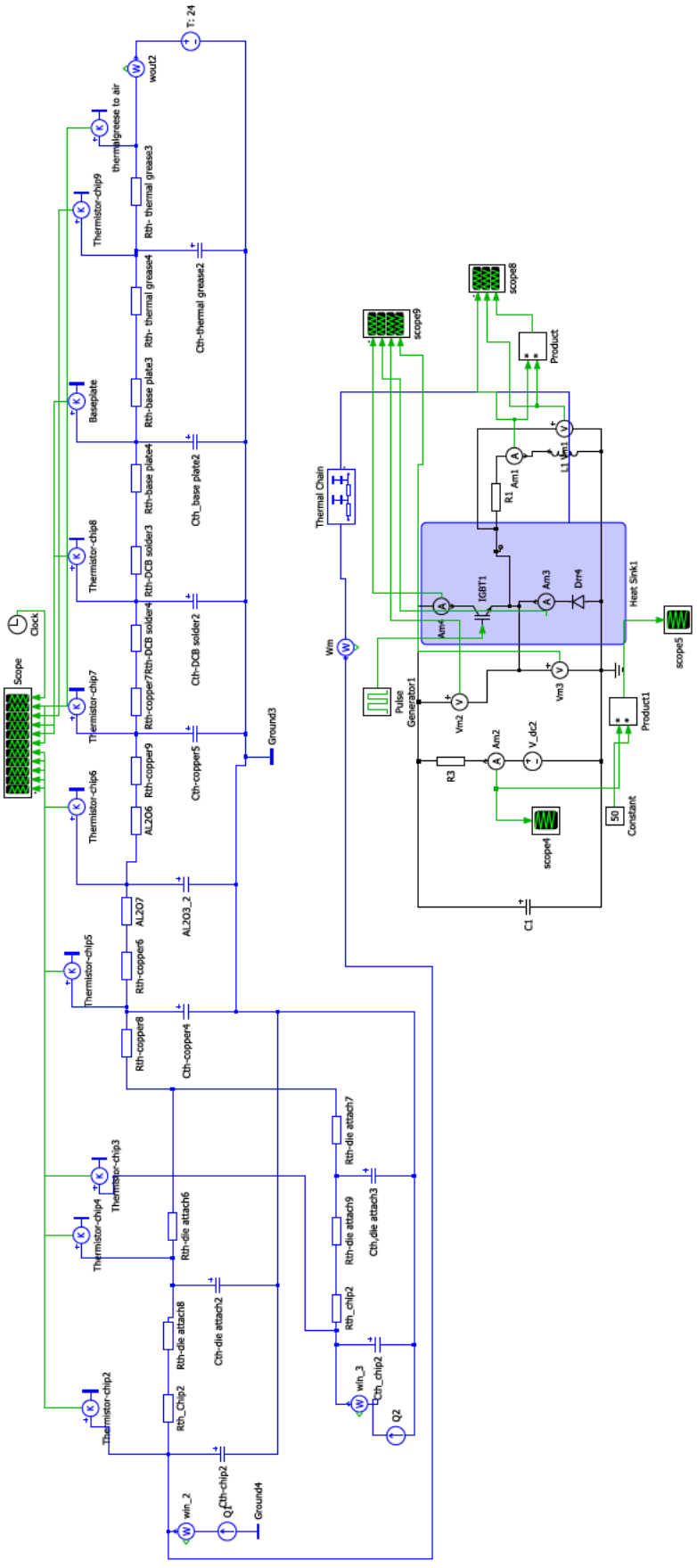


Figure 6.27: Thermal model

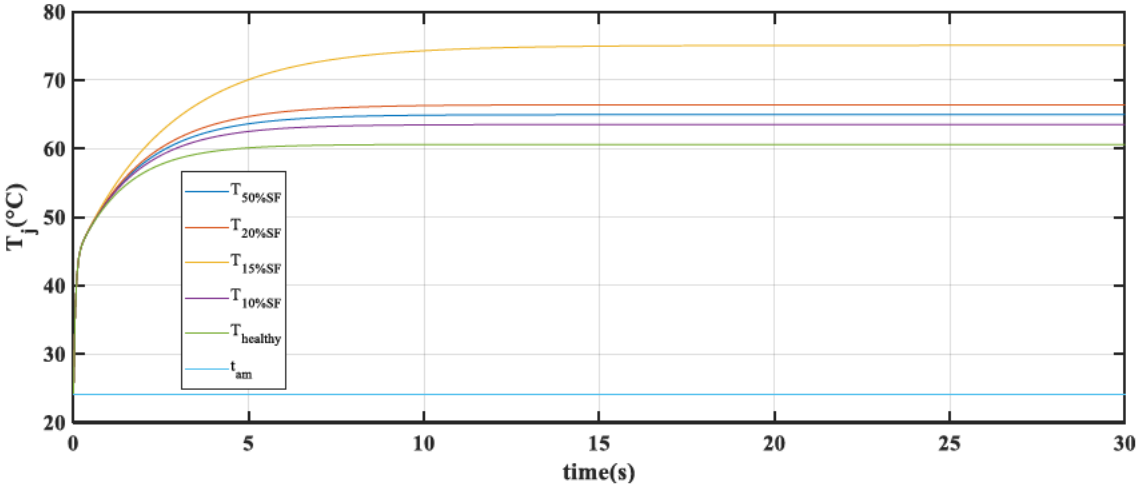


Figure 6.28: Temperature differences against time

The dissipated power affects the value of $R_{th,j-c}$ and should be investigated during the heating up process. The effect of ambient temperature on $R_{th,j-c}$ is a positive linear trend. A look-up table comprises the healthy thermal impedance at various T_{am} and can be built up for a healthy IGBT. A rise above this reference level in $R_{th,j-c}$ represents the progress of SF.

6.6 Detecting solder fatigue through monitoring $V_{CE,on}$

The variation of $V_{CE,on}$ with different level of SF degradation has been investigated to understand how $V_{CE,on}$ is sensitive to the progress of SF. Die-attach degradation causes increases in electrical as well as thermal resistance. Higher thermal resistance means higher T_j. This, in turn, generates higher charge carrier concentrations and lower $P^+ - N$ junction drop (V_i). In addition, an increase in T_j affects the carrier mobility and causes more reduction in the drift region (V_{drift}) [16]. The effect of SF on $V_{CE,on}$ is summarised in Figure 6.29. In this section, the sensitivity of this failure detector to SF is studied within the operation of three-phase converter. However, for the IGBT under test, increase in SF causes a decrease in $V_{CE,on}$ because the BJT effect is stronger than the MOSFET effect for currents below 80 A.

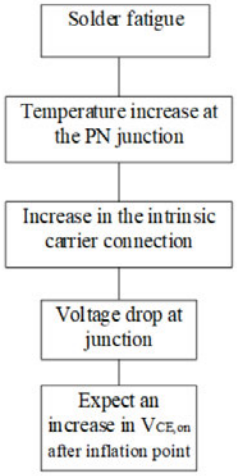


Figure 6.29: Effect of SF on $V_{CE,on}$

6.7 References

[1] Infineon, “Transient thermal measurements and thermal equivalent circuit models”, application note AN 2015-10, 2015.

[2] Y. Jian, J. D. van Wyk, W. G. Odendaal, and L. Zhenxian, "Comparison of transient thermal parameters for different die connecting approaches," Industry Applications Conf, IAS Annual Meeting, pp. 1818-1825 vol.3, 2003.

[3] A. S.Bahman; K. Ma, F. Blaabjerg, “A Novel 3D Thermal Impedance Model for High Power Modules Considering Multi-layer Thermal Coupling and Different Heating/Cooling Conditions”, IEEE Applied Power Electronics Conference, 2015.

[4] M. Quraan, P. Tricoli, D’Arco, and L. Piegari “Efficiency assessment of modular multilevel converter for battery electric vehicles”, IEEE Trans. Power Electron., accepted for publication, DOI: 10.1109/ TPEL.2016.2557579.

[5] S.Asuma, M. Kimata ; M. Seto ; Xinjian Jiang ; Haiwei Lu ; Dewei Xu and Lipei Huang “Research on the power loss and junction temperature of power semiconductor devices for inverter”, Proceedings of the IEEE International Vehicle Electronics Conference (IVEC'99) (Cat. No.99EX257), 2002.

[6] Z. Khatir, S. Carubelli, and F. Lecoq, "Real-time computation of thermal constraints in multichip power electronic devices," Components and Packaging Technologies, IEEE Transactions on, vol. 27, pp. 337-344, 2004.

[7] D. Xu, H. Lu, L. Huang, S. Azuma, M. Kimata, and R. Uchida, "Power loss and junction temperature analysis of power semiconductor devices," IEEE Transactions on Industry Applications, vol. 38, pp. 1426-1431, 2002.

[8] J. Antonios, N. Ginot, C. Batard, Y. Scudeller, and M. Machmoum, "Electrothermal investigations on silicon inverters operating at low frequency," in Thermal, Mechanical & Multi-Physics Simulation, and Experiments in Microelectronics and Microsystems (EuroSimE), 2010 11th International Conference on, 2010, pp. 1-5.

[9] Tang, Y. K. Fang, W. S. Liao, D. C. Chen, C. S. Yeh, and S. C. Chien, "Investigation and modelling of hot carrier effects on performance of 45- and 55-nm MOSFETs with RF automatic measurement", IEEE Trans. Electron. Devices, vol. 55, no. 6, pp. 1541–1546, Jun. 2008.

[10] J. Antonios, N. Ginot, C. Batard, Y. Scudeller, and M. Machmoum, "Electrothermal investigations on silicon inverters operating at low frequency," International Conference on Thermal, Mechanical and Multi-Physics Simulation, and Experiments in Microelectronics and Microsystems, 2011.

[11] D. Xiang, L. Ran, P. Tavner, A. Bryant, S. Yang, and P. Mawby, "Monitoring solder fatigue in a power module using case-above-ambient temperature rise", IEEE Trans. Ind. App., vol. 47, (6), pp. 2578–2591, Nov./Dec. 2011.

[12] C. Yu, J. S. Yuan, and H. Yang, "MOSFET linearity performance degradation subject to drain and gate voltage stress", IEEE Trans. Device Mater. Reliab., vol. 4, no. 4, pp. 681–689, Dec. 2004.

[13] Y.-S. Kim and S.-K. Sul, "On-line estimation of IGBT junction temperature using on-state voltage drop," in Proceedings of the 1998 IEEE Industry Applications Conference. Part 1 (of 3), October 12, 1998 - October 15, 1998, St.Louis, MO, USA, 1998, pp. 853-859.

[14] Gap Pad® 1500 Datasheet, Dec, 2011,
Available: http://www.bergquistcompany.com/pdfs/dataSheets/PDS_GP_1500_12.08_E.pdf

[15] Gap Pad® 3000S30 Datasheet, Dec, 2011.
Available: http://orionind.com/catalog/datasheets/PDS_GP_3000S30_12.08_E.pdf

[16] J-P M. CLECH, R.J. COYLE and B. ARFAEI, "Pb-Free Solder Joint Thermo-Mechanical Modelling: State of the Art and Challenges", Vol. 71, No. 1, 2019.

Chapter 7: Numerical Modelling of the Electrical Drive Train in a Wind Turbine

7.1 Introduction

Note that some parts of this chapter appeared in the Proceedings of the International Winercost conference held in Ankara (Moeini, Pietro, Hemida and Baniotopoulos) with appropriate referencing. This chapter describes the operating principles of the electrical drive train of a WT and culminates in a model using the Power Systems toolbox in Matlab. The electrical drive train of WT is split into the grid-side converter and rotor-side converter, the rotor-side and grid-side controllers, and the pitch angle controller. The model is based around a permanent magnet synchronous generator (PMSG).

7.2 Overview of the drive train

Figure 7.1shows an overview of the drive train from rotor blades, on the left, that convert wind power into rotation of the PMSG rotor shaft. The rotor-side converter converts mechanical power into electrical power in the form of a DC voltage and current. The grid-side converter converts the DC voltage and current on the DC-link into a three-phase voltage and current suitable for connection to the electricity grid.

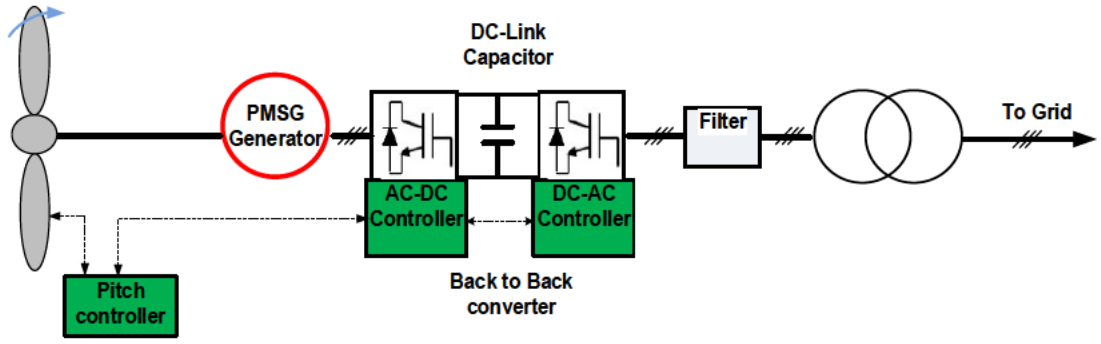


Figure 7.1: Diagram of back-to-back converter and controllers

Controllers for pitch angle, maximum power point tracking (MPPT), current, and speed were implemented in the model to investigate the effect of wind speed variations on the electrical quantities as seen by the rotor-side converter IGBTs and its influence on power losses that can directly affect the temperature variations of the power devices and, hence, their state of health. The various parts of the drive train and their numerical models are described further in the following sections, starting with the PMSG.

7.3 The permanent magnet synchronous generator

A PMSG is one of the common types of generator used in WT industry, as described earlier on in this thesis. The three-phase voltages of stator, v_a, v_b, and v_c, are the three phase voltages applied to the generator stator winding. The three-phase currents of the stator, called i_a, i_b, and i_c, flow in the machine. If the machine acts as a generator, there will be a net flow of real power out of the machine, the electrical power being given by $\sum vi^*$ (summed over all three phases).

The angular rotation speed of the PMSM rotor is denoted by ω_m (machine) or ω_r (rotor). The rotor angle θ_r is defined as the angle between the axis of the first phase to the q-axis. A three-phase PMSG with one pole pair shown in Figure 7.2. Electromagnetic torque (T_e) is positive when the PMSM operates as a motor and increases θ_r, and it becomes negative when the machine operates as a generator [1].

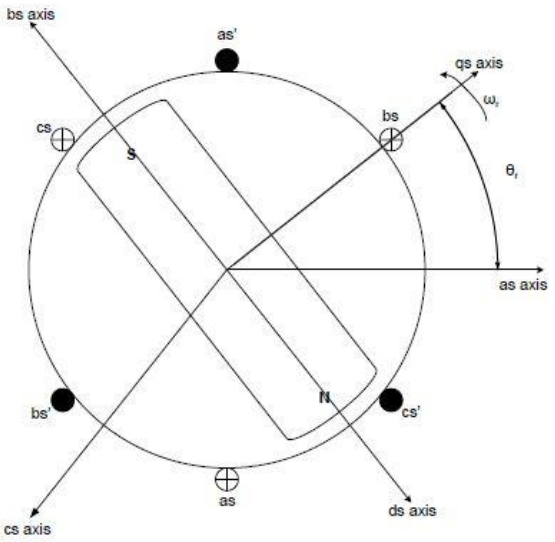


Figure 7.2: Schematic representation of a 1-pole three-phase PMSM [1]

For later, the d-axis is defined as aligned with the north pole of the rotor PM and the q-axis is 90° ahead [1]. When there is no load, the generator generates no current, rotates at its fastest rate, but generates no power. As the load current increases, the resisting mechanical torque on the generator shaft increases and the rotor speed reduces, increasing the generated electrical power. If the load is too high, the rotor slows down too much and the power produced drops to zero. The maximum power point tracking controller is designed to maximise the power output from the generator for a given wind speed. The rotor-side controller is designed to both control the speed of the shaft and to control the current in the generator.

7.4 MPPT and pitch controller

The maximum conversion efficiency of the WT occurs when the ratio between the turbine angular speed and wind speed, called tip speed ratio (TSR) [2]. As wind speed varies in time, the angular speed of WT will be adjusted to keep the conversion efficiency at the maximum level, for example looking at the power generated by the turbine using a dedicated control loop called maximum power point tracking (MPPT). The MPPT controller aims to maintain the power extraction coefficient of WT (C_P) at its maximum value. Figure 7.3 shows how the MPPT (the black dots) is affected by wind speed and the green line is the optimum power generated.

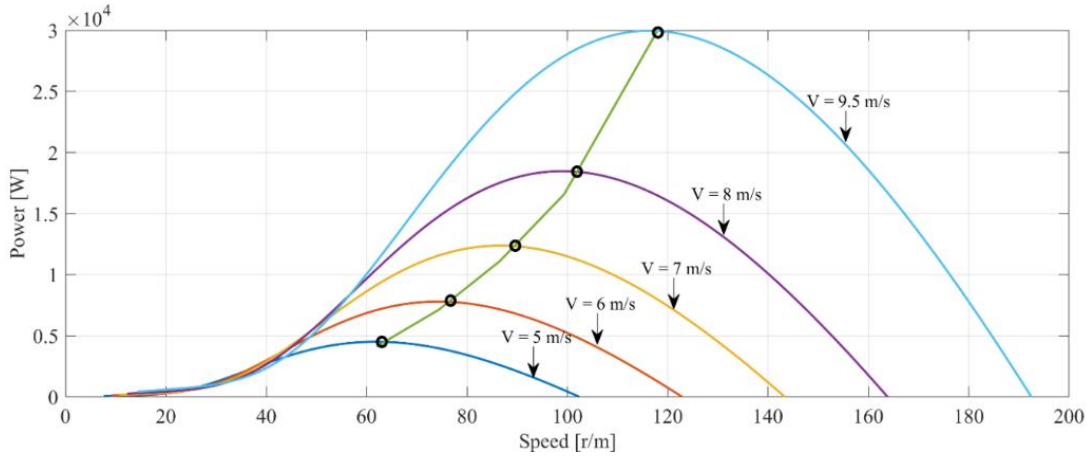


Figure 7.3: Mechanical power vs rotor rotational speed

7.5 Pitch controller

If the pitch angle of the blades can be altered, there is a pitch angle controller. This modifies the pitch angle of the blades to maximise the power that can be obtained from the wind. Figure 7.4 shows the pitch controller diagram. The speed and output power of the generator are continuously compared against the reference values. The reference pitch angle, β^*, can be mapped from the wind speed. P_m is calculated by equation (7.6).

$$P_m = T_n \times \omega_m \tag{7.6}$$

where P_m and ω_m are generator power and speed respectively. T_n is nominal torque of the WT.

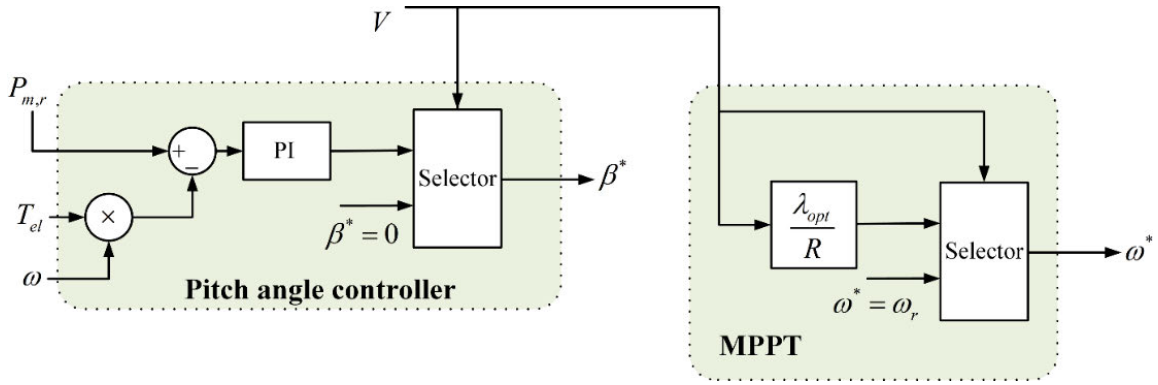


Figure 7.4: Diagram of pitch controller (and MPPT)

7.6 The rotor-side controller

The three-phase back-to-back converter has two separate controllers, namely the rotor-side controller and the grid-side controller. The rotor side controller receives input signals from the generator speed, current and the pitch controller to generate the pulse signals for the rotor side converter. The-grid side controller receives input signals from the grid voltage, grid current, and DC-link voltage to generate the pulse signals required as an input to the grid side converter. Each part of electrical drive train system is separately discussed in the following.

The rotor-side controller is used to control the generated torque and speed of the generator. The controller algorithm used for this purpose is called 'field oriented control' (FOC) [3]. The three axes of the generator, (a, b and c), 120º apart, are defined by the stationary winding of the stator. The diagram of the rotor-side controller is shown in Figure 7.5. It is made up of a pair of inner current control loops and an outer speed control loop. The rotor angle θ_r is measured by a rotary encoder and supplied to the Clarke-Park and inverse Clarke-Park transformations, and also used to obtain the angular speed ω_m by differentiation. The angular speed is compared to the reference rotor speed $\omega_{m,r}$ to generate an error input to the PI speed controller. The output of the speed PI controller is i_q^*, one of the rotating-frame current references for the inner current control loops.

The current control loops generate two mutually perpendicular voltage references, V_q and V_d, that are transformed into three-phase rotating voltage values, V_a, V_b and V_c, using an inverse Clarke-Park transformation. In practice, the values are in the form of duty cycle values to feed into three PWM generators that make the actual voltages applied to the generator. The resistance and inductance of the stator phase (R_s and L_s) can also added to the Clarke transformation for decoupling.

The three phase currents, i_a, i_b, and i_c, are measured and transformed into mutually perpendicular i_q and i_d by a Clarke-Park transformation that feeds back to the PI current controllers. Here, i_d is fed to one PI current controller (1) for which $i_d{}^*$is defined as the reference d-axis current and is set to zero. The other current, i_q is fed back to the other PI current controller (2) and compared to the reference given by the output of the speed controller.

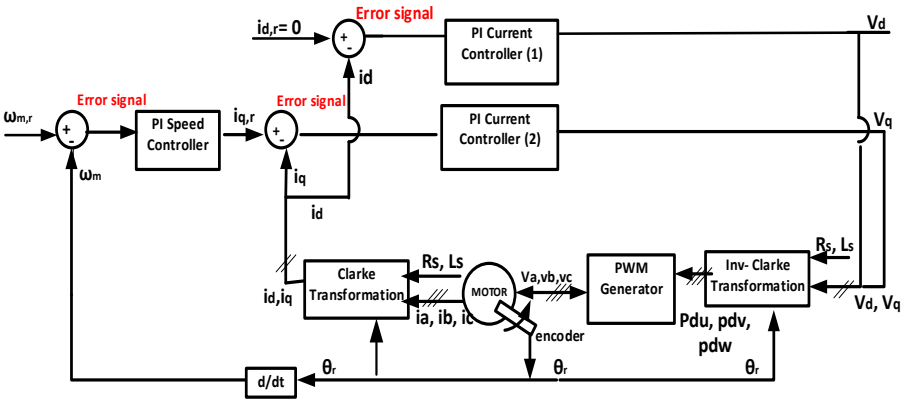


Figure 7.5: Rotor-side converter and controller diagram

The rotor-side controller (RSc) keeps the generator rotating at the reference speed value ω_m^* by changing the torque T_m^* produced by the generator. When the wind speed is below the rated wind speed, ω_m^* is set to maximise the available power (with MPPT). This is done such that the 'tip speed ratio', that is the ratio between the tangential speed of the tip of a blade to the actual wind speed, is such that maximum power can be extracted from the wind flow [4]. The reference speed ω_m^* is obtained by equation (7.4) [4].

$$\omega_r = \frac{\lambda_{opt} \times v}{R} \tag{7.4}$$

where R is rotor radius (m), ω_r is angular velocity (rad/s) of the rotor, v is wind speed (m/s) and λ_{opt} is optimal tip speed ratio. Equation (7.5) is used to achieve MPPT based on the value of T_e [5].

$$\frac{d\omega_m}{dt} = \frac{1}{j}(T_e - T_m - \beta\omega_r) \tag{7.5}$$

where J is rotor moment of inertia, T_m is the mechanical torque, β is the damping coefficient, ω_m is the generator speed, and T_e is the electromagnetic torque.

For wind speeds above the rated wind speed, the generator cannot generate any more electromagnetic torque T_e nor handle any more power, so the a pitch-angle controller takes over and keeps ω_m^* equal to ω_n. When the control range of the pitch angle has been fully used up, the rotor will be braked to a standstill until the wind speed reduces sufficiently.

Alternatively, when the wind speed is greater than the rated wind speed, the generator may be able to operate in an overspeed mode with weakening of the magnetic flux in the generator, so that that generator torque and power remain within their limits. Field weakening is achieved by applying and controlling i_d to weaken the desired magnet flux at the rotor. The PMG machine flux and the developed torque can be controlled separately and decoupled from each other – a major advantage of FOC.

7.6.1 Rotor-side controller

In synchronous machines operating up to the base speed, the speed of rotor is measured by a rotor encoder or resolver and used as feedback signal of the PI speed controller to generate the reference current i_q^* . The speed controller is designed from the Newton's 2nd law for rotating bodies, as indicated in (7.2). The transfer functions in the speed controller loop are shown in Figure 7.6. Control parameters, K_{P1} and K_{I1} are calculated by (7.3). The deal speed controller damping ratio is $\eta_W = \frac{1}{\sqrt{2}}$.

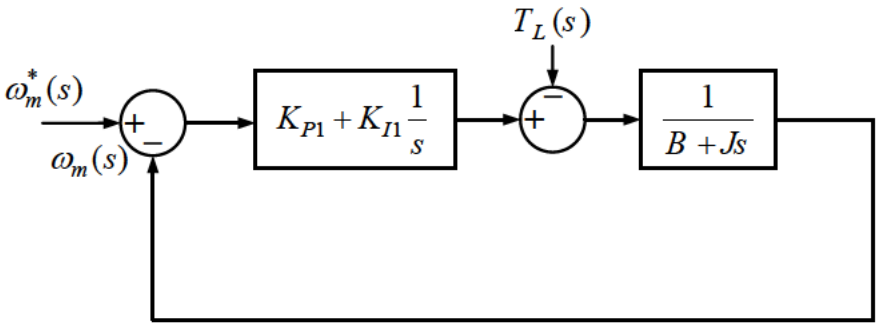


Figure 7.6: Speed controller block diagram

$$T = J\frac{d\omega_m}{dt} + \beta\omega_m \tag{7.2}$$

$$K_{P1} = 2 \times J \times \zeta_n \times \omega_n, \quad K_{I1} = J \times {\omega_n}^2 \qquad \omega_n = 2 \times \pi \times f_n \left(\frac{rad}{s}\right) \tag{7.3}$$

where J is moment of rotor inertia, T_m is assumed to be the mechanical torque, β is the damping coefficient, ω_m is the generator angular speed, T_e is the electromagnetic torque, ζ_n is damping ratio., and ω_n is generator rated speed.

7.6.2 Rotor-side converter and controller rotor-side converter

RSC utilises two independent controllers, namely the speed and torque controllers [1]. Figure 7.7 shows a block diagram of the conventional RSc. The speed controller determines the reference T_{el}^* with a PI regulator. The FOC control method is then used to control the electromagnetic torque of PMSG [6].

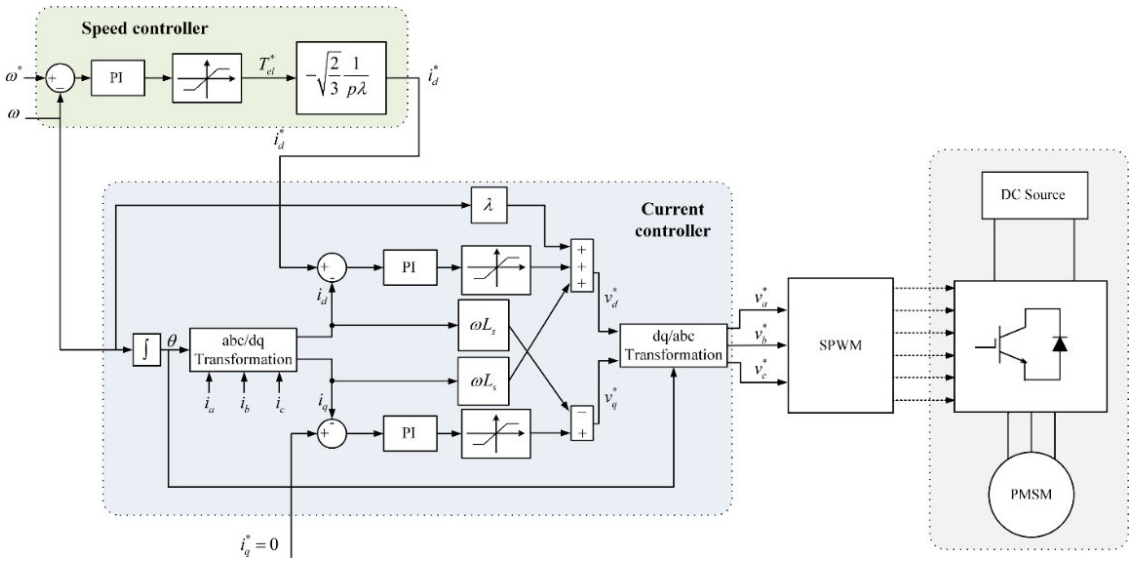


Figure 7.7: d-q axes current and speed controller

The FOC controls the stator current [7] so that the three-phase stator current is transformed into two orthogonal components using the following equations:

$$i_\alpha = i_a \tag{7.7}$$

$$i_\beta = \frac{1}{\sqrt{3}}(i_a + 2i_b) \tag{7.8}$$

These equations use the fact that $i_a + i_b + i_c = 0$.

The current components i_α and i_β are then transformed into a reference frame that is synchronous with the rotor to obtain the d-axis current, i_d, and q-axis current, i_q.

$$i_d = i_\alpha \cos\theta + i_\beta \sin\theta \tag{7.9}$$

$$i_q = i_\beta \cos\theta - i_\alpha \sin\theta \tag{7.10}$$

where θ is the rotor angular position.

In a PMSG, the flux generated by the magnet is approximately constant. Therefore, i_d^* is typically set to zero for operations below the base speed and the torque is only controlled by i_q [26], as shown in equation (7.11):

$$T_e = \frac{3}{2} N_p i_q \varphi_f \tag{7.11}$$

where N_p is number of pair pole and φ_f is flux.

The tuning process for the current PI controller is simpler if the current control is decoupled [7]. In order to decouple the control of i_q and i_d, (7.12) and (7.13), which are the stator equations written in

the rotating reference frame, can be rearranged to assume that the current i_q in the first equation and the current i_d in the second equation are feed-forward terms taken from the measurement of the actual current. The inverse Clarke Park is applied to transform the reference voltages V_d and V_q into the three-phase voltages, V_a^*, V_b^* and V_c^*. These three phase voltages then generate three duty cycles of PWM pulses using a PWM generator.

$$V_d = R_s i_d - L_s \frac{di_d}{d_t} - \omega_r L_s i_q \tag{7.12}$$

$$V_q = R_s i_q - L_s \frac{di_q}{d_t} - \omega_r L_s i_d + \omega_r \emptyset_f \tag{7.13}$$

$$V_\alpha = V_d \cos(\theta_r) - V_q \sin(\theta_r) \tag{7.14}$$

$$V_\beta = V_d \sin(\theta_r) - V_q \sin(\theta_r) \tag{7.15}$$

$$V_a^* = \mathrm{V}_\alpha \tag{7.16}$$

$$V_b^* = \frac{-\mathrm{V}_\alpha + \sqrt{3}\mathrm{V}_\beta}{2} \tag{7.17}$$

$$V_c^* = \frac{-\mathrm{V}_\alpha - \sqrt{3}\mathrm{V}_\beta}{2} \tag{7.18}$$

where V_α ,V_β are orthogonal stationary reference frame quantities and V_d, V_q are rotating reference frame quantities.

7.7 GSC and GSc

The grid-side controller maintains the DC-link voltage constant by adjusting the power flowing to the grid and hence the amount of current taken from the DC-link. In a similar way to the rotor-side controller, FOC is used. A Clarke-Park transform is used to turn three-phase grid currents to i_q and i_d These currents are fed to two separate current controllers. Phase is maintained using a phase-locked loop (PLL) that locks the output frequency of WT to that of the grid. The whole controller is shown in Figure 7.8.

Here, i_d^* is considered zero as reactive power is assumed zero. Active power is linked only to i_q^*. Here, i_q^* is achieved through a PI controller that sets the PWM duty cycles in a three-phase voltage generator. The reference DC-link voltage and DC-link voltage are inputs to a PI controller. Then, an inverse-Clarke Park transformation is applied to generate three PWM pulse voltages. The generated PWM pulse voltages are applied to the semiconductor gates. In this model, with increasing generator torque, the DC-link voltage tends to increase. To maintain the DC-link voltage constant, the current controller increases the amount of current fed to the grid while voltage and phase angles stay constant.

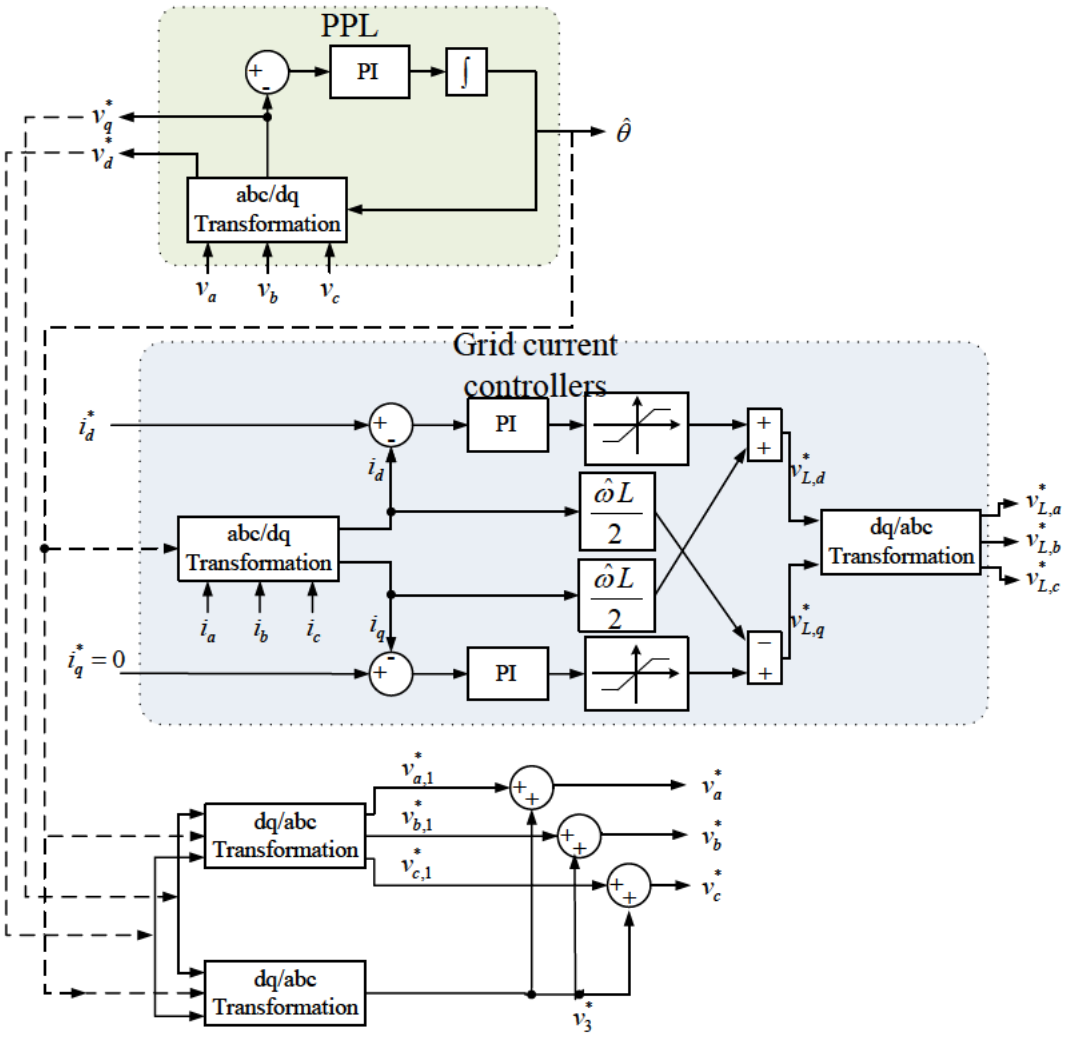


Figure 7.8: d-q axes current controller and PLL for grid side controller

The majority of insulated gate bipolar transistor (IGBT) failures occur in the rotor-side converter (RSC) so the DC-link and the grid-side converter (GSC) are replaced in the model with an ideal DC voltage source. The GSC controller is considered to be fast enough to maintain the DC-link voltage constant during wind speed variations. The ideal voltage source can absorb any amount of current and can even supply current to the rotor side converter and turn the rotor blades if the rotor side is operated as a motor rather than as a generator.

7.8 Modelling of RSC for a large wind turbine with pitch controller

In this subsection, the RSC and RSc are modelled for a 35 kW WT as a case study. This model is used to investigate the effects of wind speed variations on IGBTs used in power electronic converters. The

results of this chapter helps to evaluate the effects of wind speed variations on the converter. This has been done to validate effect of wind speed fluctuations on IGBT failure detectors.

The specifications of PMSG and controllers used in RSC are described in [8]. An RSC is numerically modelled while GSC is assumed as an ideal voltage source, Figure 7.9. A large WT with a PMSG is used. The parameters are selected to keep the numerical model the same as real application where pitch controller is applied. A modelled wind profile is used for to drive the WT [8]. A real wind speed profile has been applied and varies from 6 to 12 m/s. The three-phase PMSG has a rated speed of 230 RPM. The DC-link voltage is set as 850 V and achieved based on equation (4.19). The generator has 26 pole pairs, R_s is 0.05 Ω and L_s is 6.3 mH.

$$V_{ac} = \sqrt{\frac{3}{2}} \times M \times \frac{V_{dc}}{2} \tag{7.19}$$

where M is the modulation index, and V_{ac} is the generator voltage.

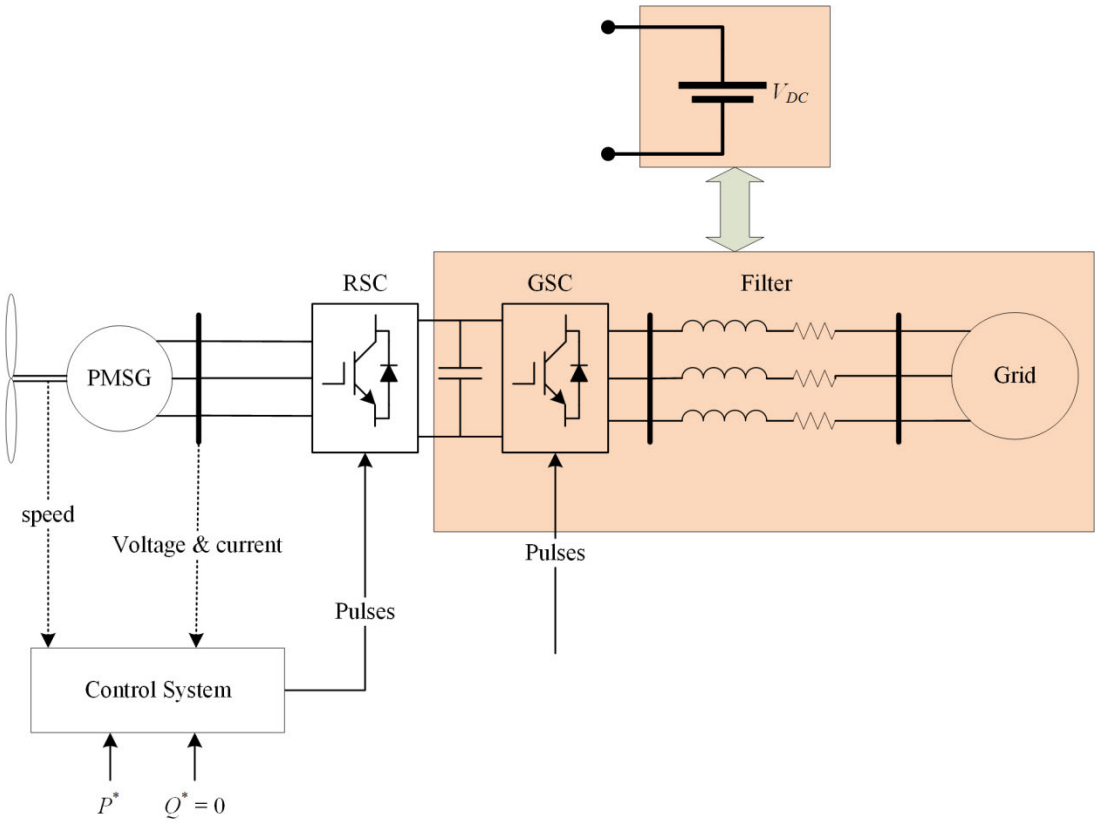


Figure 7.9: Rotor-side diagram and controllers

7.8.1 Output of controllers

Here, i_d^* is considered zero and torque is only controlled through i_q. As shown, i_d and i_d^* follow each other. Validation of current controllers is shown in Figure 7.10.

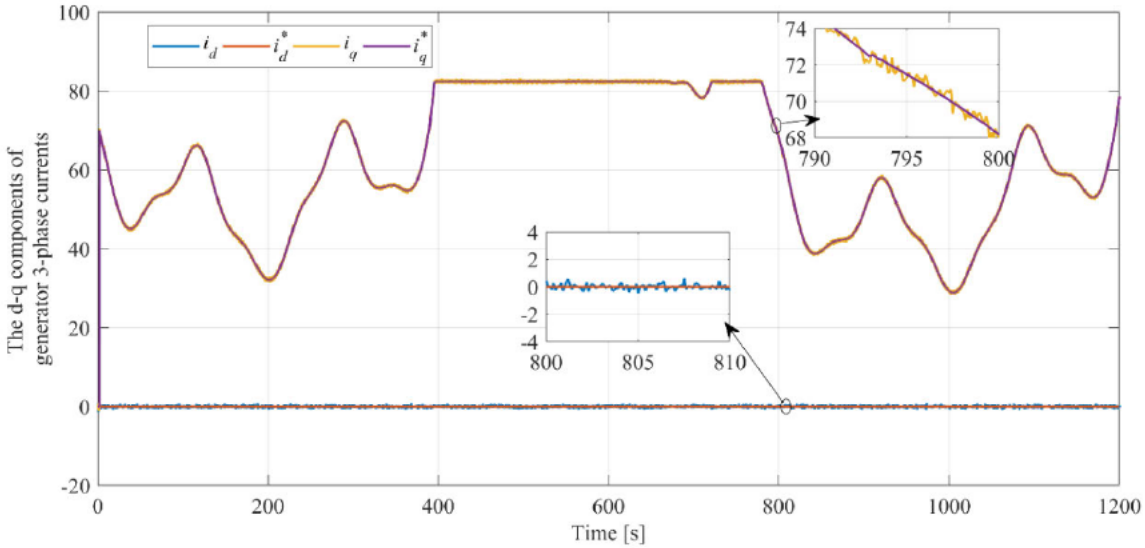


Figure 7.10: Validation of current controller

The transfer function of the current controller is shown in Figure 7.11. The PI controller parameters are achieved by (7.20) thru (7.25).

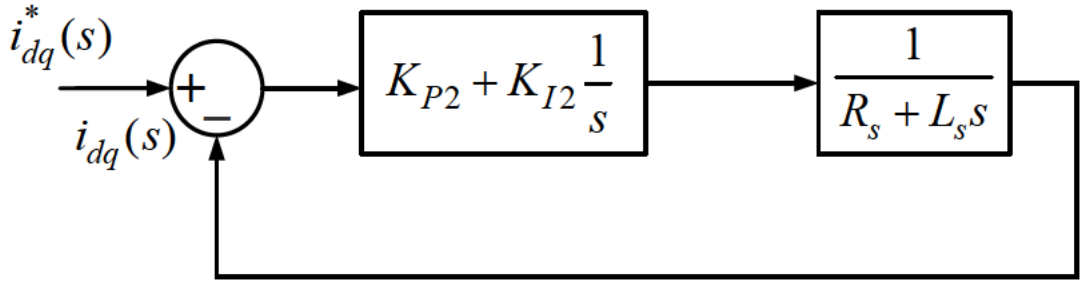


Figure 7.11: Block diagram of current controller

$$\tau_R = \frac{1}{\sqrt{2}} \tag{7.20}$$

$$\omega_{nR} = 2 \times \Pi \times f_{nR},\ f_{nR} = 2000 \tag{7.21}$$

$$kp_{aR} = 2 \times L_s \times \tau_R \times \omega_{nR} \tag{7.22}$$

$$ki_{aR} = L_s \times (\omega_{nR}{}^2) \tag{7.23}$$

$$kp_{dR} = kp_{aR} - (ki_{aR} \times \frac{T_s}{2}) \tag{7.24}$$

$$Ki_{dR} = Ki_{aR} \times T_s \tag{7.25}$$

For lower rated wind speed, the MPPT is operating. Thus, the torque and power output are variable. From 0 to 400s and 780 to 1200s, the wind speed is lower than rated and the MPPT controller operates and pitch angle is zero. When the wind speed becomes higher than the rated speed, the pitch actuators will change pitch angle of the blades. During this time the generator speed and torque are kept constant. Figure 7.12 shows a block diagram of the pitch controller. The WT rotor diameter, R, is 12.5 m. Controller parameter K_{p3} (7.26) and K_{I4} (7.27) are constant parameters and calculated from the transfer function in Figure7.10. K_{p3} is 0.001 and K_{I4} is 0.1.

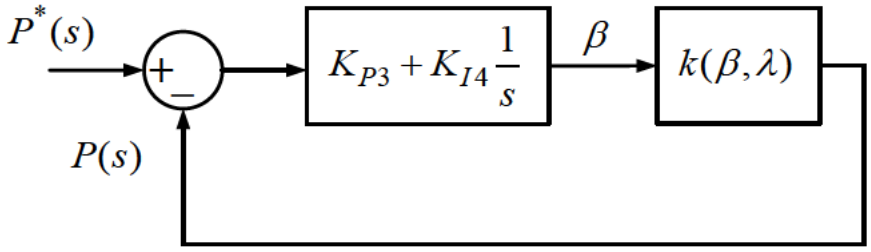


Figure 7.12: Blade pitch controller

$$K_{P3} = \frac{1}{2\zeta\omega_n} \tag{7.26}$$

$$K_{I4} = \frac{\omega_n}{2\zeta} \tag{7.27}$$

As shown in Figure 7.13, the generator speed remains constant for higher than rated wind speed if the pitch controller is used. This can help to reduce load fluctuations and consequently temperature swings within the RSC IGBTs.

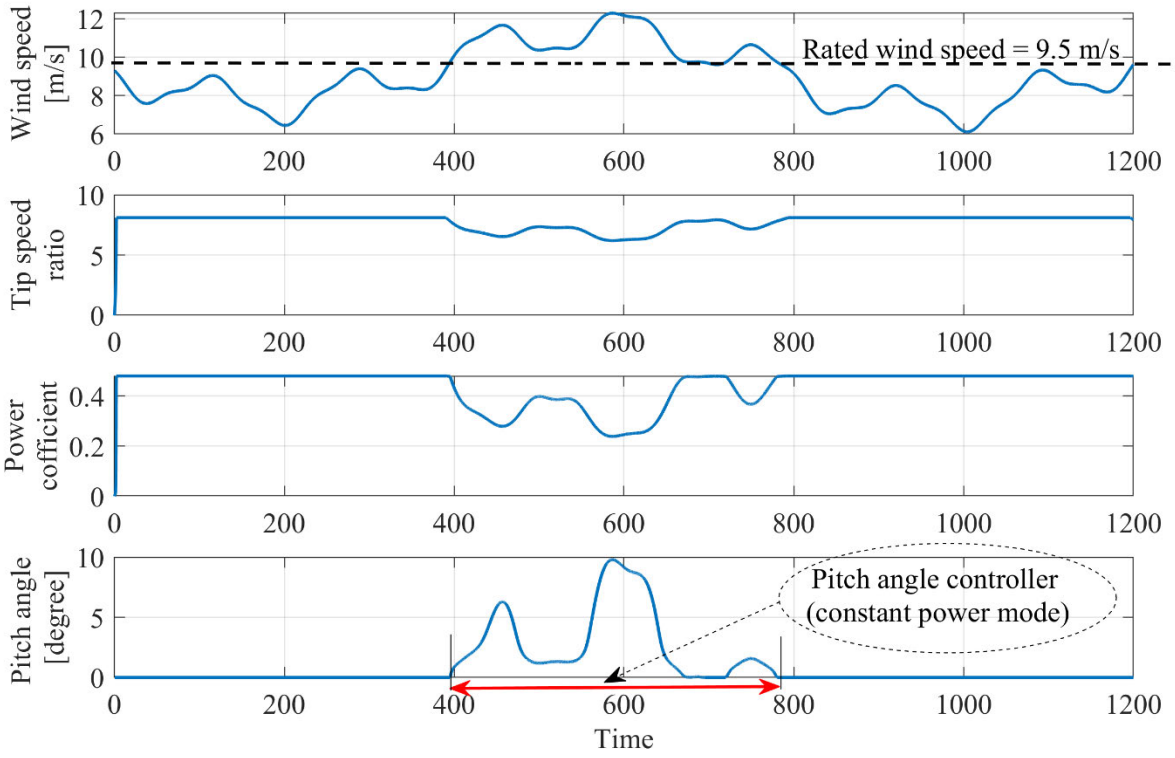


Figure 7.13: Validation of blade pitch controller

Figure 7.14 shows the generator torque applied to a PMSG. The machine speed reaches 230 RPM for the rated wind speed. The operation of the speed controller is shown in Figure 7.14b. As shown, ω_m follows ω_m^*. Here, ω_m is kept constant when the wind speed is higher than rated. The generator speed changes quickly with ω_m^* as torque is high and inertia is low. In this WT, Δt has a component with positive gain to $\Delta\omega_m$, $100\times\frac{\pi}{30}$, and a negative gain to torque, 2.5×10^3. Thus, Δt is too low and ω_m can follow ω_m^* very quickly. The electrical frequency of the generator also follows the same trend as ω_m^*. The frequency varies from 0 to 50 Hz according to the wind speed. As shown in Figure 7.14c, fundamental frequency varies with wind speed. Figure 7.15 shows the active and reactive power of the WT. Reactive power is kept zero and active power is kept constant for higher range of wind speed and varies based on MPPT.

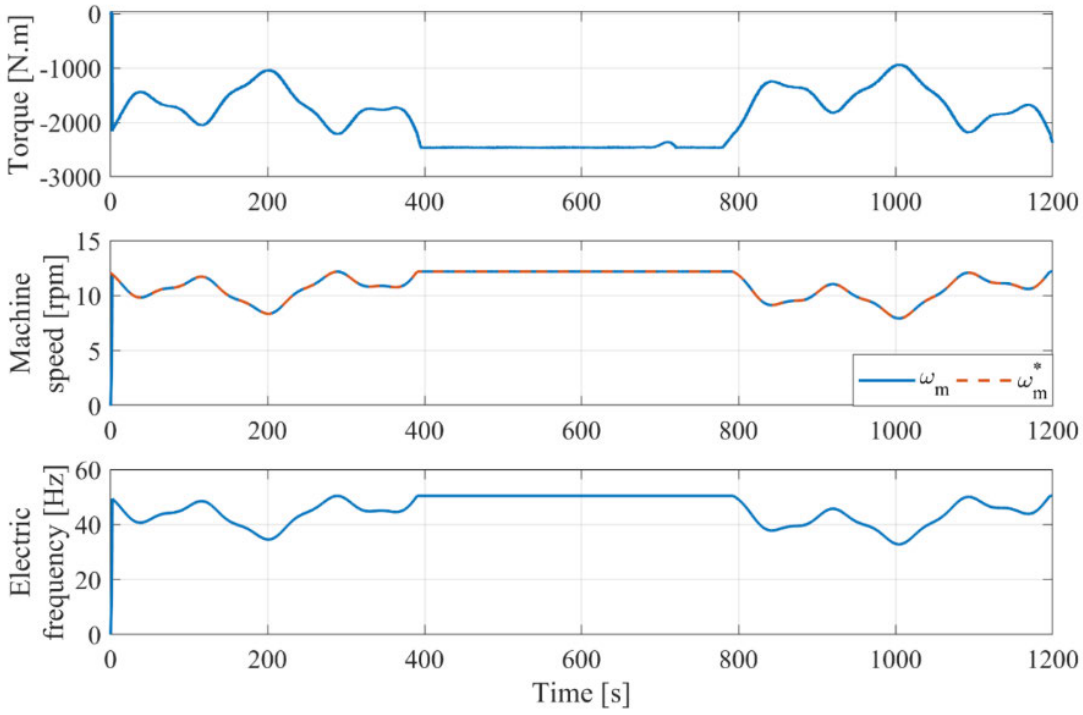


Figure 7.14: Validation of speed controller

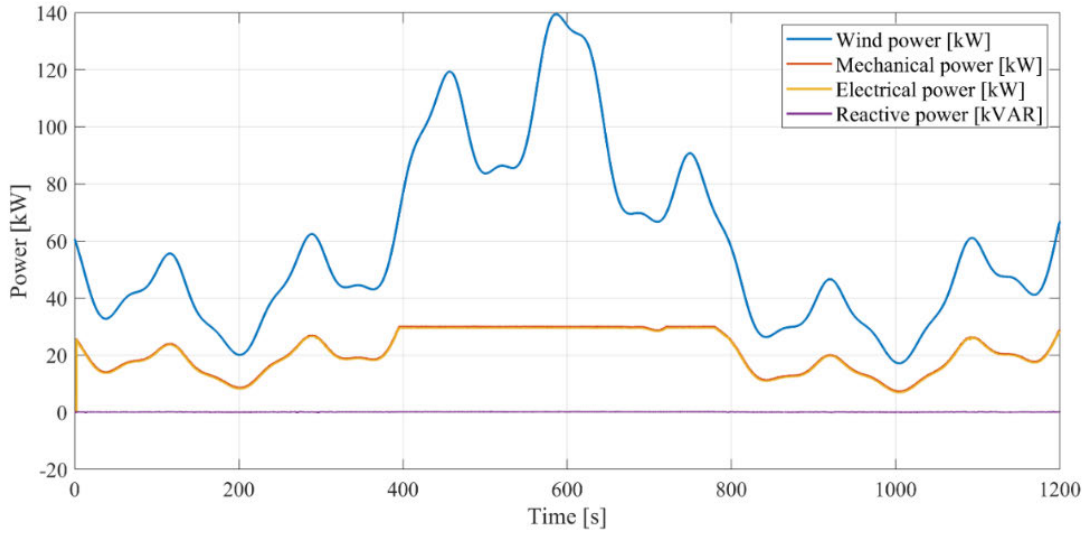


Figure 7.15: Active and reactive power of the WT and applied wind profile

Figure 7.16 shows the C_P curve of a WT which is obtained from a datasheet, Appendix B. The maximum available instantaneous output power of the WT is shown with black dots on the curve. Here, C_p is calculated by equation (7.28).

$$C_p = \frac{P_{m,n}}{(0.5\times(R^2\times\pi)\times R_{ho}\times(V_r{}^3))} \tag{7.28}$$

where P_m^* is power in per unit of nominal power for particular values of ρ and A; R_{ho} is 1.225.

Here, $C_{\mathrm{P,pu}}$ is the performance coefficient in per unit for the maximum value of C_p. $v_{wind,pu}$ is wind speed in per unit for the mean value of expected wind speed in m/s (as base). k_p is power gain for $C_{P,pu}$ is 1 per unit and $v_{wind,pu}$ is 1 per unit. A generic equation is used to model $C_p(\lambda,\beta)$ explained by (7.29). This equation is based on the modelling turbine characteristics of [1]: c_1 = 0.5176, c_2 = 116, c_3 = 0.4, c_4 = 5, c_5 = 21 and c_6 = 0.0068; R is rotor diameter, 12.5 divided by 2.

$$C_p(\lambda,\beta) = c_1\left(\frac{c_2}{\lambda_i} - c_3\beta - c_4\right)e^{-\frac{c_5}{\lambda_i}} + c_6\lambda \tag{7.29}$$

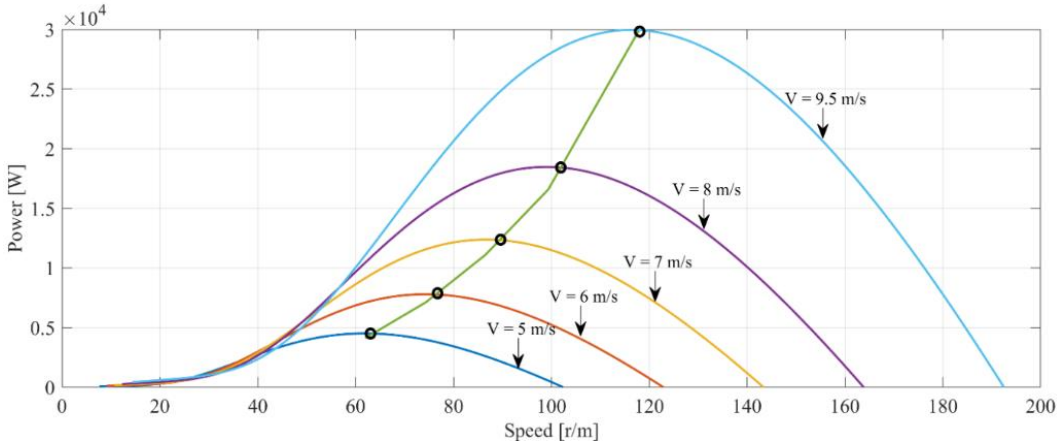


Figure 7.16: Power coefficient and instantaneous power output of WT

Figure 7.17 shows the output current and fundamental frequency of the generator at 5 different wind speeds. The wind speed is shown from 6.5 m/s to 12.3 m/s in the rows. The first column is the line-to-line voltage. The second column shows the phase voltage and a low pass filter is applied to the PWM signal to find out the fundamental frequency of the generator in at different wind speeds. The third column is line current for phase a.

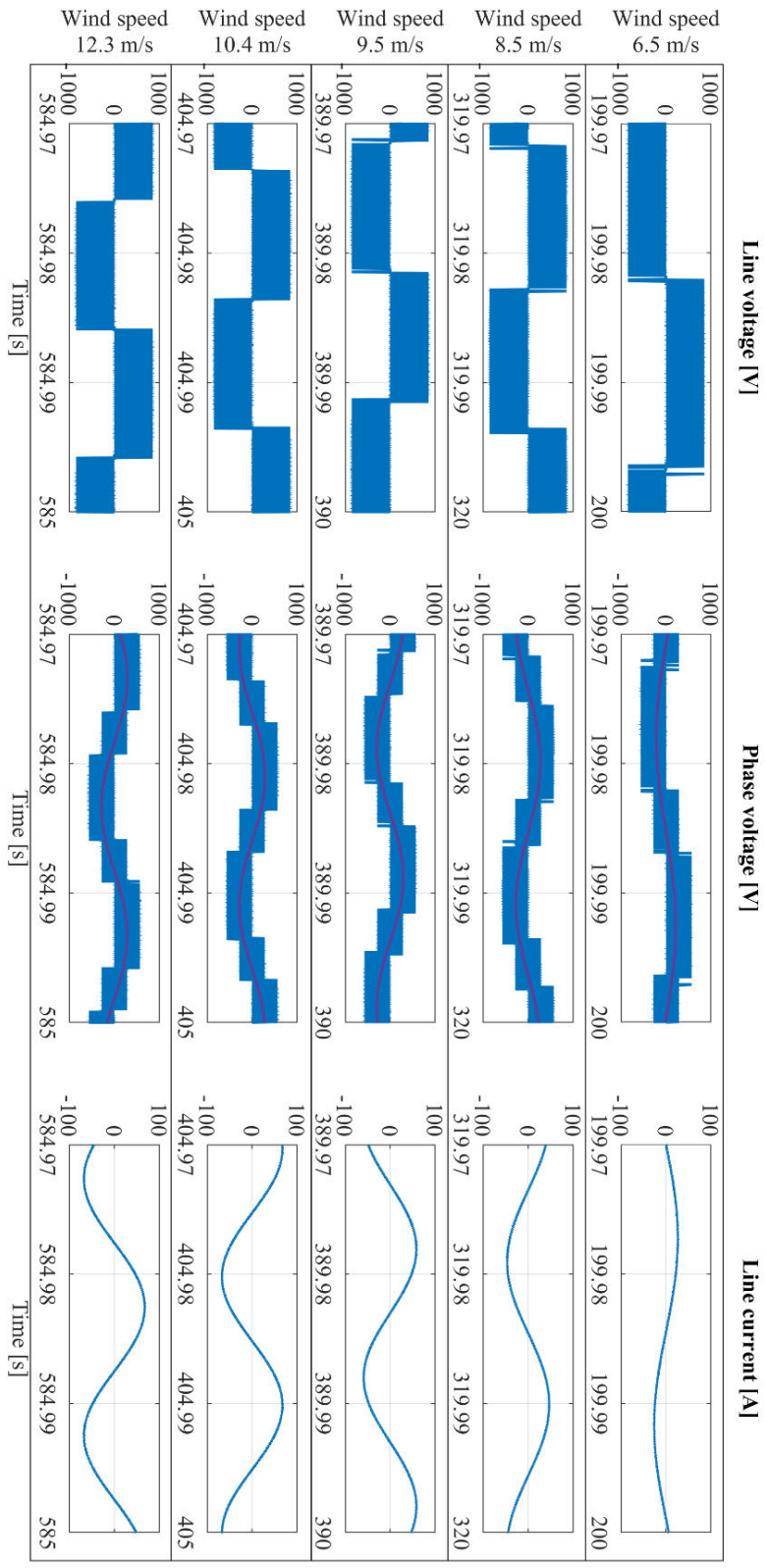


Figure 7.17: Line-to-line output voltages and currents

7.9 Modelling of RSC and RSc without pitch angle for a micro wind turbine

An RSC is numerically modelled while GSC is again assumed as an ideal voltage source. The rated power is 105 W and the rated speed is 900 rpm. Here, T_m^* is 1.11 Nm, V_n is 81 V and ω_m^* is 94.2 rad/s. The wind speed varies from 4.7 to 10.88 m/s. These parameters are selected to keep this numerical model the same as an off-the-shelf micro WT, Appendix B. In this model there is no pitch controller. The model was used to match the physical hardware use in the lab setup with almost the same electrical parameters and control algorithms as used in the laboratory test rig. In addition, the results in Figure 7.30 are used to as a load profile for a prototype converter in the experimental chapters.

7.9.1 Validation of rotor side controller without pitch angle

Direct coupling with the PMSG is the type of EDTS in this model. Since the generator flux is constant, it is assumed that i_d^* is zero. Validation of the current controllers for the rotor side is shown in Figure 7.18. The operation of speed controller is shown in Figure 7.19. As it is discussed previously, ω_m^* is determined based on wind speed variations. The generator speed follows ω_m^*. Here, ω_m^* is the rated speed, 8 m/s. As there is no pitch angle controller, the torque varies with wind speed variations higher that the rated speed.

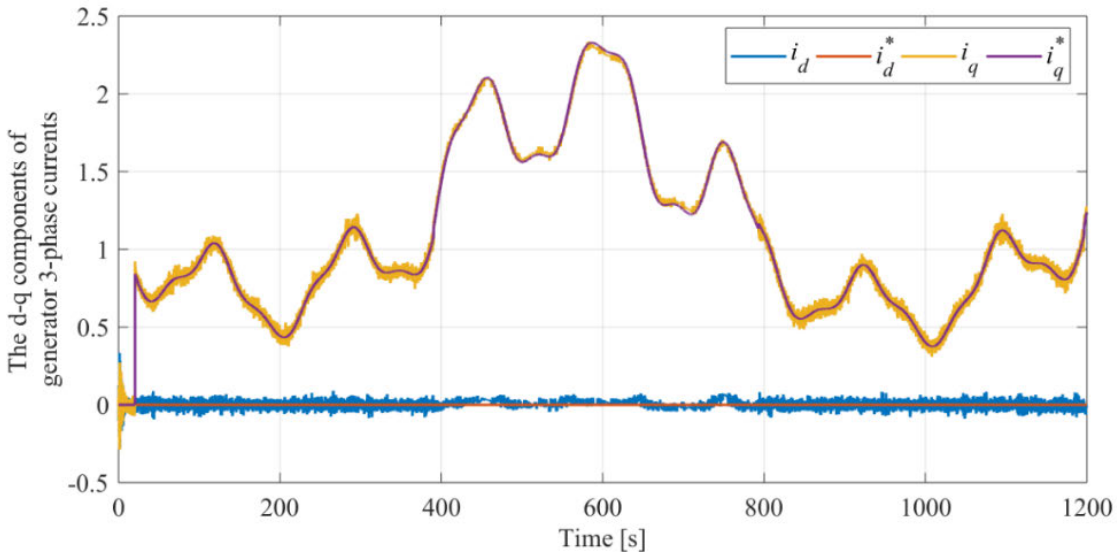


Figure 7.18: Validation of current controller

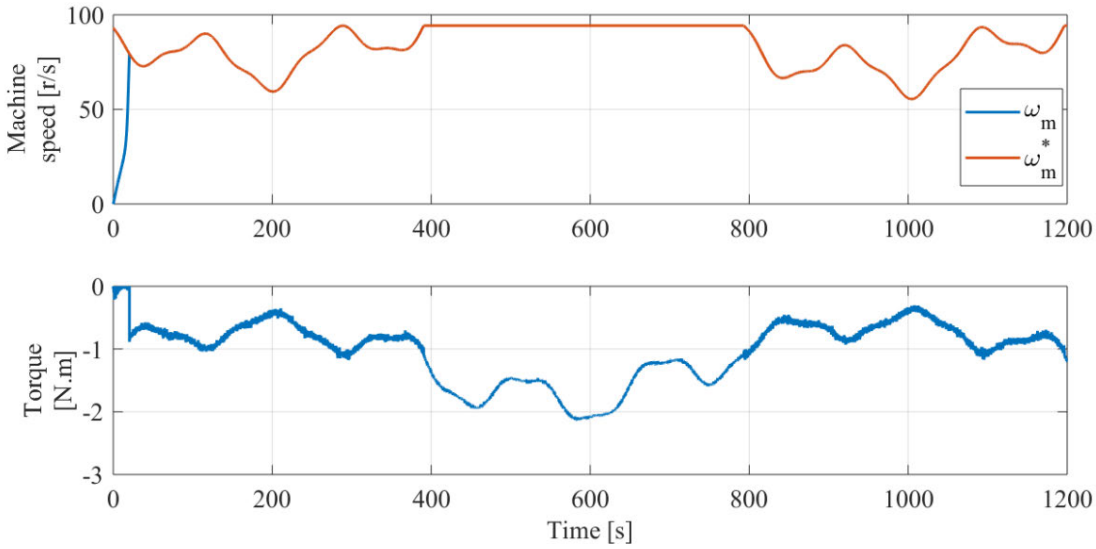


Figure 7.19: Validation of speed controller

Active and reactive generated power as well as mechanical power are shown in Figure 7.20. Reactive power should be zero, and is roughly so. Figure 7.21 shows the wind speed profile applied to the WT as well as the tip speed ratio and C_p. Figure 7.22 shows the three phase currents and voltages of the generator for a range of wind speeds. A low-pass filter has been applied to the PWM phase voltage to show the fundamental frequency, Figure 7.23. Figure 7.24 shows C_P curve of WT based on datasheet. Black dots show the instantaneous maximum power output of the generator.

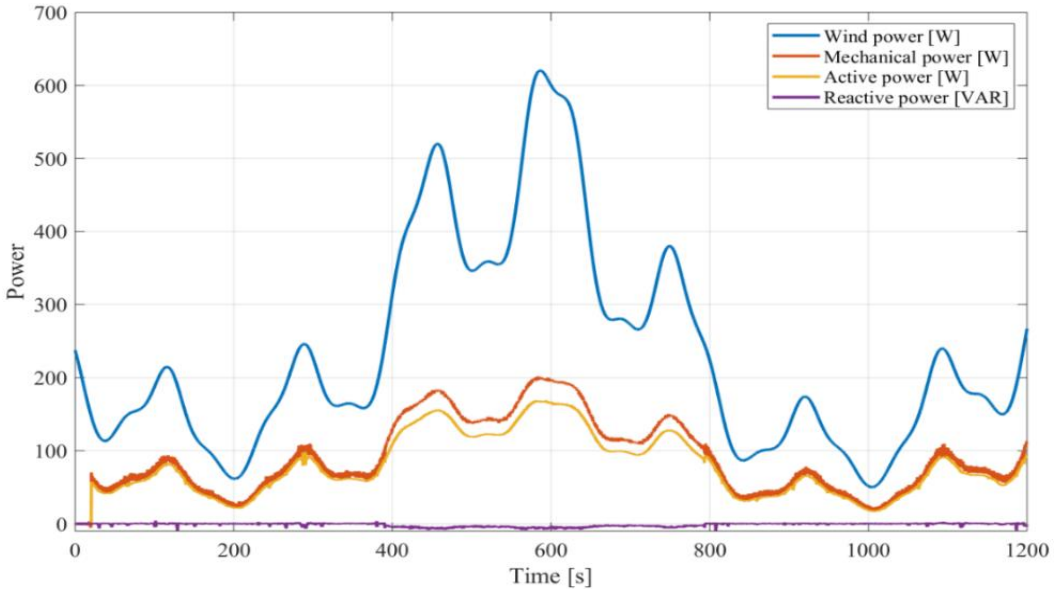


Figure 7.20: Active and reactive power

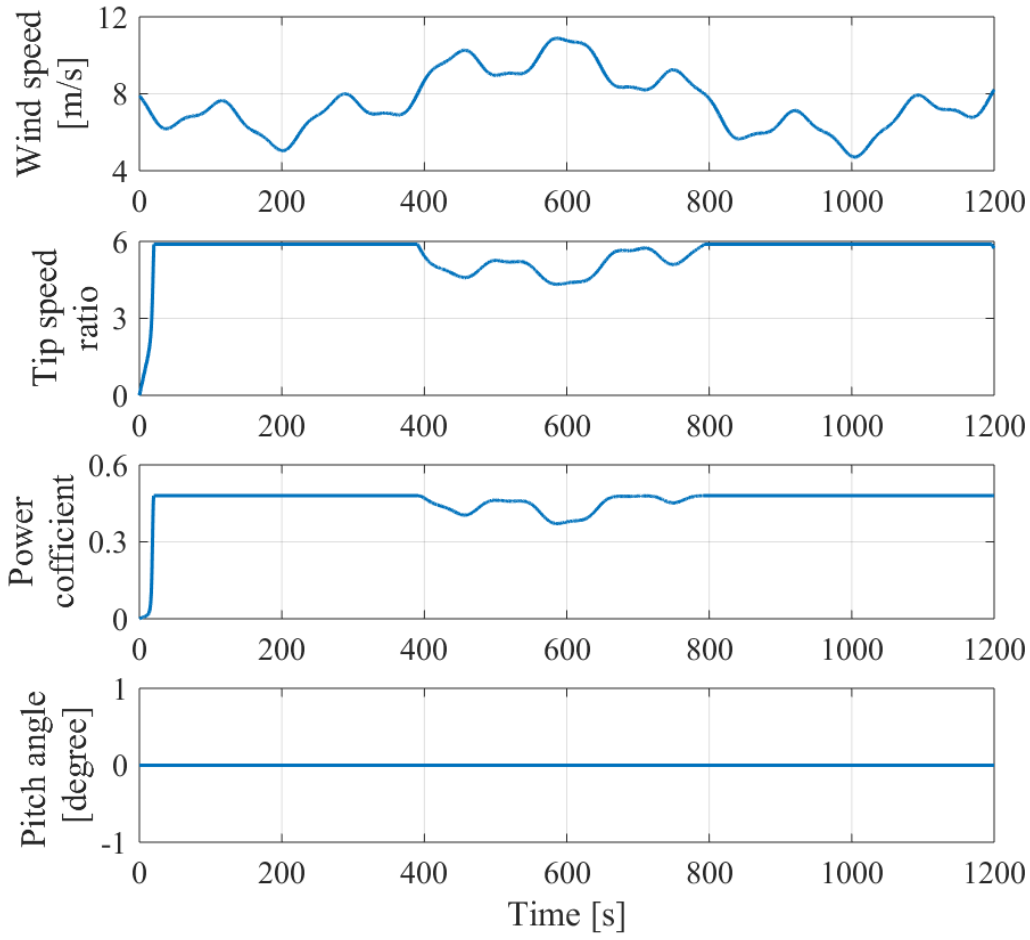


Figure 7.21: Tip speed ratio and power coefficient

To understand failure mechanisms of IGBTs in a WT application, it is necessary to realise the effects of wind speed variations on IGBT performance. This is because the random nature of the wind speed leads to random degradation and subsequent reduction in lifetime of the IGBTs. It might be possible to investigate the failure mechanisms and possible failure of detectors within the operation of a full-scale WT as used in a wind farm or perhaps within a wind tunnel. However, because of lack of facilities such as real data from a wind farm or an appropriate wind tunnel, the effect of wind speeds on IGBTs is instead investigated separately, based on what the IGBTs would 'see' as a result of random wind speeds. Outcomes of this chapter help to understand the relationship between wind speed, generated current, and generator frequency. As explained, ω_m^* is modified for lower than rated wind speed if a pitch controller is present and will change continually where there is no pitch controller. Figure 7.22 shows the three-phase generator current – the current amplitude has a positive correlation with wind speed. At lower than rated wind speeds, the amplitude is variable as ω_m^* varies with wind speeds. This causes temperature swings and increase in conduction losses for higher load currents. At higher than rated wind speed, the amplitude and fundamental frequency of the generator is constant as ω_m^* is equal to ω_n. Figure 7.23 shows the fundamental frequency of the generator. The fundamental frequency of generator

can also affect acceleration of the cooling down process of the IGBT modules. The higher the frequency, the lower the available time to cool down the IGBT. These issues can reduce the lifetime of IGBTs and result in premature failures.

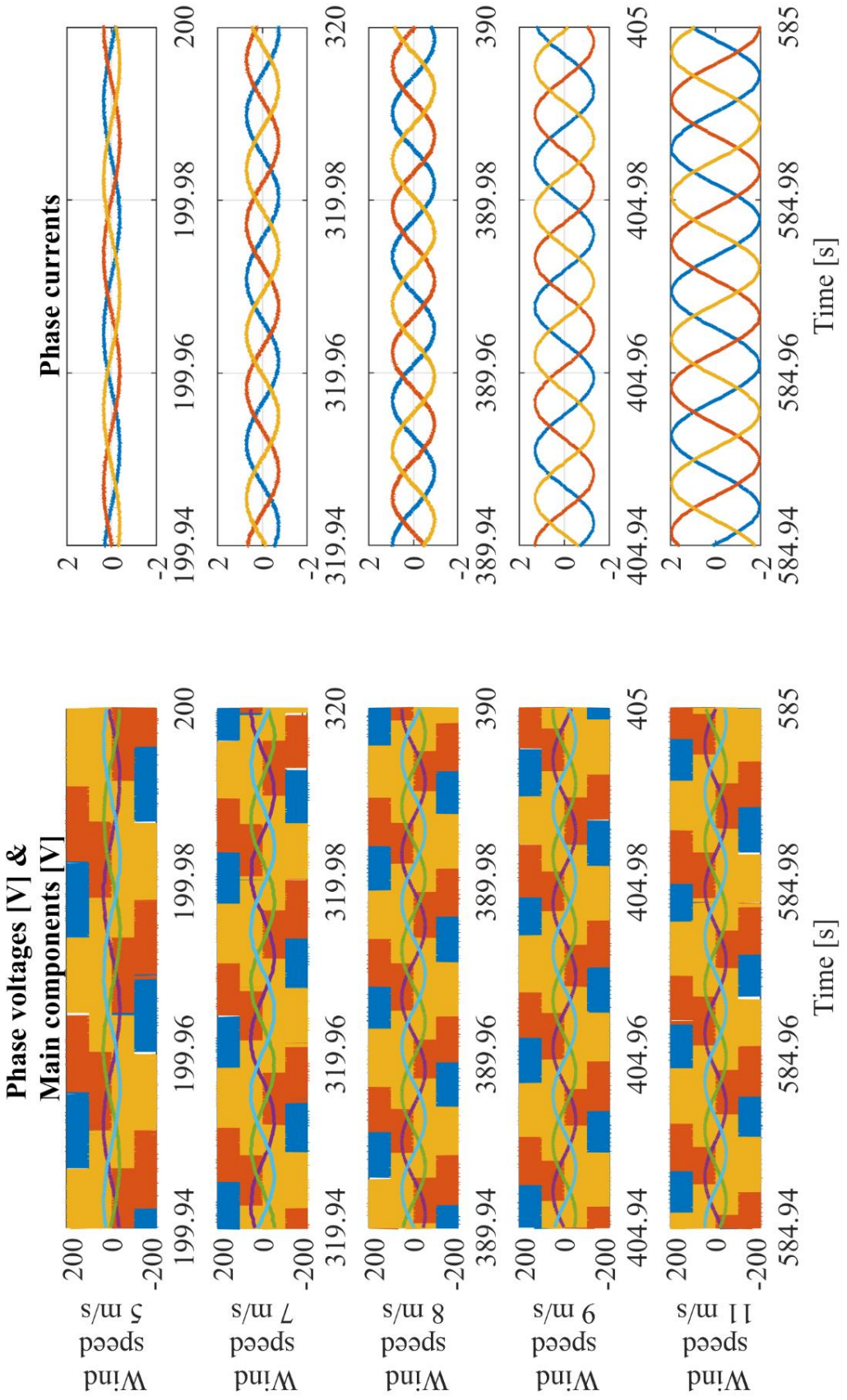


Figure 7.22: Phase and current/voltage of converter

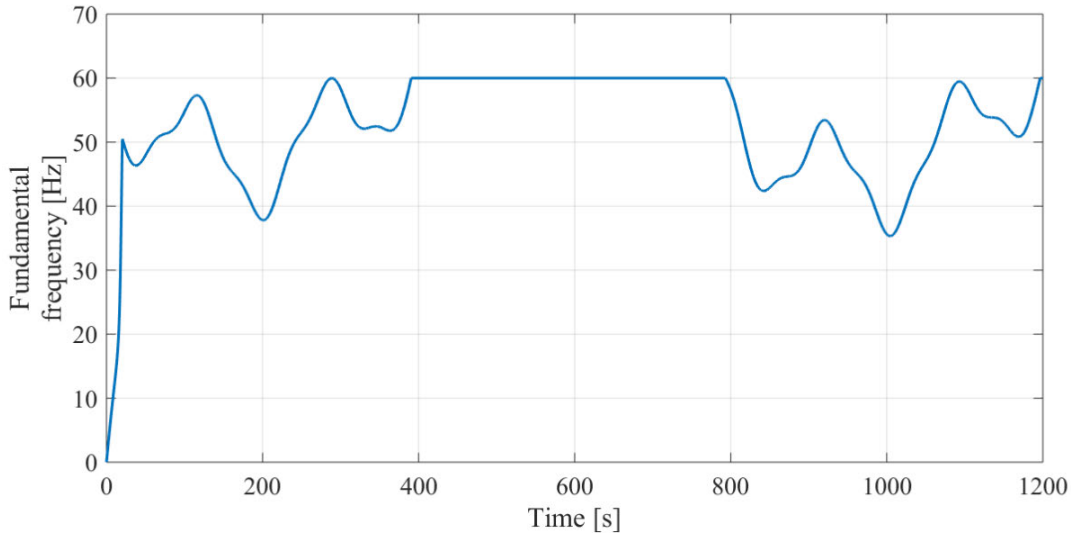


Figure 7.23: Electrical fundamental frequency of generator

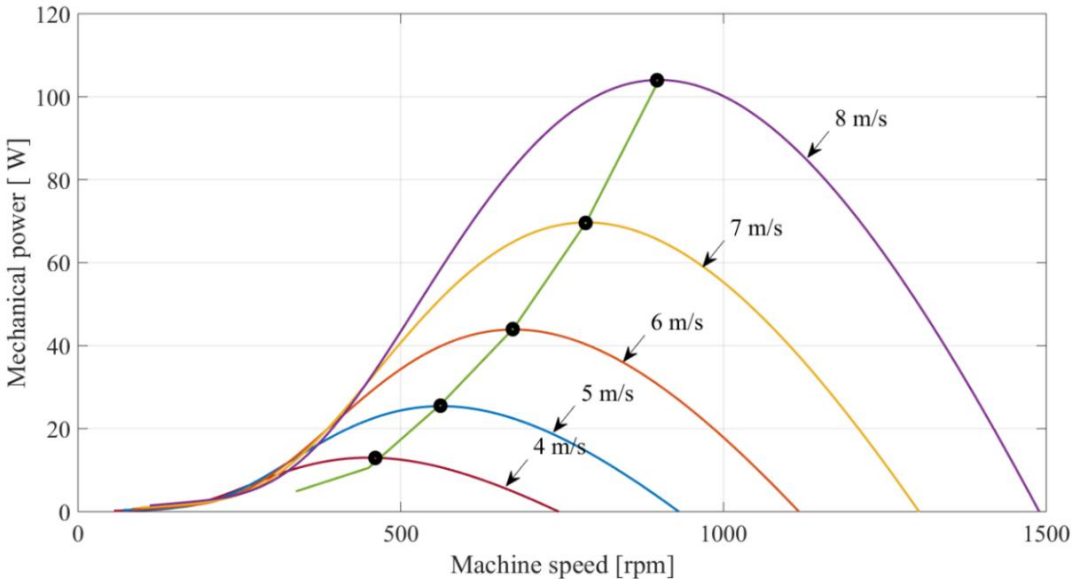


Figure 7.24: Machine power vs machine speed

7.10 Effect of wind condition on the efficiency and reliability of wind turbines

In order to enhance efficiency of WTs and satisfy grid utility codes, power converters are used [9]. Power electronic converters are therefore commonly used in advanced WTs. Consequently, increasing the availability of the converters can enhance the reliability of WTs. To achieve this target, consideration of the root causes of failure mechanisms of the power converters is required.

Wind flow originates from differential heating of the atmosphere by the sun in combination with forces arising from the rotation of the earth and different heat storage in water and on the land causing variable atmospheric pressure around the world. WTs can generate electrical power from the wind [9]. The higher the wind speed, the higher the potential power generated – up to a point [10].

Wind speed is one parameter that affects WT efficiency. Temperature swings are divided into long-term thermal cycling originating from wind speed variations, and short-term thermal swings originating from switching losses of the converter itself [11].

Wind speed variations adversely affect the residual lifetime of IGBTs so that although higher wind speeds (above 10 m/s) occur during only a small portion of the wind profile of a whole year, the majority of the consumption of the IGBT lifetime can be assigned to this portion [12-13]. However, the effect of wind condition on the lifetime of IGBTs is generally ignored so further evaluation is needed to find the effect of wind speed variations on TSEPs and failure mechanisms. Temperature ripple caused by wind speed variations significantly reduce the lifetime of IGBTs [14]. Generator side converters have lower lifetime compared to grid side converters as variation in the grid side output power is much smoother due to the dc-link capacitors [15]. The installation location of WTs is also important for their lifetime and failure mechanisms. IGBTs used in offshore applications have less lifetime compared to those used in on-shore applications with the same rated output power [19]. This is because offshore WTs experience much higher average wind speeds than their on-shore counterparts.

Wind condition also is another parameter that can seriously affect the efficiency of WTs through aerodynamic effects. There are two different types of wind flow, laminar and turbulent flow [17]. All WTs operate in an atmospheric boundary layer, as they close to the surface of the earth and the air flow is affected by friction and the viscosity of ground surface. Turbulent inflow increases the efficiency of WTs because turbulent inflow hinders separation of wind flow in the suction side of WT blades [18, 19]. Furthermore, in wind farms, many WTs operate in the wake of another WT, causing different efficiencies for wind turbines operating in different turbulent intensities. The higher turbulent intensity, the faster the wake wind recovery [20]. Turbulence influences the power curves of WTs so that with an increase in turbulent intensity the power increases at the cut-in speed and power decreases at the rated and cut-out speed [21]. Significant and high fluctuations of wind speed and wind gusts and different turbulent intensity flow causes a severe fluctuation of the electrical power generated by WTs. The voltage across the DC-link changes in different wind condition during WT operation. Fluctuation of the DC-link voltage causes temperature swings especially in electrical switching semiconductor components (the IGBTs). However, the direct effect of atmospheric turbulent flow and wind gusts on the accuracy of health condition monitoring systems of power converters is not clear and needs further investigation [22].

An implementation of on-line health condition monitoring system is the aim, so the possibility of practical implementation of each failure indicator is scored. Moreover, the accuracy of each indicator is scored based on the dependency on the occurrence of failures in time and appearance of the other failures at the same time. Complexity of implementation of each indicator depends on the linearity of the detectors with T_j: the better the linearity the less the complexity. Sensitivity to detection of the appearance of failures early enough to be useful is scored and based on literature, and the trend variation of each indicator is mentioned in the table. It can be concluded that it is necessary to find the relationships between wind condition and wind speed and the effect on T_j within the converter operation. The wind speed is a three-dimensional vector. However, the direction of the vector wind speed in the vertical axis can be ignored due to this is not be observed by an active surface (active surface facing the wind).

7.11 Summary

The majority of failure mechanisms occur in the rotor-side converter rather than in the grid-side converter. This is because the rotor side converter can operate at a lower range of frequencies as well as with wide range of load fluctuations. This will lead to a significant change in the output current of the generator. The higher the wind speed, the more the generated current. A pitch controller can keep the generator speed constant for higher rated wind speed. However, not all WTs use a pitch angle controller. In addition, the adverse effects of wind fluctuations can be still a concern for lower-than-rated wind speed when the pitch angle is zero. The effect of using a pitch angle controller on the operation of IGBT will be discussed further in the discussion chapter. Wind speed is emulated to change the fundamental frequency and current of the generator. The current and frequency profile achieved by the second numerical model is used in a practical converter. The effects of current and frequency fluctuations on the operation of IGBT as well as IGBT failure detectors were studied in chapters 5 and 6.

7.12 References

[1] Y. Liu, G. Tao, H. Wang, F. Blaabjerg, “Analysis of indirect rotor field oriented control-based induction machine performance under inaccurate field-oriented condition”, IECON IEEE Industrial Electronics Society, 2017.

[2] A. Takemura ; F. Tatsuta ; H. Yokoyama ; S. Nishikata, “Studies on field current control method for constant tip speed ratios of series connected WT generators in a wind farm”, Int Conf on Electrical Machines and Systems (ICEMS), 2012.

[3] C. Busca, A.-I. Stan ; et al, “Control of Permanent Magnet Synchronous Generator for large wind turbines”, 2010 IEEE International Symposium on Industrial Electronics, 2010.

[4] K. Tan, S. Islam," Optimum control strategies in energy conversion of PMSG wind turbine system without mechanical sensors", Vol.19, (2), IEEE Transactions on Energy Conversion , 2004.

[5] J.Morren a, J. Pierik b, S. W.H. de Haana, "Inertial response of variable speed wind turbines", Electric Power Systems Research, 2006.

[6] I. Houtzager , "Towards data-driven control for modern wind turbines", PhD thesis, 2011.

[7] Nilu Mary Tomy ; Jebin Francis, "Field oriented sensorless position control of a hybrid stepper motor with extended Kalman filter", Int Conf on Intelligent Systems and Control (ISCO), 2016.

[8] T. Samina ; S. Rama Iyer ; A. Bisharathu Beevi, "Rotor side control for improving the transient response of Doubly fed induction generator in wind power system", International Conference on Technological Advancements in Power and Energy (TAP Energy), 2017.

[9] K. Xie, Z.Jiang, and W.Li, "Effect of Wind Speed on Wind Turbine Power Converter Reliability", IEEE Transactions on energy conversion, VOL. 27, NO. 1, MARCH 2012.

[10] J. Ribrant and L. M. Bertling, "Survey of failures in wind power systems with focus on Swedish wind power plants during," IEEE Trans. Energy Convers., vol. 22, no. 1, pp. 167–173, Sep. 2007.

[11] S, X. Dewei, L. Haiwei, H. Lipei, S. Azuma, M. Kimata, and R. Uchida, "Power loss and junction temperature analysis of power semiconductor devices," IEEE Trans. Ind. Appl., vol. 38, no. 5, pp. 1426–1431, Sep. 2002.

[20] M. Aten, G. Towers, C. Whitlry, P. Wheeler, J. Clare, and K. Bradley, "Reliability comparison of matrix and other converter topologies," IEEE Trans. Aero. Electron. Syst., vol. 42, no. 3, pp. 867–875, Jul. 2006.

[21] G. Zhang, D. Zhou , J. Yang , F. Blaabjerg , "Fundamental-frequency and load-varying thermal cycles effects on lifetime estimation of DFIG power converter, Microelectronics Reliability 76–77 (2017), pp.549–555.

[22] S R. Allen, "Energy analysis and environmental life cycle assessment of a micro-wind turbine", Sage journal, 2008.

Chapter 8: Discussion and conclusion

8.1 Research achievement and project specific

Note that some parts of this chapter appear in the Proceedings of the International ICMT conference, Italy (Moeini, Tricoli, Weston, Tricoli, Dinh, McGordon) with appropriate referencing.
Health condition monitoring of WTs can be an effective way to reduce costs related to maintenance and to limit unexpected power generation interruptions. The electrical systems of a WT, especially the power converters, see the largest proportion of failures; hence, health condition monitoring is key to improving the reliability of WTs. From the literature review it is clear that there is a complex correlation between the variation of the IGBT parameters and failure mechanisms and, therefore, an effective health condition monitoring algorithm has to be considered that operates at the same time as the converter operation.

The main issue with state-of-the-art health condition monitoring systems is the trade-off between accuracy, complexity and implementation costs, especially for on-line health condition monitoring. This work has been reviewed the main methods used to detect faults and the degradation of the IGBT modules used in WT converters to highlight the main areas of research - "failure detection of BWLO and SF in the IGBT using failure detectors in the WT". Although several health condition monitoring methods have previously been proposed, undesired false alarms remain a huge challenge. This is because all degradation mechanisms of the IGBTs have an impact on the module T_j. Consequently, almost all inherent electrical IGBT parameters can be affected by, T_j. However, T_j can be varied by unrelated failure phenomena such as wind conditions in the application of WTs. Therefore, this is necessary to decouple the temperature variations originating from failure mechanisms from those variations unrelated to failure phenomenon.

Three different electrical parameters are chosen to be continuously measured and analysed. One parameter is assigned as a failure detector and the other one as a T_j estimator. The chosen temperature

estimator parameter has a low sensitivity to the progress of failure. This low sensitivity helps more accurate estimation of T_j regardless to the progress of failure. Two another electrical parameters are chosen as 'failure detectors' to detect failure mechanisms via $V_{CE,on}$, used to detect BWLO, and $R_{th,j-c}$ to detect SF. At each moment of diagnosis two electrical parameters are assigned to be measured. One is the instantaneous measured failure detectors and the other is that expected to be achieved according to the outcomes of the calibration set up. Two different electrical parameters are assigned to be measured in each time interval. Divergence from the expected value represents the presence of a failure mechanism.

Wind speed variations can cause errors when identifying the IGBT health status in a WT application. This is due to the different load cycling and consequent IGBT thermal fluctuations. This can be considered as an unrelated-failure phenomenon in a WT application. Future health condition monitoring systems are expected to overcome the limitations of the current methods by combining several methods together and using cross-correlation techniques to discriminate different degradation mechanisms.

The IGBT modules are extensively used in the WT power electronics converter. Yet, it is difficult to approximate correctly their reliability as it is reliant on the operating condition of the system. This is due to thermal expansions mismatch between multi-layers of the IGBT modules, especially between the silicon die and the next few layers. BWLO and SF are the most common degradations causes failure in the IGBT modules. These degradations affect the temperature distribution within the IGBT modules and hence, early failures of the modules.

Therefore, monitoring of temperature is not recommended as a health condition monitoring approach of IGBT especially for variable and unpredictable loads like those of the WTs. This work studies the influence of BWLO on the switching characteristics in particular the t_{off}. This study has been conducted at different DC-bus voltages, T_j and load currents. BWLO is manually enforced to the module by physically lifting off some of the bond wires. Moreover, SF is modelled by changing the thermal resistance between junctions to case. SF effects the thermal coupling between the silicon die and the contact pad, introducing voids between the layers and reducing the effectiveness of the power transfer from the die to the heatsink. The effects of these faults on the switching characteristics of the IGBT module are discussed in detail by comparing the experimental results of healthy and degraded modules.

The aim of the following experiments was to verify feasibility of the proposed approach and the behaviour of the diagnosis parameters. The test was carried out using a half bridge Vishay module. The experiment was carried out in different scenarios: calibration of failure detector parameter ($V_{CE,on}$) was conducted by applying one short pulse signal to the calibration circuit (shown in Figure 5.6). The test

was carried out while keeping the temperature constant during the test. The validation results show that $V_{CE,on}$ is a function of i_c and T_j. The higher sensitivity to temperature is achieved at around 50º C. During the test V_{GE} was frequently checked in order to determine that the rise in measured voltage was due to the BWLO or change in other condition such as T_j and i_c. The chip temperature and *ic* are continuously measured. Multiple measurements of V_{GE} and i_c were recorded and analysed to validate t_{off}. These three parameters are put in a lookup table to estimate T_j. The module has its own NTC is inserted inside the substrate. The NTC sensor temperature is close to the local diode chip and is distant from the IGBT chips, thus local chip temperature should be separately measured. Multiple measurement (three samples) were made for averaging the readings. The achievement of this test scenario was a relationship between $V_{CE,on}$ as a function of i_c and T_j, which is called $V_{CE,on_{cal}}$. The second stage was to apply a failure in the calibration circuit to find out the sensitivity of $V_{CE,on}$ to the progress of BWLO, while temperature is kept constant. The measured $V_{CE,on}$ is compared with the expected $V_{CE,on_{cal}}$ achieved by the calibration circuit in state one. The third state was detecting the failure mechanisms within the operation of the three-phase converter (Chapter 4) as described in Chapter 5.

One reason why T_j should be measured, is that in both the design and application phases the instantaneous T_j should be guaranteed not to exceed the maximum rating under all conditions. Estimating temperature through power loss and thermal modelling of the IGBT has the following negative points:

- T_j is estimated by monitoring an electrical parameter (t_{off}) particularly not affected by different BWLO.
- Early BWLO is detected by another electrical parameter ($V_{CE,on}$) that is sensitive to the progress of the failure.

Using two electrical parameters, one for estimation of temperature (t_{off}) and another to detect the premature BWLO ($V_{CE,on}$) in a novel combination provides a new health condition monitoring for an in-service IGBT. Other novel ways of combining electrical parameters could lead to other failure detection combinations. Another possibility for a three-phase converter is to compare parameters from all three half bridges as they are all essentially seeing the same conditions. A switching time algorithm was developed to calculate switching times in each sample interval, Figure 8.1.

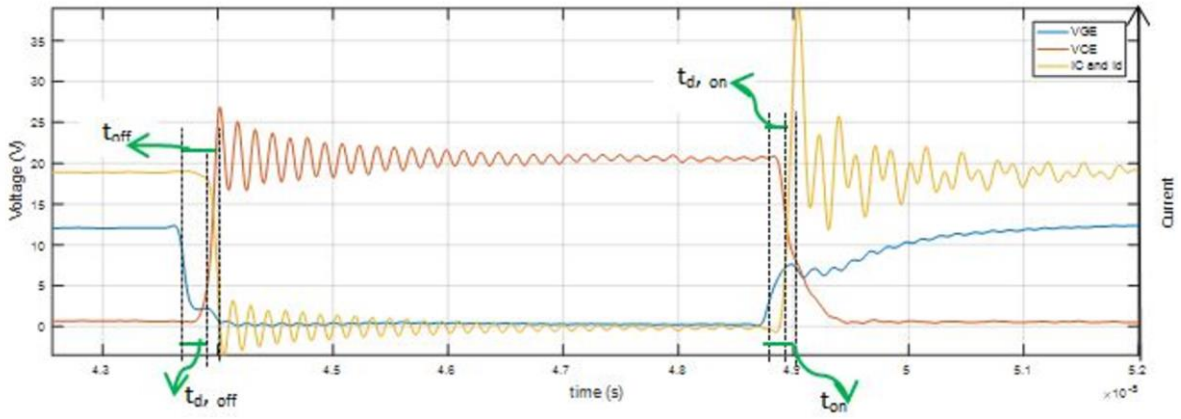


Figure 8.1: Switching parameters of the IGBT under test

Several measurements were carried out to check the repeatability of the developed algorithm. All these measurements have been carried out at the same conditions of temperature, DC-link voltage, load and speed. The temperature of heatsink was adjusted to 23, 51 and 70ºC to study the effect of temperature variations on switching parameters. The results plotted on the same vertical scale for a current of 60 A and a voltage of 70 V (Figure 8.2) show that with increase of temperature, switching time t_{off} is by far the most sensitive to temperature.

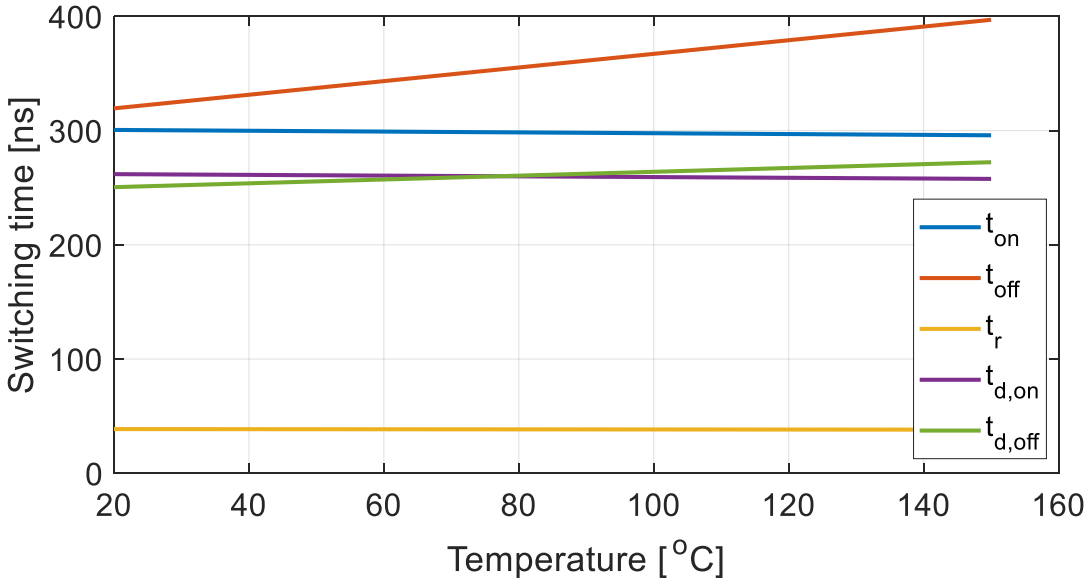


Figure 8.2: t_{on}, t_{off},t_r and t_f and $t_{d,on}$ and $t_{d,off}$ versus T_j ($i_c = 60\ A$)

A specific power was applied to the test set up to replicate temperature rise in substrate and baseplate of the IGBT to validate the thermal model. The same amount of power loss (as a heat flow) was applied to the thermal model. The results have been compared with the experiment results in order to tune the thermo-electrical model. The electrical characteristics of the IGBT are also tuned with the same

topology as explained above. The failure detectors of the IGBT were monitored and studied in healthy and unhealthy states.

BWLO and SF were emulated in the IGBT to understand the effect of failure mechanisms on the failure detectors. The on-state voltage ($V_{CE,on}$) at the high side IGBT has to be measured with mV accuracy in the presence of high common-mode voltages, potentially hundreds of volts. In order to accurately extract $V_{CE,on}$, a precision high common-mode voltage difference amplifier was used. Voltage $V_{CE,on}$ is measured as a failure parameter with a precision difference amplifier that capable of carrying high $V_{CE,off}$ during the off time of the IGBT. In theory, $V_{CE,on}$ is a function of i_c, V_{GE} and T_j. Voltage V_{GE} is assumed constant as the change is small and has little effect on $V_{CE,on}$ within its delta range. Therefore, $V_{CE,on}$ is modelled as a function of i_c and T_j in this work. The accuracy of measurement is investigated and verified by comparing the measured parameters with the $V_{CE,on}(T_j, i_c)$ specified in the datasheet. The accuracy of the amplifier is 1 mV which is enough to detect lift-off of a single bond wire. Voltage $V_{CE,on}$ has a sensitivity of 77 mV to one BWLO. This sensitivity significantly increases about 500 mV for three wires lift-off when one of the parallel dies is lost. t_{off} is used as a temperature estimator and has a sensitivity of 0.02 ns to the number of BWLO which is less than its sensitivity to the T_j 0.46 ns/ºC.

8.2 Modelling analysis

A thermal model of the IGBT's layer has been developed in PLECS environment. The thermal network is validated based on calculation of the thermal resistance and capacitance of each individual layer of the IGBT. The thermal model was validated based on a known heat source being applied to the thermal network and compared with the internal NTC sensor temperature rise together with thermocouples on the baseplate and heatsink. The BWLO was emulated by adding resistance in the IGBT emitter terminal. The conduction and switching power losses are assigned to the IGBT based on the experimental results and calculated results in chapters 5 and 6. A 2-D look up table is based on a series of measured electrical parameters with interpolation, the points of this 2-D are extracted and sent to a larger look up table. In this work the inflection point (shown in chapter 4) is 80 A, which is higher than the IGBT operation current recommended by the manufacturer - 50 A at 70º C. This means that a negative correlation of $V_{CE,on\ cal}$ with T_j is expected for lower than 80 A.

The sensitivity of $V_{CE,on\ cal}$ to T_j reduces with increasing current flow in the device. The maximum sensitivity of $V_{CE,on\ cal}$ to the temperature is seen at 20 A. Different sensitivity of $V_{CE,on\ cal}$ to the variations of T_j and i_c are found from the lookup table used to estimate $V_{CE,on\ cal}$. This helps to get a more accurate estimation of $V_{CE,on}$ under different load current and temperature conditions. A snubber circuit is added to the collector emitter IGBT terminal to damp voltage spikes and current oscillations.

This in turn increases the IGBT switching times and switching power losses when compared with datasheet figures and means that in practice calibration of switching times needs to be done using the final application circuit. Sensitivity of $V_{CE,on}$ to T_j is -4 mV/ºC at 20 A, decrease to -2.35 mV/ºC at 50 A and +1.25 mV/ºC at 100 A. A lookup table was also developed to estimate T_j by considering t_{off}, i_c and $V_{CE,off}$. Switching time t_{off} shows the highest sensitivity to i_c and T_j amongst all switching times. The sensitivity of t_{off} to T_j variations is 0.4 ns/ºC, which is twice its sensitivity to t_{on} and 8 times its sensitivity to $t_{d,on}$ and 10 times its sensitivity to $t_{d,off}$. As such, t_{off} is chosen as an estimator for T_j. Another thing that should be taken into account is the sensitivity of t_{off} to the progress of BWLO. t_{off} is obtained at each stage of the failure progress. The sensitivity of t_{off} from healthy state to full degradation as a result of BWLO is summarised in Table 8.1.

Table 8.1: Sensitivity of t_{off} to progress of bond wire lift off

Progress of failure	Sensitivity of t_{off} (ns)
One wire cut	0.02
Two wires cut	0.05
Three wires cut	0.11
Four wires cut	0.15
Five wires cut	0.23

Results also show that with the progress of BWLO, $V_{CE,on}$ increases to 77 mV for one wire cut, 186 mV for 2 wires cut, 620 mV for 3 wires cut, 930 mV for 4 wires cut and 1255 mV for 5 wires cut in a calibration circuit when the temperature is kept constant during the test.

8.3 Results justifications and critical analysis of data

One challenge is when $V_{CE,on}$ should be measured and analysed during the operation of the converter. This is due to normal operational change in T_j and i_c during power cycling of the converter. This means T_j and i_c should be continuously measured and considered when T_j is estimated. The i_c and T_j are applied in the lookup table to archive $V_{CE,on}$ called '$V_{CE,on_{-cal}}$'. This voltage $V_{CE,on_{-cal}}$ is compared with $V_{CE,on\_measured}$ that is measured by the differential amplifier. SF is detected by monitoring the variations of $R_{th,j-c}$ and varies from 0.49 in a healthy state to 0.74 for the fully degraded state.

As described, increasing T_j reduces $V_{CE,on}$ up to the inflection point at a current of 80 A. It is important to evaluate the source of electrical parameters variations, since both BWLO and SF can be monitored via variation of T_j and $V_{CE,on}$ and from which failure the variations originate. Firstly, the BWLO is highly likely to cause changes in $V_{CE,on}$ rather than temperature distribution in the layers. This is due to BWLO only affecting the current distribution from the die to the bond wires. Due to the small cross-

sectional area, these wires do not contribute to the heat transfer of the device and hence, their degradation does not make a significant modification to the temperature distribution. As a result, the only effective way to detect BWLO is through monitoring the electrical parameters. Secondly, $V_{CE,on}$ increases with the progress of BWLO whereas it reduces with progress of SF, at least for currents below 80 A. As such, an increase in $V_{CE,on_{measured}}$ in comparison with the $V_{CE,on-cal}$ can be a symptom of BWLO for i_c lower than 80 A. For i_c above 80 A, $R_{th,j-c}$ should be taken into account to understand whether $V_{CE,on_{measured}}$ originated from SF or from BWLO. If $R_{th,j-c}$, T_j and T_c increase from the expected value, then a rise in $V_{CE,on_{measured}}$ can be due to the presence of SF.

8.4 Support findings

The process of detecting BWLO is shown in the flowchart in Figure 8.3. $V_{CE.on\_measure}$ and $V_{CE,on_{cal}}$ are continuously changing during the operation of the converter. So long as the voltage difference between $V_{CE,on_{measure}}$ and $V_{CE,on_{cal}}$ shows less than a 10 % increase, no warning is issued. It should be noted that $V_{CE,on}$ is measured with an accuracy of 1 mV.

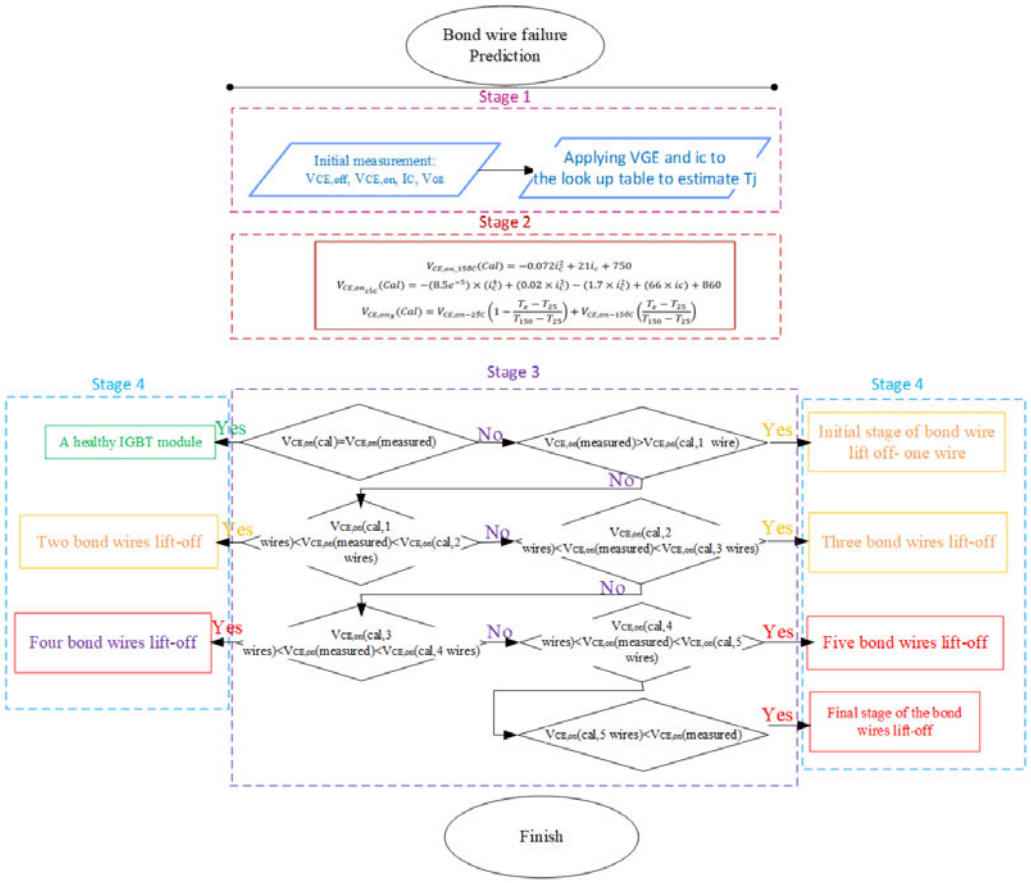


Figure 8.3: Flowchart to detect BWLO

The on-state V_{CE} is additionally increased if a second bond wire lifts off. The voltage changes, as a ratio to the original voltage, are shown in Figure 8.4. In this figure, $V_{CE,on}$ shows a jump in the voltage when 3 bond wires have been cut. This is because each IGBT has two dies and two pads with 6 bond wires.

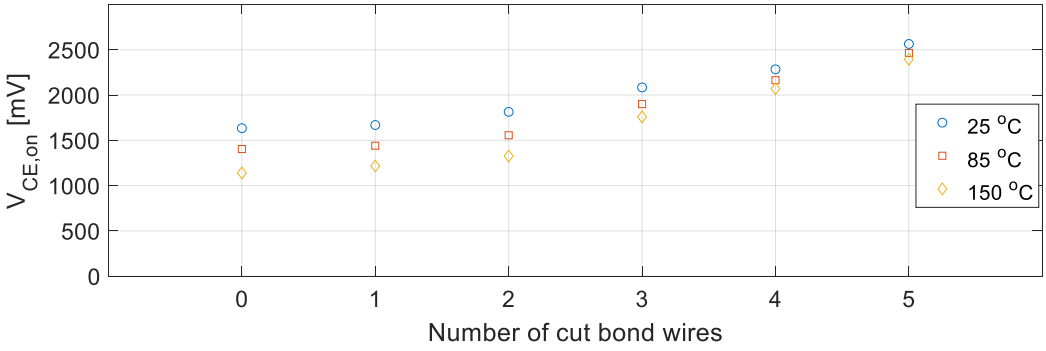


Figure 8.4: $V_{CE,on}$ against number of cuting bond wires at three temperatures

The VS-50mt060whtapbf power module has one die per IGBT chip. Each IGBT chip has an aluminium metallization pad and consists two dies in parallel for both high side and low side IGBT. Each pad is connected to the PCB using three bond wires, shown in Figure 8.5.

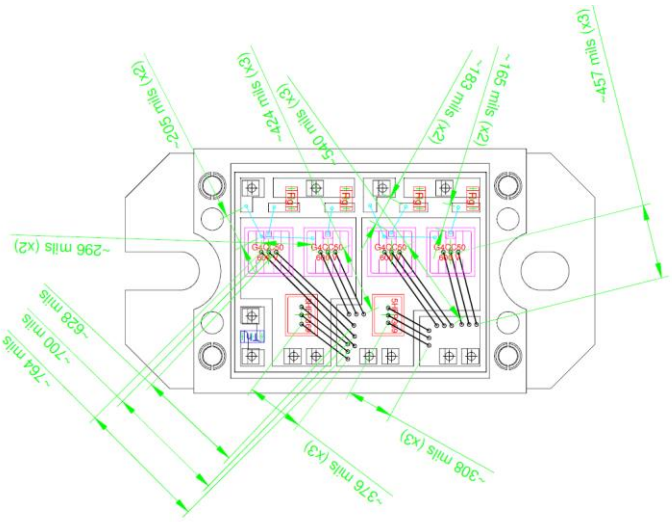


Figure 8.5: VS-50mt060whtapbf power module

Thus each IGBT has 6 wires in total that handle a rated current up to 50 A (100 ºC) per two dies. Consequently, each bond wire is carries a nominal maximum current of about 8 A. When a bond wire fails the current density in the die does not dramatically change since the current is still distributed between metallization pads (as two pads are in parallel). This will lead to gradual increase in $V_{CE,on}$ that is mainly due to the increase in voltage drop across the remaining bond wires. However, when one pad loses all its electric connections, the current density in the other pad doubles and this leads to a

significant jump in $V_{CE,on}$ measurement as shown in Figure 8.4. Figure 8.6 shows the sensitivity of $V_{CE,on}$ to the progress of BWLO, based on calculations according to (8.6).

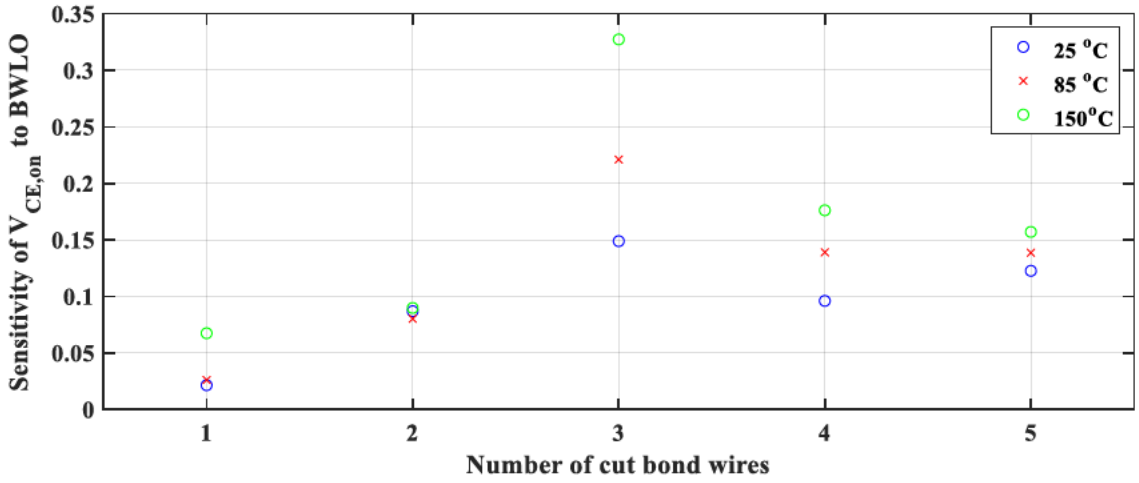


Figure 8.6: Sensitivity of $V_{CE,on}$ to the progress of BWLO

$$\frac{\Delta V_{CE,on}}{V_{CE,on(0)}} = \frac{V_{CE,on(n)} - V_{CE,on\_healthy}}{V_{CE,on\_healthy}} \tag{8.6}$$

where $V_{CE,on\_healthy}$ means the IGBT is in healthy state and no wires cut. $V_{CE,on(n)}$ describes the sensitivity of $V_{CE,on}$ at the number of lifted bond wires n.

Solder fatigue has been emulated by adding $R_{th_{j-c}}$ via inserting various thermal pads. Diagnosis of solder fatigue has been carried out by obtaining and monitoring of $R_{th_{j-c}}$. variations.

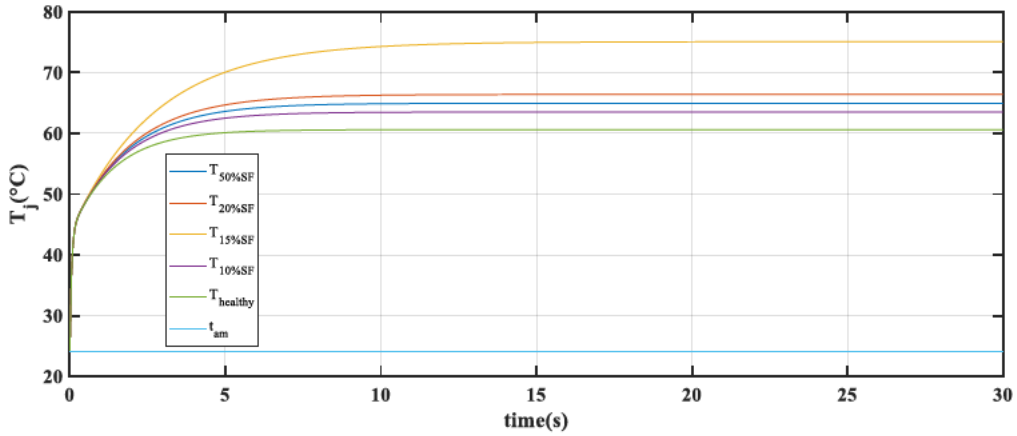


Figure 8.7: Transient temperature rise achieved in thermal model

The process is summarised in the flowchart in Figure 8.8**Error! Reference source not found.** The power losses are achieved by calculation of switching and conduction losses. Conduction loss is determined by measurement of $V_{CE,on}$ and i_c in a PWM duty cycle. Switching power loss is found using

a look up table for E_{on} and E_{off} as functions of i_c and temperature (and, implicitly, $V_{CE,off}$). To find out the health state of the IGBT, $R_{thj-c(measured)}$ is compared with $R_{th_{j-c,cal}}$. T_j rises 6.4ºC in 20% of increase in thermal resistance, considering the sensitivity of $V_{CE,on}$ to the T_j at 13 A at 24ºC ambient temperature, $V_{CE,on}$ will decrease from 1250 mV in healthy status to 1233.4 mV in solder degradation.

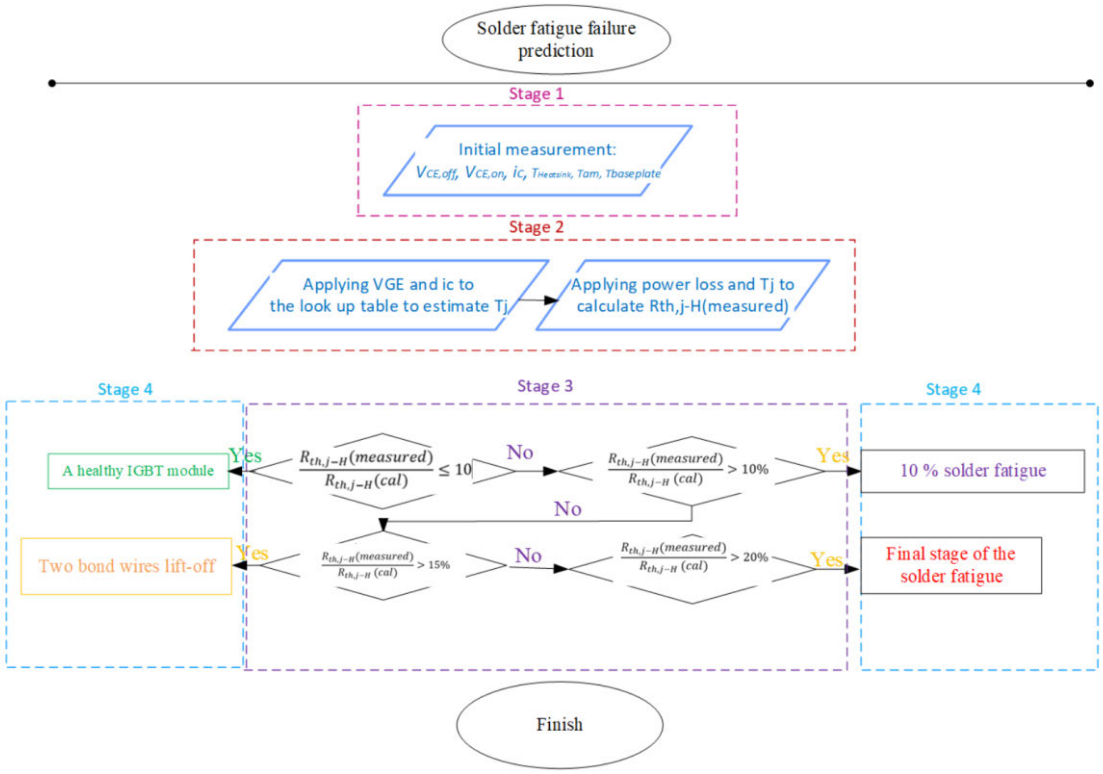


Figure 8.8: Flowchart to detect solder fatigue

The flowchart in Figure 8.9 summarises the health condition monitoring system, considering both bond wire, lift-off and solder fatigue. Initially electrical parameters such as V_{GE}, i_c, $V_{CE,off}$, $V_{CE,on}$ and T_c are measured. Both V_{GE} and i_c are analysed through the state machine algorithm to find t_{off}. Then $R_{th,j-c}$ is obtained by considering power loss of the IGBT and T_j. To find the health status of the IGBT in next step $V_{CE,on}$ is compared with $V_{CE,on-cal}$, if they are within 10% rise, then the IGBT is in a healthy state, otherwise the level of degradation and type of failure will be analysed by the state machine algorithm based on i value as shown in flow chart.

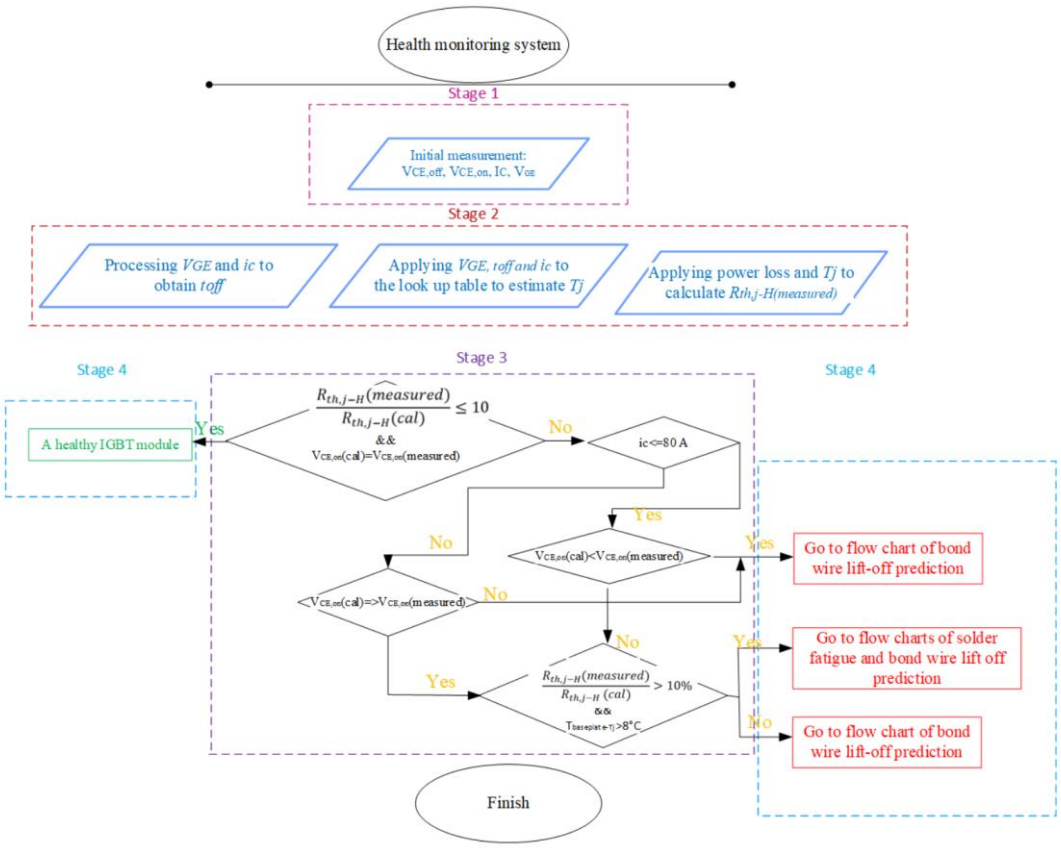


Figure 8.9: Fowchart to detect solder fatigue and BWLO.

8.5 Conclusion and summary

There is a lack of understanding on how temperature variations can affect the reliability of failure diagnostics in an IGBT health condition monitoring system in previous studies. As the modelling results in chapter 7 suggest, with changes in wind speed the output current and fundamental frequency of the generator will change. This affects $T_{j,max}$ and ΔT_j of the IGBT. Variations of T_j are also a symptom of degradation in the IGBTs, in fact variations of almost all inherent electrical parameters of the IGBT results in variations of T_j. Using the electrical parameters as failure detectors can raise the possibility of misinterpreting a healthy IGBT as needing attention, resulting in an increase in costs rather than a decrease. As such, T_j should be estimated by electrical parameters that show very low sensitivity to the progress of the failure. In this work t_{off} has been suggested to be used as a temperature estimator. A discussed in chapter 4, the sensitivity of t_{off} to the progress of bond wire deterioration and breakage is negligible. Monitoring switching times within operation of the converter is also another challenge. In other words, finding exact points where 90% and 10% of V_{GE} and i_C is also a challenge in a real application (within operation of three-phase converter). This challenge is due in part to fast switching of the IGBT resulting in short measurement sampling interval (2.1 G sample per second which is

equivalent to a sampling interval of 0.48 ns) being required at very high sampling frequencies, but also current oscillation and transient voltage spikes when changing from the 'on' state to the 'off' state and back again.

To address this switching time measurement challenge a state machine was developed and applied, so that 10% and 90% of i_c can be found according to the nearest points to 90% V_{GE} during turning off time and 10% of V_{GE} during turning on time. Voltage $V_{CE,on}$ is used as a failure detector as it has shown high sensitivity to the i_c and hence BWLO that was discussed in detail in this chapter and chapter 5. The possibility of the measurement of $V_{CE,on}$ during operation of three-phase converter (described in chapter 4) has been discussed further in this chapter. The proposed failure detector can detect the progress of BWLO and shows an observable increase, especially when the third bond wire is detached. Solder fatigue is another common failure within an IGBT. This failure affects temperature distribution of the IGBT due to change in $R_{th,j-c}$. As such the T_j estimator (t_{off}) is not independent from progress of failure this failure. Variation of $R_{th,j-c}$ at any specific load current and T_j can be distinguished as a solder fatigue failure detector if $R_{th,j-c}$ is compared with what is expected from $R_{th,j-c,cal}$. The effect of solder fatigue on $V_{CE,on}$depends on i_c (being either higher or lower than the inflection point). However, $V_{CE,on}$ always increases with the progress of BWLO .In conclusion, $R_{th,j-c}$, $V_{CE,on}$, T_c, T_j and t_{off} are used as failure detectors

Chapter 9: Thesis conclusions

This chapter summarises the results from previous chapters and the achievements of each of the original objectives.

9.1 Final original contribution

This work originated as part of "Aeolus4Future" Marie Skłodowska-Curie innovative training network, aiming to promote "efficient harvesting of wind energy". The author (of this thesis) was in charge of work package 6, improving the condition monitoring of the WT, in collaboration with the University of Bochum (Ruhr-Universität Bochum, Germany). Work package 6 was divided into two subsections: 6.1 – condition monitoring of WT structures (Ruhr University of Bochum); and 6.2 – condition monitoring of the electrical drive train of power electronic converters in WTs (University of Birmingham). As described in chapter 1, improving the reliability of health condition monitoring of semiconductor components (IGBTs) used in power electronic converters will reduce unplanned downtime and the associated costs for WTs. This has been the main motivation of this thesis. Two under-researched issues were identified, summarised by two separate problems:

- Proposing failure detection methods to evaluate the health status of the IGBTs in the face of variation in load variations (wind speed).
- To investigate the feasibility of measurement and analysis of the proposed failure detectors in an operational three-phase converter.

These two problems have been tackled by conducting lab experiments on a single-phase calibration circuit for initial electrical characterisation of an IGBT in its healthy state. A three-phase converter (described in Chapter 4) was used to study the capability of monitoring of the proposed electrical parameters during normal its operation. Numerical modelling of the WT converter and IGBT have helped in the understanding of the effect of wind speed variations on the health of the IGBTs.

The two problems have been addressed by a list of objectives to approve the hypothesis and assumptions that were presented in Chapter 1. Table 9.1 summarises the list of objectives that were presented in Chapter 1, and the associated outcomes.

Table 9.1: List of objectives and associated outcomes

Objectives	Outcomes
1. Literature review: The challenges associated with previous health condition monitoring approaches.	• From the literature review, there is a lack of understanding of how different failure mechanisms cause false alarm in the health condition monitoring system. • There is a lack of understanding of how load variations can affect the reliability of a health condition monitoring systems.
2. To propose effective electrical failure detectors that are sensitive to the progress of the failures and can be feasibly calibrated in healthy and unhealthy states of IGBT. (effect of BWLO on $V_{CE,on}$ as a failure detector)	• Very accurate estimation of one wire lift-off (1300 mV) within the operation of the converter. • Significant rise in $V_{CE,on}$ value while losing one parallel silicon die • Sensitivity of $V_{CE,on}$ to variation of T_j is not constant and shows maximum sensitivity at 20 A, but also it does not have same trend of variations. The sensitivity of $V_{CE,on}$ to T_j is positive after inflection point (80 A) and negative before the inflection point.
3. To find out an appropriate method of processing the measured data corresponding to the electrical failure detectors and also to validate the measured data. (Effect of solder fatigue on $V_{CE,on}$ as a failure detector)	• Switching on time has no observable sensitivity to the load variations. • Difficulty to obtain switching times within operation of the converter has been tackled by a state machine algorithm to find out the exact points associated with fall time of IGBT. • Only the switching-off time of the IGBT shows any useable sensitivity (0.45 ns/ºC) to junction temperature variations. • Solder fatigue is detectable through monitoring $V_{CE,on}$. • Monitoring of T_j and $V_{CE,on}$ are not enough to monitor health of IGBT while both solder fatigue and BWLO are prone to occur. • The trend variations of $V_{CE,on}$ in the presence of solder fatigue depends on

	the collector current (i_c>80 A or i_c< 80 A).
To generate a temperature estimator to be independent from the progress of BWLO in order to independently measure temperature variations from load variations. (Propose a temperature estimator to be independent from progress of the failure.)	• Switching-off time has low sensitivity to the progress of BWLO, about 0.1 ns/ºC.
4. To numerically model the WT in order to understand the effect of wind speed variations on IGBT. (Effect of wind speed variations on the health status of IGBT.)	• Wind speed variations causes temperature rise at the IGBT that follows the same trend as that of a failure detector. • Having pitch angle controller can reduce temperature stresses on the IGBTs. • Wind speed variations affect the current amplitude and fundamental frequency of WT rotor-side converter current output. The former will change the maximum junction temperature and the latter will change the temperature swings.
5. To measure and detect early failure mechanisms within operation of three-phase converter by the proposed electrical failure detectors.	•

9.2 Key findings for detecting BWLO and SF

With respect to the failure detection for an IGBT module used in the power electronic converters, th answer to the hypothesis (it is possible to improve existing the health condition minoring of IGBT) and main research contributions to existing knowledge are listed below:

1. A new method of temperature detection that is uncoupled to the common failure mechanisms (the bond wire lift-off and solder fatigue) in wind turbines.
2. Introduced a new temperature estimation method that is uncoupled to common failure mechanisms
3. Estimation of junction temperature by using an IGBT electrical parameter during the operation of converter with an accuracy of ±2ºC.
4. Presented an 'in-sutu' measurement technique to detect premature failures; with an accuracy of detection of one wire lift-off with an increase of 10%. The technique is practically applicable in wind turbine applications.
5. Presented a temperature estimator that is independent of the progress of failure.

9.3 Future purpose and accountability

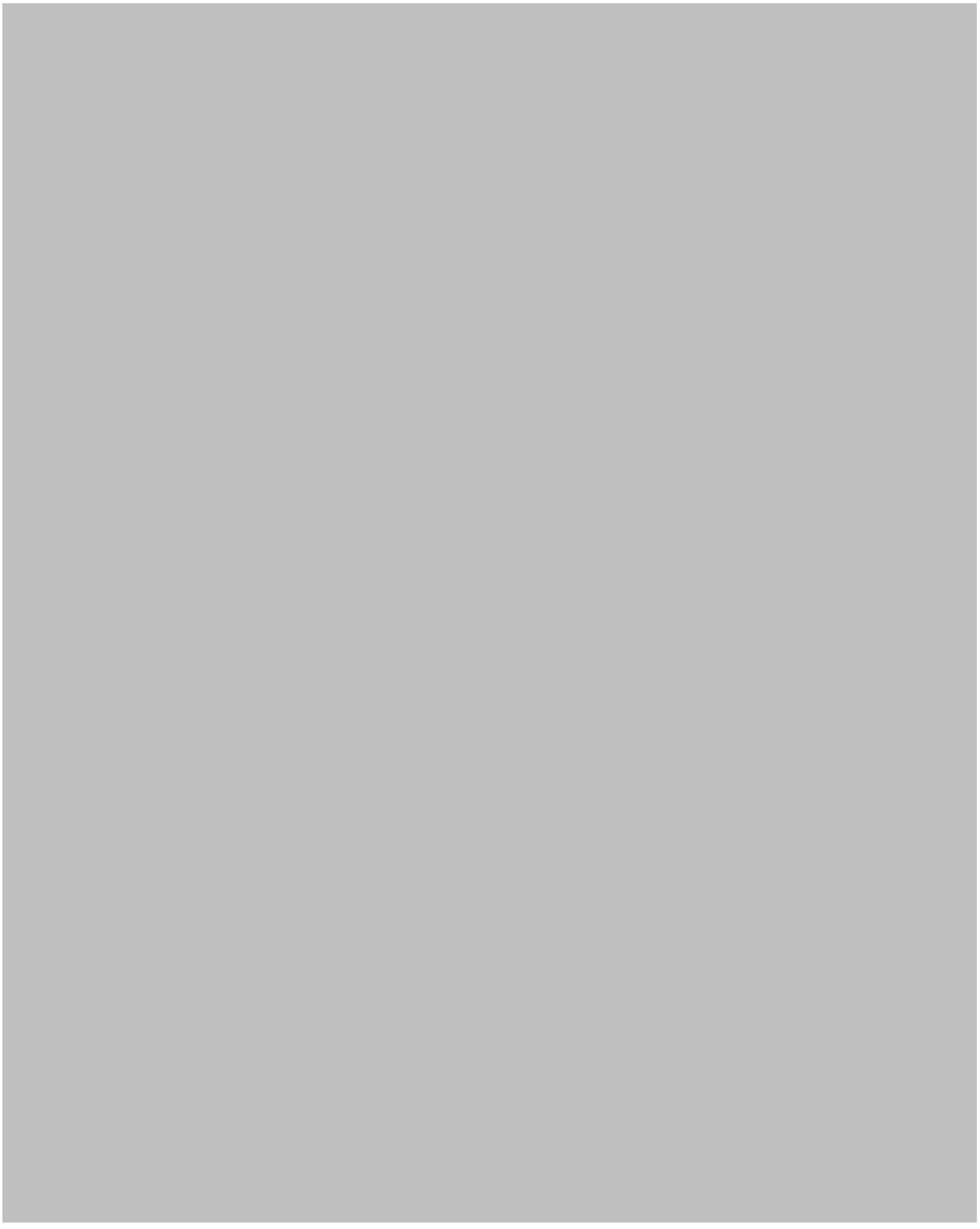
The experimental outcomes from and numerical modelling proposed in this work confirm that BWLO and solder fatigue can be detected by monitoring three parameters, switching-off time (t_{off}), junction temperature (T_j) and thermal resistance from junction to case ($R_{th,j-c}$). From modelling results it is confirmed that wind speed variations cause changes in the temperature profile of the IGBTs. Continuous monitoring of T_j within an operation of converter and finding the associated $V_{CE,on_{cal}}$ to compare with measured $V_{CE,on}$ can stop false errors from being reported by a health condition monitoring system.

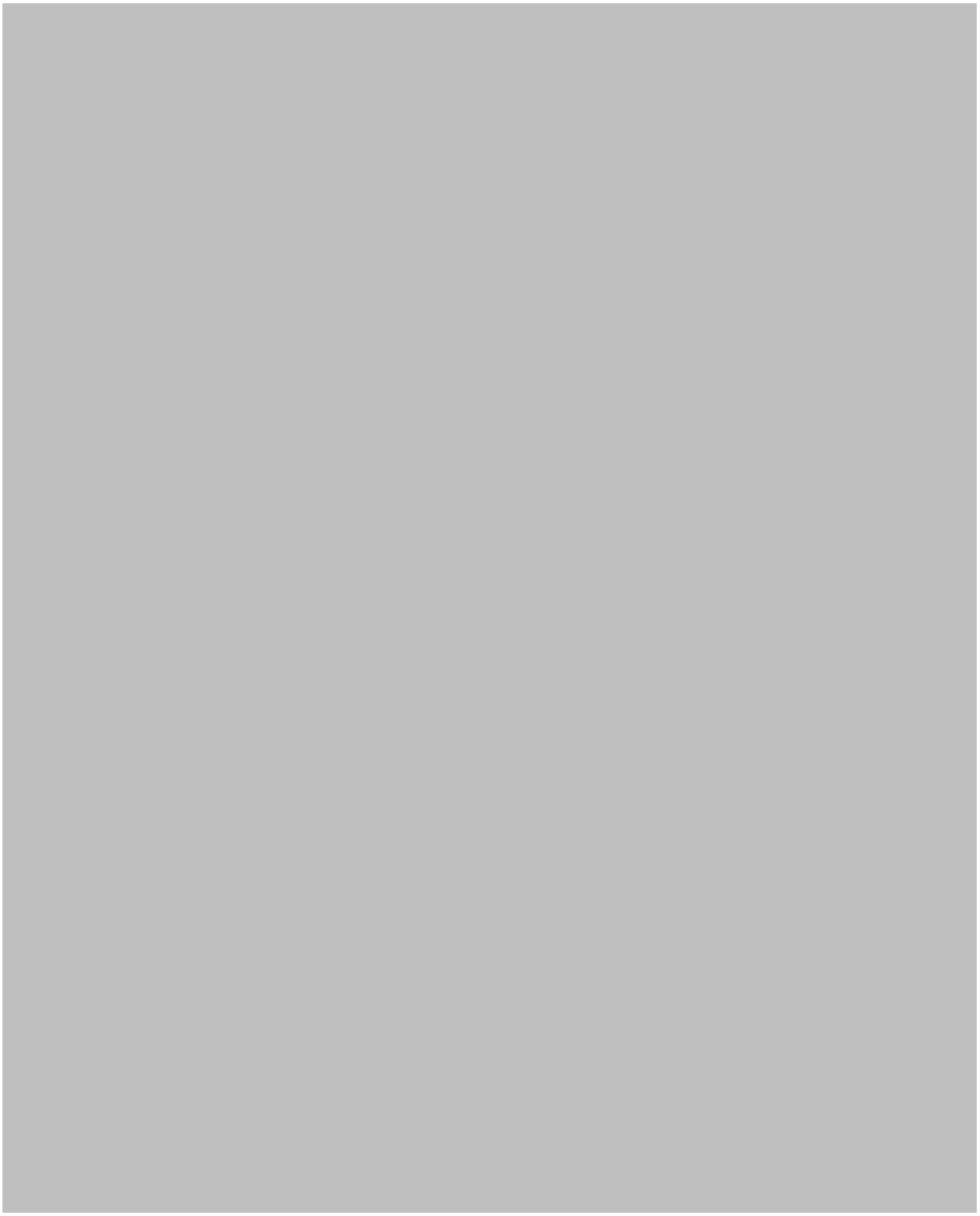
However, further study is required to expand the implementation of the proposed health condition monitoring system on the back-to-back converter of a commercial WT. It is also necessary to investigate further the detailed effect of wind flow on the health condition monitoring during operation of the converter.

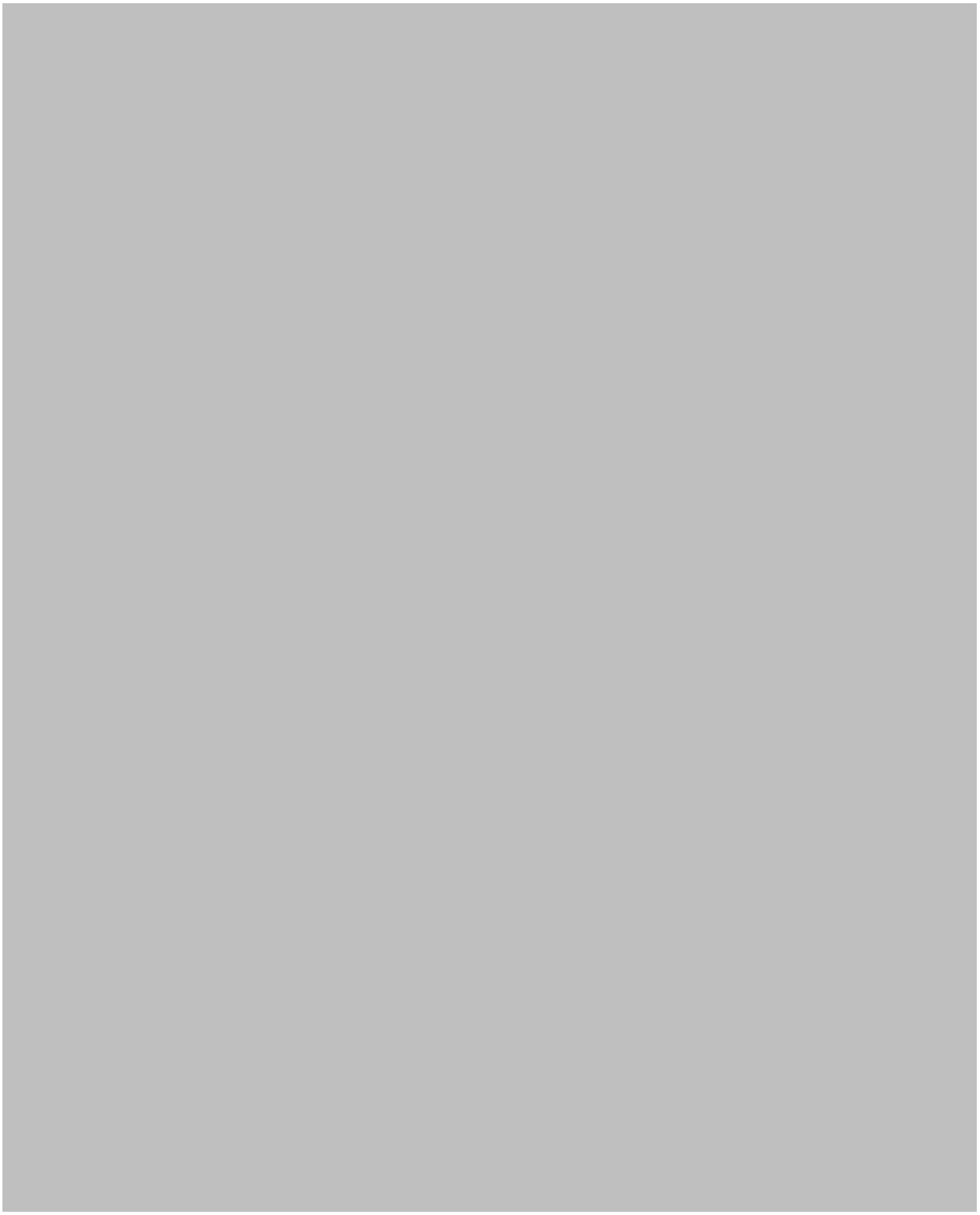
It would be worthwhile to study the effect of wind speed variations on junction temperatures of the IGBT by using the numerical model presented in chapter 7 and combining with the thermal model of the IGBT.

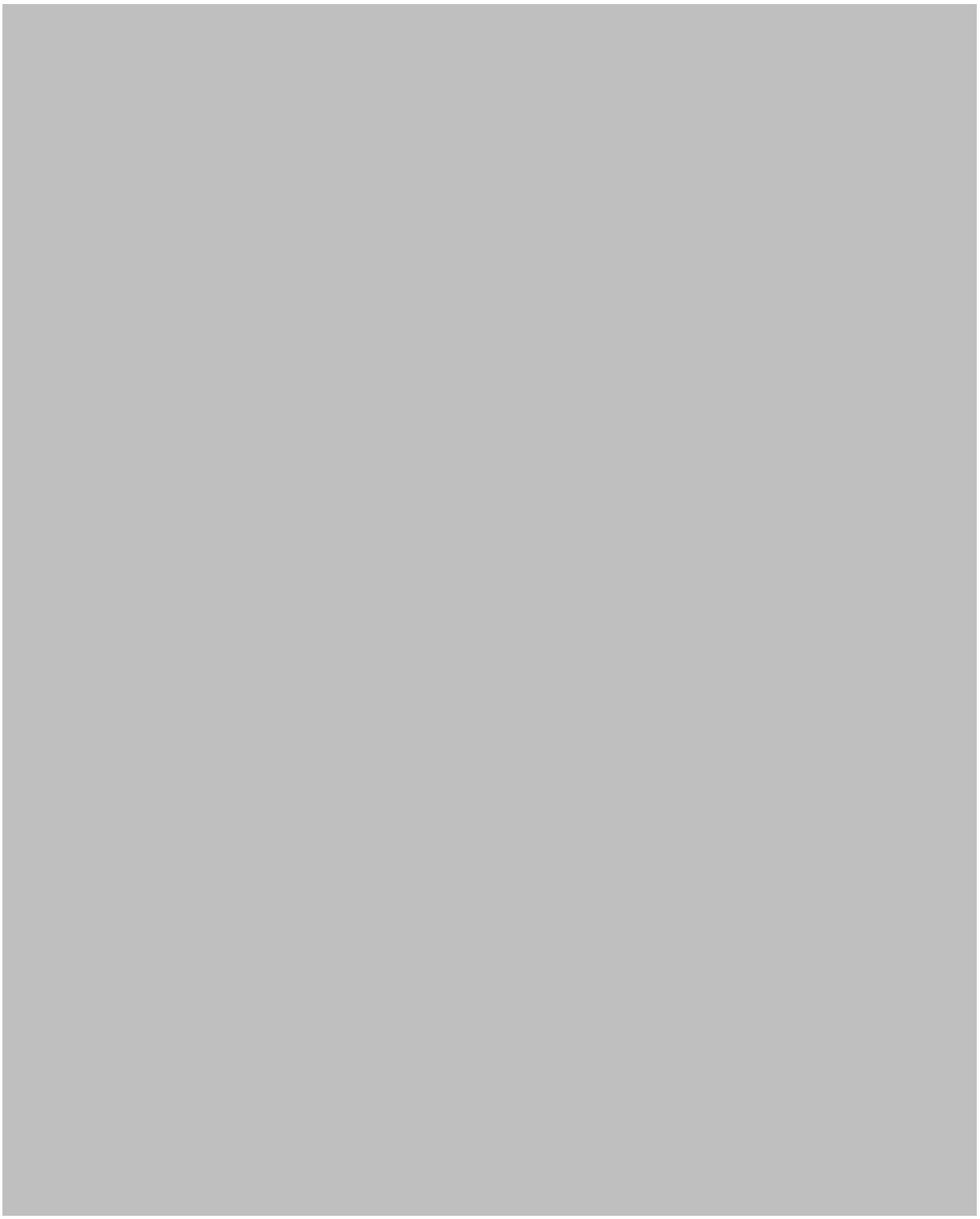
In this work a health condition monitoring algorithm for detecting early degradation of IGBT has been proposed; however, more intelligent algorithm such as fuzzy decision making and neural network could be applied to the 'big data' that is potentially available from a wind farm containing many WTs of identical design in similar wind conditions to determine health level of IGBT module within operation of the converter.

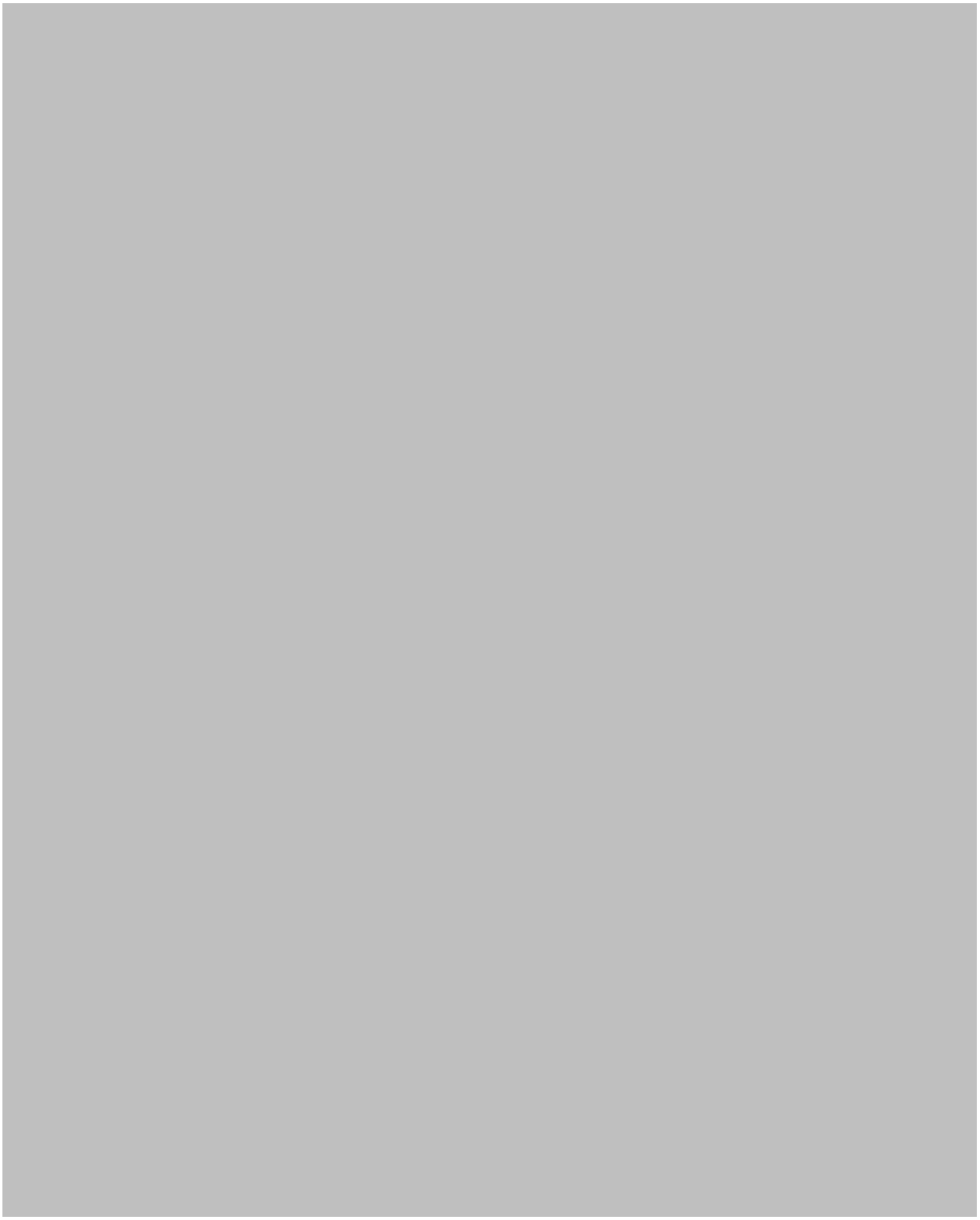
Appendix A: IGBT module datasheet

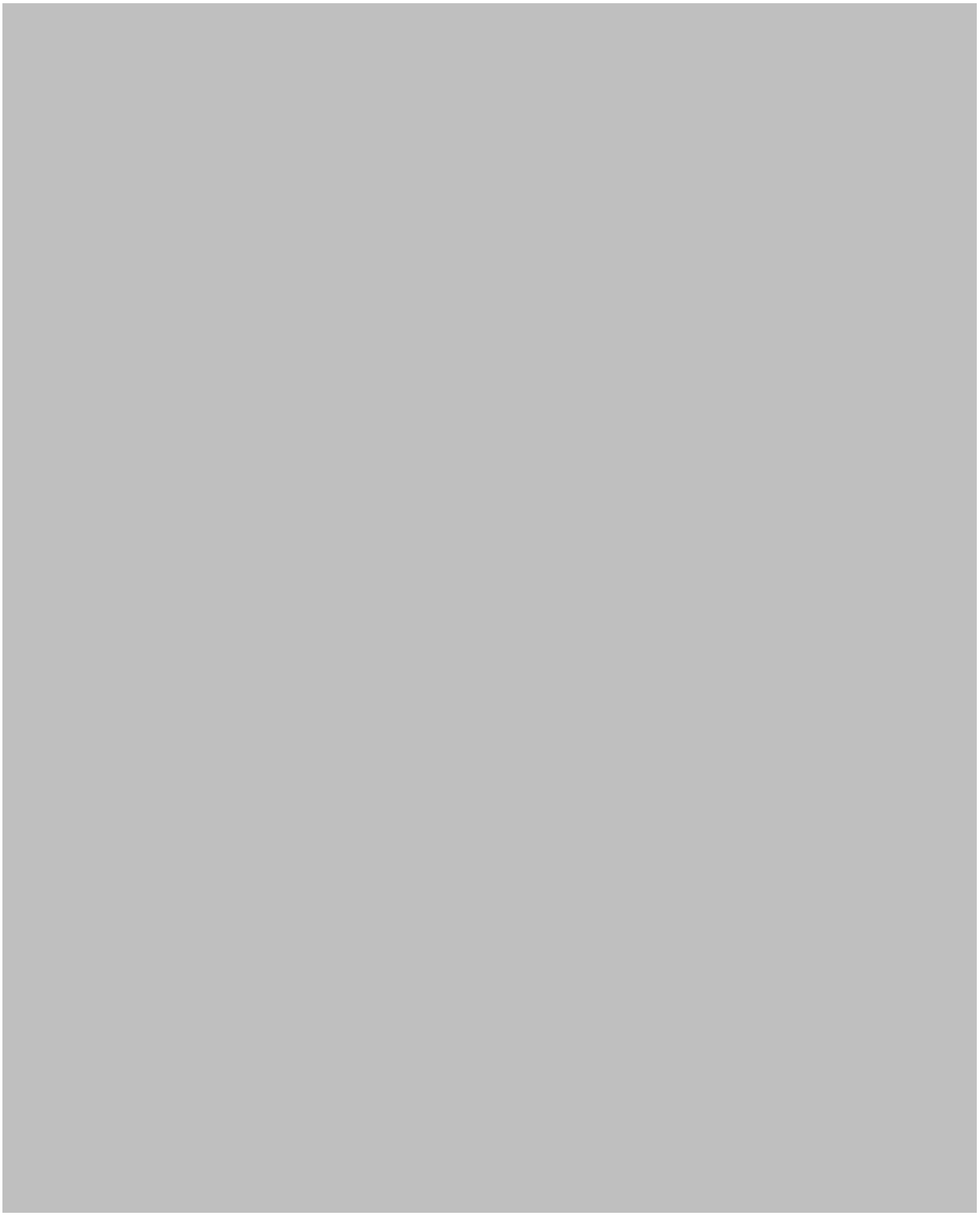


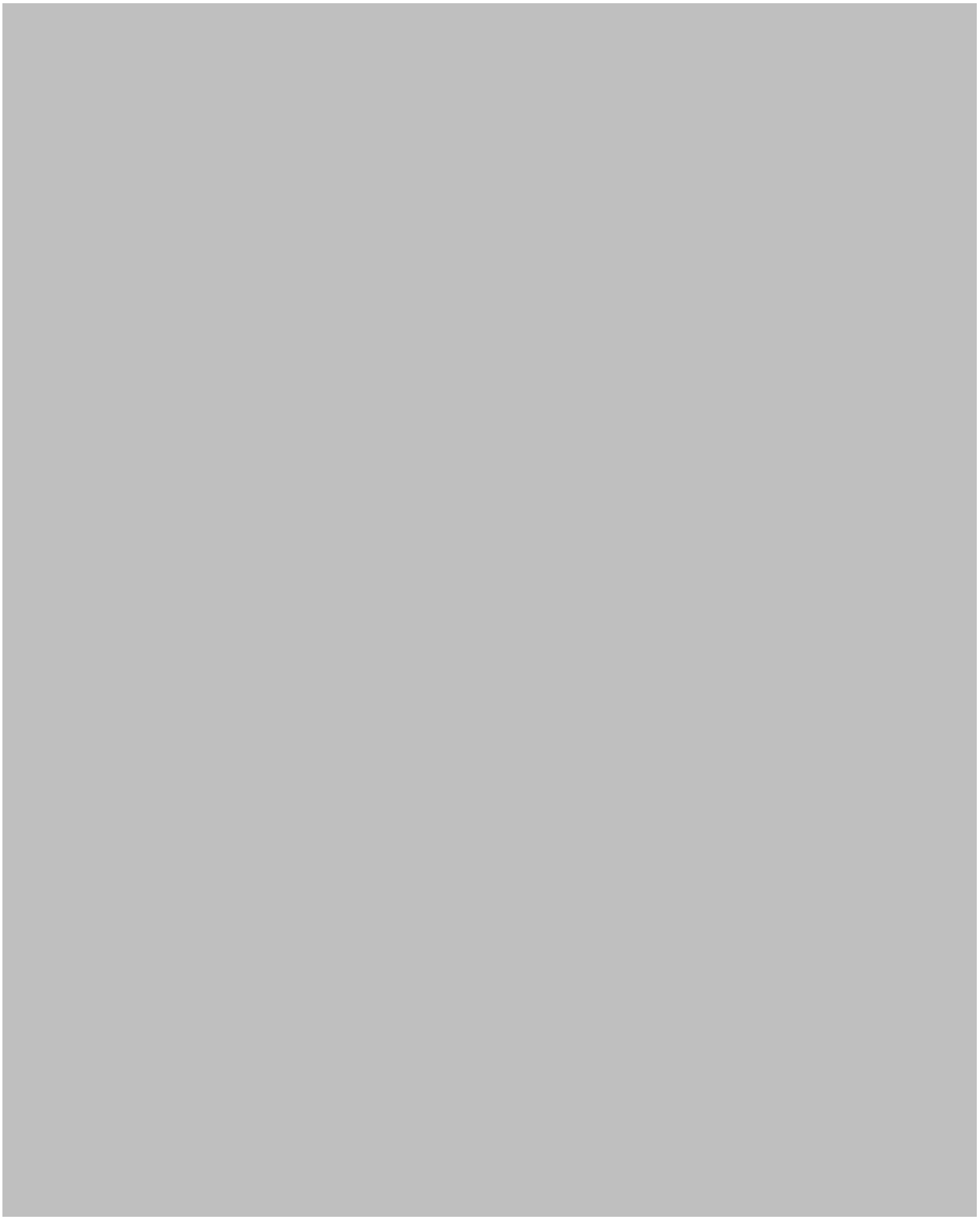




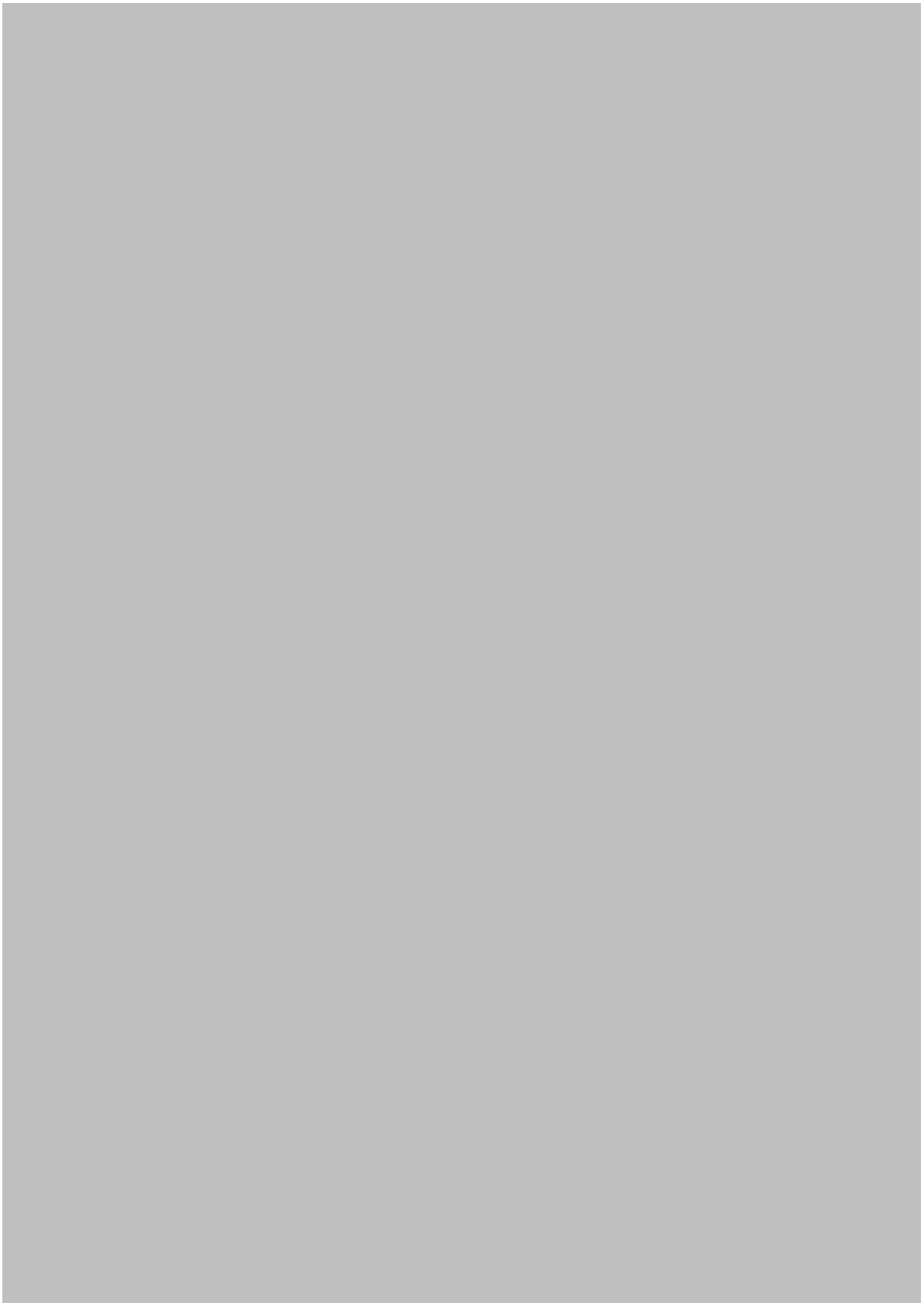


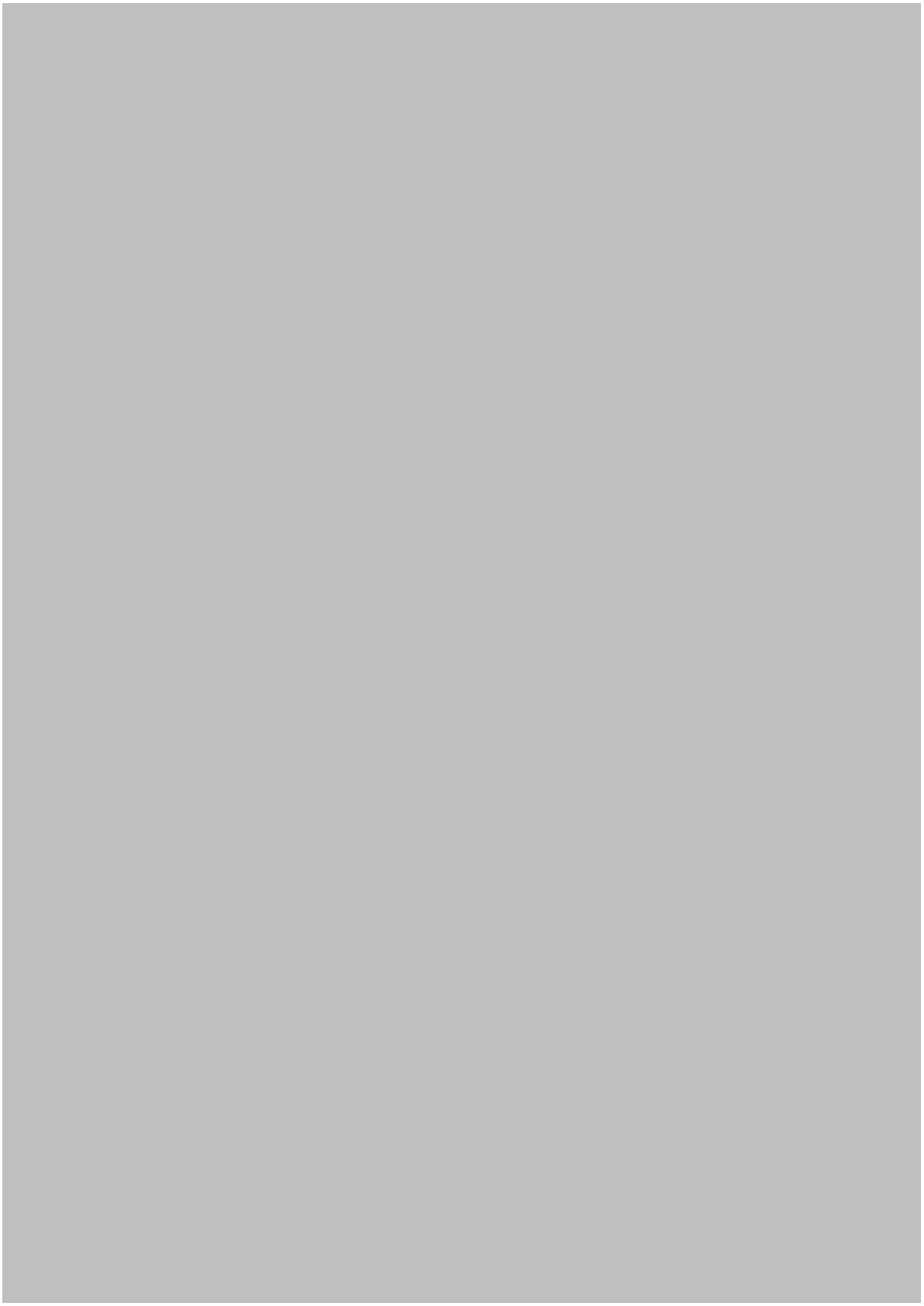


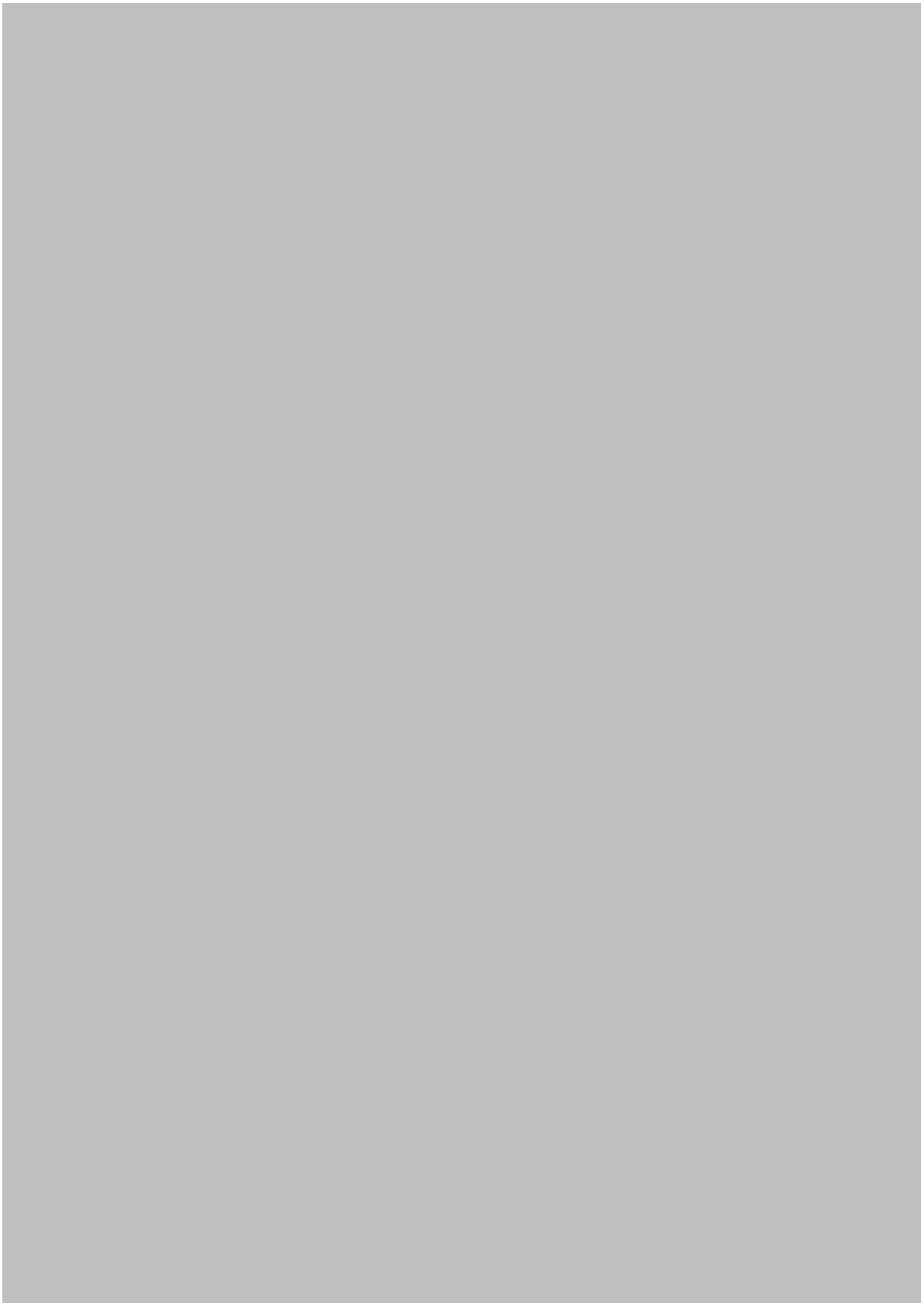


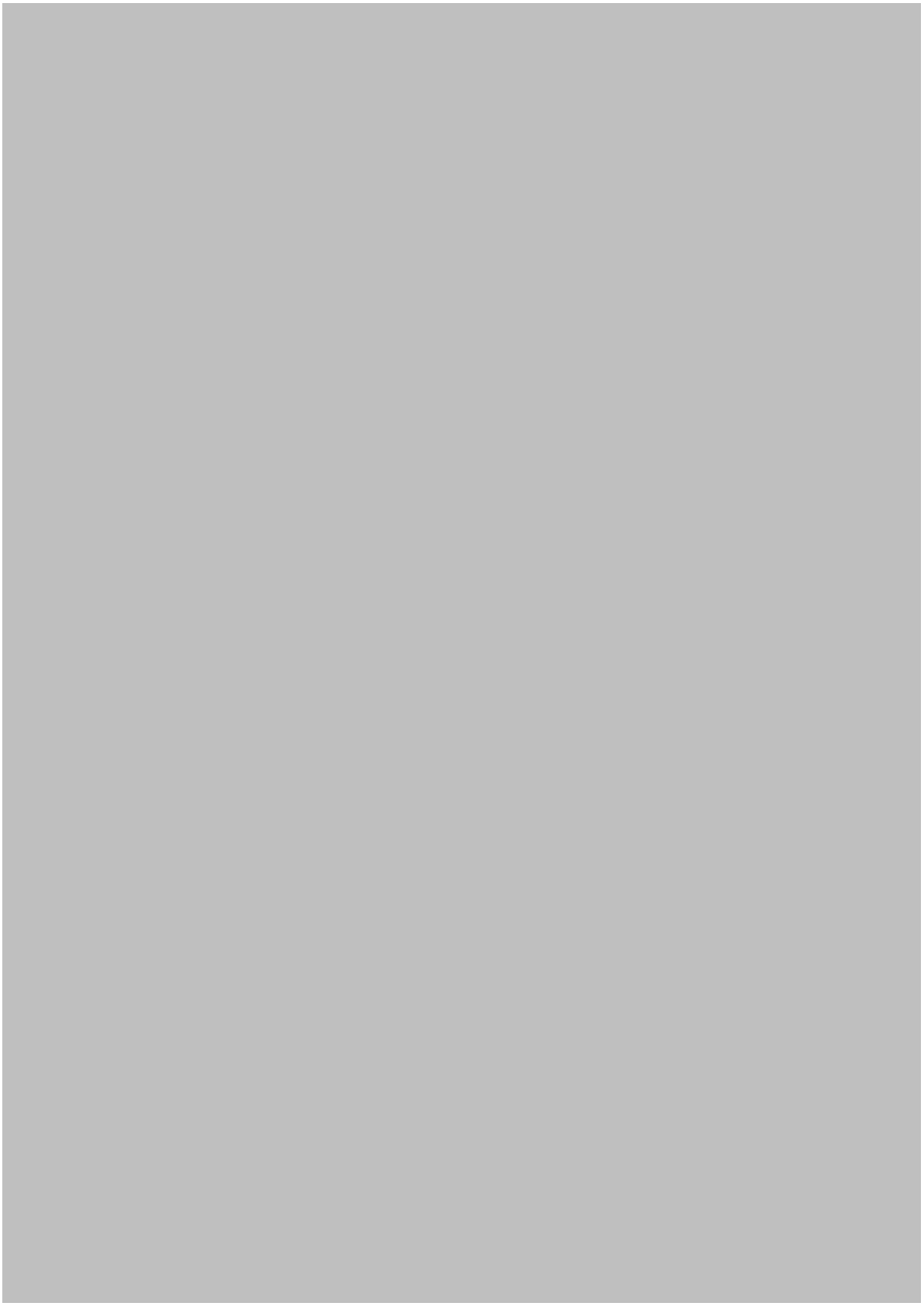


Appendix B: Wind turbine datasheet









به پایان آمد این دفتر

حکایت همچنان باقیست.....